



GRL Platform Solutions

DP2.1 PHY CTS UHBRx Sink MOI

[Note: In this MOI, the GRL-DP21-SINK-AN Calibration and Test Software is used to automate the DisplayPort 2.1 PHY CTS UHBRx Sink testing along with the Anritsu MP1900A BERT and Keysight/Tektronix scope.]

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TABLE OF CONTENTS

1	INTRODUCTION	9
2	RESOURCE REQUIREMENTS	10
2.1	EQUIPMENT REQUIREMENTS	10
2.2	SOFTWARE REQUIREMENTS	12
3	INSTALLING AND SETTING UP GRL-DP21-SINK-AN SOFTWARE	13
3.1	DOWNLOAD AND SET UP GRL-DP21-SINK-AN SOFTWARE	13
3.1.1	On the Anritsu MP1900A BERT.....	13
3.1.2	On the PC Used for GRL Platform Solutions Framework Installation.....	14
3.1.3	Set Up Remote File Server	17
3.2	CONFIGURE THE GRL-DP21-SINK-AN SOFTWARE BEFORE CALIBRATION AND TESTING....	18
3.2.1	Enter Calibration/Test Session Information.....	18
3.2.2	Set Up Conditions for Calibration/Testing	19
3.2.3	Set Up AUX Controller for DUT Test Automation	21
3.3	SELECT CALIBRATION/TEST.....	25
3.4	CONFIGURE CALIBRATION/TEST PARAMETERS	26
3.5	CONFIGURE CALIBRATION TARGET VALUES.....	30
3.6	RUN CALIBRATION/TESTS.....	31
4	SINK CALIBRATION CONNECTION SETUPS	32
4.1	PRE-CALIBRATION/TEST PROCEDURES	32
4.2	CONNECTION SETUP FOR ANRITSU MP1900A BERT GENERATOR SET	32
4.3	DISPLAYPORT USB TYPE-C FIXTURE CONNECTOR PIN ASSIGNMENTS.....	33
4.4	STANDARD/MINI DISPLAYPORT FIXTURE CONNECTOR PIN ASSIGNMENTS.....	34
4.5	CALIBRATION CONNECTION SETUPS.....	35
4.5.1	Calibration Setup at TP1	35
4.5.2	Calibration Setup at TP3_EQ for DisplayPort USB Type-C Mode.....	36
4.5.3	Calibration Setup at TP3_EQ for Standard/Mini DisplayPort Mode	38
5	SINK DUT COMPLIANCE TEST SETUPS	42
5.1	TEST CONNECTION SETUPS.....	42
5.1.1	DUT BER Compliance Test Setup at TP2 for DisplayPort USB Type-C Mode.....	42
5.1.2	DUT BER Compliance Test Setup at TP2 for Standard/Mini DisplayPort Mode	44
5.1.3	DUT BER Compliance Test Setup at TP3_EQ for DisplayPort USB Type-C Mode	46
5.1.4	DUT BER Compliance Test Setup at TP3_EQ for Standard/Mini DisplayPort Mode	48
5.1.5	Margin Testing.....	51
6	TEST RESULTS AND REPORTS USING GRL-DP21-SINK-AN	52
6.1.1	DUT Information	53

6.1.2	Results Summary Table	53
6.1.3	Calibration & Test Result Details	54
6.2	DELETE TEST RESULTS.....	56
7	SAVING AND LOADING TEST SESSIONS	57
8	APPENDIX A: MANUAL CTS SINK CALIBRATION AND TEST PROCEDURE	58
8.1	PRESET CALIBRATION FOR UHBR10, UHBR13.5 AND UHBR20.....	58
8.1.1	Set Up Oscilloscope.....	61
8.1.2	Record Preset Measurements.....	63
8.2	CALIBRATE RECEIVER STRESSED EYE FOR UHBR10 (10.0 GBIT/S) AT TP1.....	68
8.2.1	Set Up Oscilloscope.....	74
8.2.2	Record ISI Measurements.....	78
8.3	CALIBRATE AND SAVE FOR UHBR10 (10.0 GBIT/S) RECEIVER AT TP3_EQ.....	93
8.4	CALIBRATE AND SAVE FOR UHBR13.5 (13.5 GBIT/S) RECEIVER AT TP1.....	98
8.4.1	Set Up Oscilloscope.....	98
8.4.2	Record ISI Measurements.....	100
8.5	CALIBRATE AND SAVE FOR UHBR13.5 (13.5GBIT/S) RECEIVER AT TP3_EQ	102
8.6	CALIBRATE AND SAVE FOR UHBR20 (20.0 GBIT/S) RECEIVER AT TP1	107
8.6.1	Set Up Oscilloscope.....	107
8.6.2	Record ISI Measurements.....	109
8.7	CALIBRATE AND SAVE FOR UHBR20 (20.0 GBIT/S) RECEIVER AT TP3_EQ	111
9	APPENDIX B: CONNECTING KEYSIGHT OSCILLOSCOPE TO PC117	
10	APPENDIX C: CONNECTING TEKTRONIX OSCILLOSCOPE TO PC119	

List of Figures

Figure 1. Turn on Miscellaneous System	14
Figure 2. Select and Launch GRL Platform Solutions Framework	14
Figure 3. Start DisplayPort Sink Test 2.1 Application	14
Figure 4. See License Details.....	15
Figure 5. Check License for Installed Application	15
Figure 6. Connect Instruments with GRL Platform Solutions Software.....	16
Figure 7. Installed GRLRemoteProxyServer.exe File Directory	17
Figure 8. Verify Proxy Server Connection for Control PC and Scope.....	17
Figure 9. Configure Remote Proxy Server Network Settings on GRL Platform Solutions Software.....	18
Figure 10. Session Info Page.....	18
Figure 11. Select Lane Under Tests	19
Figure 12. Compliance Test Conditions	19
Figure 12. Select Test Points.....	20
Figure 13. Select Data Rates	20
Figure 14. Select SJ Frequencies	20
Figure 15. Select AUX Controller	21
Figure 16. UCD323 DP Source Console— #1.....	21
Figure 17. UCD323 DP Source Console— #2	22
Figure 18. UCD323 DP Source Console— #3	22
Figure 19. Detect Unigraf UCD-323 Aux Controller in Control PC.....	23
Figure 20. Open License Manager	23
Figure 21. UCD License Screen	24
Figure 22. Install DisplayPort Reference Source License.....	24
Figure 23. Calibration Selection	25
Figure 24. Tests Selection.....	25
Figure 25. Parameters Configuration Page	26
Figure 26. Calibration Overwrite	31
Figure 27. Run Tests Page	31
Figure 28. Connection Setup for MP1900A BERT Generator Set Modules	32
Figure 29. DisplayPort USB Type-C Receptacle Fixture Connector Pin Assignments.....	33
Figure 30. DisplayPort USB Type-C Plug Fixture Connector Pin Assignments	33
Figure 31. Standard/Mini DisplayPort Receptacle Fixture Connector Pin Assignments.....	34
Figure 32. Standard/Mini DisplayPort Plug Fixture Connector Pin Assignments	34
Figure 33. Typical TP1 Sink Calibration Setup	35
Figure 34. Setup for TP3_EQ Calibration at 10G for DisplayPort USB Type-C Mode.....	36
Figure 35. Setup for TP3_EQ Calibration at 13.5G for DisplayPort USB Type-C Mode.....	37
Figure 36. Setup for TP3_EQ Calibration at 20G for DisplayPort USB Type-C Mode.....	38
Figure 37. Setup for TP3_EQ Calibration at 10G for Standard/Mini DisplayPort Mode	39

Figure 38. Setup for TP3_EQ Calibration at 13.5G for Standard/Mini DisplayPort Mode	40
Figure 39. Setup for TP3_EQ Calibration at 20G for Standard/Mini DisplayPort Mode	40
Figure 40. BER Compliance Test Setup for DP Sink DUT at TP2 for DisplayPort USB Type-C Mode	42
Figure 41. BER Compliance Test Setup for DP Sink DUT at TP2 for Standard/Mini DisplayPort Mode	44
Figure 42. DisplayPort USB Type-C Mode BER Compliance Test Setup for DP Sink DUT at TP3_EQ at 10G.....	46
Figure 43. DisplayPort USB Type-C Mode BER Compliance Test Setup for DP Sink DUT at TP3_EQ at 13.5G and 20G.....	48
Figure 44. Standard/Mini DisplayPort Mode BER Compliance Test Setup for DP Sink DUT at TP3_EQ at 10G.....	49
Figure 45. Standard/Mini DisplayPort Mode BER Compliance Test Setup for DP Sink DUT at TP3_EQ at 13.5G and 20G.....	50
Figure 46. Margin Test Configuration	51
Figure 47. Sink Margin Test Selection.....	51
Figure 48. Report Results Page	52
Figure 49. DUT Information.....	53
Figure 50. Results Summary Table Example	54
Figure 51. Calibration/Test Result Details Example.....	55
Figure 52. Delete Individual Calibration/Test Results Example	56
Figure 53. Saving and Loading Calibration and Test Sessions	57
Figure 54. PPG Output Setting.....	59
Figure 55. Pattern Setting	59
Figure 56. PPG Emphasis Setting.....	60
Figure 57. Jitter Source Setting	60
Figure 58. CM Setting.....	61
Figure 59. Keysight Oscilloscope Vertical and Horizontal Setup	62
Figure 60. Emphasis CH1 Interface.....	64
Figure 61. Deemphasis Configuration (1).....	65
Figure 62. Deemphasis Configuration (2)	65
Figure 63. Deemphasis Configuration (3)	66
Figure 64. Results Summary Table Example	66
Figure 65. 10G Preshoot and Deemphasis Preset Calibration Result Diagram Example	67
Figure 66. 13p5G Preshoot and Deemphasis Preset Calibration Result Diagram Example	67
Figure 67. 20G Preshoot and Deemphasis Preset Calibration Result Diagram Example.....	68
Figure 68. Jitter Clock Source Setting.....	69
Figure 69. PPG Misc2 Settings	70
Figure 70. Pattern Setting	71
Figure 71. PPG Emphasis Setting.....	71
Figure 72. SSC Setup.....	72
Figure 73. DATA+ Amplitude Setting	72

Figure 74. CM Setting	73
Figure 75. Oscilloscope Vertical and Horizontal Setup.....	74
Figure 76. Oscilloscope Clock Recovery Setup	75
Figure 77. Oscilloscope Jitter Setup	77
Figure 78. ISI Measurement Preset Table.....	78
Figure 79. 4Tap Emphasis CH1 Interface	79
Figure 80. Optimized Preset (Minimum DDJpp) Measurement On Keysight Scope	80
Figure 81. Optimized Preset (Minimum DDJpp) Measurement On Tektronix Scope	80
Figure 82. Calibration to Phase Match On Keysight Scope	81
Figure 83. Calibration to Phase Match On Tektronix Scope	81
Figure 84. Calibrate ACCM	82
Figure 85. Calibrate ACCM Peak-to-Peak Amplitude	83
Figure 86. Jitter Amplitudes	84
Figure 87. Calibrate RJ Amplitude #1.....	85
Figure 88. Calibrate RJ Amplitude #2 On Keysight Scope	86
Figure 89. Calibrate RJ Amplitude #2 On Tektronix Scope	86
Figure 90. Calibrate SJ Amplitude #1.....	87
Figure 91. Calibrate SJ Amplitude #2 On Keysight Scope	88
Figure 92. Calibrate SJ Amplitude #2 On Tektronix Scope.....	88
Figure 93. TJ Measurement On Keysight Scope.....	89
Figure 94. TJ Measurement On Tektronix Scope.....	90
Figure 95. Eye Amplitude.....	91
Figure 96. Eye Mask On Keysight Scope.....	92
Figure 97. Eye Mask On Tektronix Scope	92
Figure 98. DC Gain Setting.....	94
Figure 99. DFE Setting	95
Figure 100. Eye Amplitude	96
Figure 101. DFE Setting.....	104
Figure 102. Eye Amplitude	105
Figure 103. Eye Amplitude Measurements	106
Figure 104. DC Gain Setting.....	112
Figure 105. DFE Setting.....	113
Figure 106. Eye Amplitude	114
Figure 107. Eye Amplitude Measurements	115
Figure 108. Keysight Connection Expert	117
Figure 109. Oscilloscope's VISA Address	118
Figure 110. OpenChoice Instrument Manager In Start Menu.....	119
Figure 111. OpenChoice Instrument Manager Menu.....	120

List of Tables

Table 1. Equipment Requirements – Systems.....	10
Table 2. Equipment Requirements – Accessories.....	10
Table 3. Equipment Requirements – Connection Cables.....	12
Table 4. Calibration/Test Parameters Description	26
Table 5. Keysight Oscilloscope Vertical and Horizontal Setup.....	61
Table 6. Tektronix Oscilloscope Setup	62
Table 7. Keysight or Tektronix Oscilloscope Histogram Setup.....	63
Table 8. Deemphasis Configuration.....	64
Table 9. Oscilloscope Vertical and Horizontal Setup.....	74
Table 10. Oscilloscope Clock Recovery Setup	75
Table 11. Oscilloscope ACCM Setup.....	76
Table 12. Oscilloscope Jitter Setup	76
Table 13. Oscilloscope Eye Diagram Vertical Setup.....	78
Table 14. DC Gain Settings	93
Table 15. Oscilloscope Vertical and Horizontal Setup	98
Table 16. Oscilloscope Clock Recovery Setup	99
Table 17. Oscilloscope ACCM Setup	99
Table 18. Oscilloscope Jitter Setup.....	99
Table 19. Oscilloscope Eye Diagram Vertical Setup	100
Table 20. DC Gain Settings.....	102
Table 21. Oscilloscope Vertical and Horizontal Setup	107
Table 22. Oscilloscope Clock Recovery Setup.....	108
Table 23. Oscilloscope ACCM Setup.....	108
Table 24. Oscilloscope Jitter Setup	108
Table 25. Oscilloscope Eye Diagram Vertical Setup.....	109
Table 26. DC Gain Settings.....	111

1 Introduction

[Note:

For UHBRx (originally the DP2.1)

UHBRx stands for UHBR20(20G bps), UHBR13.5(13.5G bps), UHBR10(10G bps)]

This User Guide & MOI describes the procedures to perform DisplayPort 2.1 PHY CTS UHBRx Sink (or Receiver) calibration and tests of the VESA DisplayPort Logo Compliance Program using the Anritsu MP1900A BERT and High Performance Real-Time Oscilloscopes in conformance with the DisplayPort 2.1 PHY Compliance Test Specification (CTS). Sink tests are required to qualify a Sink product or silicon building block for Logo certification and listing on the DP Integrators List.

This User Guide & MOI explains how to set up and use the GRL-DP21-SINK-AN software to automate receiver calibration and compliance testing for DisplayPort 2.1 PHY CTS UHBRx Sink conformance. The GRL-DP21-SINK-AN software is used with the Anritsu MP1900A BERT for testing DisplayPort 2.1 UHBRx receivers per the Jitter Tolerance requirements of the DisplayPort 2.1 PHY CTS and DisplayPort over USB Type-C® CTS respectively.

The GRL-DP21-SINK-AN software automates stressed signal calibration and jitter tolerance testing at the following DisplayPort data rates– UHBR10 (10.0 Gbit/s per lane), UHBR13.5 (13.5 Gbit/s per lane) & UHBR20 (20.0 Gbit/s per lane) and supports USB Type-C and standard DisplayPort sink device-under-tests (DUT's). For link training, compliance, and margin testing through DPCD registers, the software provides automation control using a compatible DisplayPort AUX controller.

The following are the main topics covered by this User Guide & MOI:

1. Equipment required for calibration and testing.
2. GRL-DP21-SINK-AN software setup for calibration and test automation.
3. Manual DisplayPort 2.1 PHY CTS UHBRx Sink calibration and test methodology.

2 Resource Requirements

2.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS – SYSTEMS

System	Qty.	Description	Key Specification Requirement
GRL-DP21-SINK-AN	1	GRL Platform Solutions DisplayPort 2.1 PHY CTS UHBRx Sink Compliance Calibration & Test Automation Software for the Anritsu MP1900A BERT – www.grlps.com (Support → Download Center) – with Node Locked License to single Oscilloscope/PC OS	
Anritsu MP1900A BERT	1	MP1900A Signal Quality Analyzer, with following modules: - MU181000A/B 12.5 GHz Synthesizer - MU181500B Jitter Modulation Source - MU195020A 21G/32G bit/s SI Pulse Pattern Generator - MU195050A Noise Generator	- Option STR for stress generation - Proper test patterns ^[a]
Real-time Oscilloscope ^[b]	1	Keysight (InfiniiSim / EZ-JIT / Serial Data Analysis / Serial Data Equalization) Oscilloscope Or Tektronix DPO/MSO70000DX or 70000SX Series Oscilloscope with DPOJET (Jitter and Eye Analysis) software	> 16 GHz bandwidth ^[c]

^[a] MP1900A DisplayPort patterns are distributed with GRL-DP21-SINK-AN software and are installed during installation process.

^[b] Infiniium / DPOJET setup files and SDLA filters are distributed with the GRL-DP21-SINK-AN software and are installed during installation process.

^[c] For UHBR13.5 / UHBR20 data rates, at least 21 GHz of oscilloscope bandwidth is required.

TABLE 2. EQUIPMENT REQUIREMENTS – ACCESSORIES

Accessory	Qty.	Description	Key Specification Requirement
TP1 Plug Test Fixture	1	Test Point 1 Full Size/Enhanced DisplayPort Plug Test Fixture	Luxshare-ICT TFDP-V22PA
	1	Test Point 1 DisplayPort USB Type-C Plug Test Fixture	Wilder DPC-TPA-P, 640-0800-000 Or Luxshare-ICT LL-USBC-TPA-8P
	1	Test Point 1 Standard/Mini DisplayPort Plug Test Fixture	Wilder ENH-DP-TPA-V2.1-B-P, 640-1052-000 Or Wilder ENH-MDP-TPA-V2.1-B-P, 640-1045-000 Or Luxshare-ICT TFDP-m21PA

Accessory	Qty.	Description	Key Specification Requirement
TP3 Channel Components	2	Test Point 3 Full Size/Enhanced DisplayPort Receptacle Test Fixture	Luxshare-ICT TFDP-V22RA
	2	Test Point 3 DisplayPort USB Type-C Receptacle Test Fixture	Wilder DPC-TPA-R, 640-0801-000 Or Luxshare-ICT LL-USBC-TPA-8R
	2	Test Point 3 Standard/Mini DisplayPort Receptacle Test Fixture	Wilder ENH-DP-TPA-V2.1-B-R, 640-1053-000 Or Wilder ENH-MDP-TPA-V2.1-B-R, 640-1046-000 Or Luxshare-ICT TFDP-m21RA
TP3 Fixed ISI Trace	1	Test Point 3 Fixed ISI Board	Wild River Technology ISI-USB4 Loss Modeling Platform Set
TP3 Test Cables	1	2 m USB Type-C Cable	Insertion Loss -11.5 dB at 5 GHz
	1	0.8 m USB Type-C Cable	Insertion Loss -6.2 dB at 6.75 GHz
	1	0.8 m USB Type-C Cable	Insertion Loss -7.5 dB at 10 GHz
	1	2 m Standard/Mini DisplayPort Cable	Insertion Loss -8.5 dB at 5 GHz
	1	0.8 m Standard/Mini DisplayPort Cable	Insertion Loss -9.8 dB at 6.75 GHz
	1	0.8 m Standard/Mini DisplayPort Cable	Insertion Loss -7.5 dB at 10 GHz
DisplayPort Control Board	1	DisplayPort USB Type-C Mode Control Board	Wilder DPC-TPA-CB, 640-0802-000
DisplayPort AUX Controller	1	Compatible vendor specific AUX controller	For link training and error detection
RF Signal Generator	1	As external crosstalk source	Rigol DSG3000B Series recommended
Cable Deskew Fixture	1	Anritsu Splitter	K241B
DC Block	2		Bandwidth of at least 33 GHz
÷4 RF Splitter	2	Anritsu AN44182A 4-Way Power Divider or equivalent	
Computer	1	Laptop or Desktop PC	Windows 7+ OS For automation control (running GRL-DP21-SINK-AN software)

Note: Cable connector type and length requirements may vary according to the lab setup and the dimensions of the DUT board. Table below is a recommended list. Please also refer to the respective manufacturer for detailed cabling recommendations related to DisplayPort 2.1.

TABLE 3. EQUIPMENT REQUIREMENTS – CONNECTION CABLES

Connection Cable	Qty.	Key Specification Requirement
MU181000A/B to MU181500B	1	Anritsu J1624A SMA-SMA cable (0.3 m)
MU181500B to MU195020A	1	Anritsu J1624A SMA-SMA cable (0.3 m)
MU195020A to MU195050A	1 pair	Anritsu J1746A K-K skew matched pair short semirigid cable
Matched Cable Pairs	6	Phase Matched $\pm 5^\circ$ at 40 GHz Insertion Loss 1 dB maximum in 10 GHz
RPC-2.92 Jack to SMP Jack	4	Rosenberger 02K119-K00E3
JTAG Ribbon Cable	1	For connecting AUX controller and test fixture

2.2 Software Requirements

Software	Source
VISA (Virtual Instrument Software Architecture) API Software	VISA Software is required to be installed on the control PC running GRL-DP21-SINK-AN software. GRL Platform Solutions' software framework has been tested to work with all three versions of VISA available on the Market: 1. NI-VISA: http://www.ni.com/download/ni-visa-17.0/6646/en/ 2. Keysight IO Libraries: www.keysight.com (Search on IO Libraries) 3. Tektronix TekVISA: www.tek.com (Downloads > Software > TekVisa)
MX190000A	Anritsu High-Speed Serial Data Test Software – Mainframe MX190000A SQA Control Software (Version 4.00.00 or above). This software is located on the BERT.

3 Installing and Setting Up GRL-DP21-SINK-AN Software

This section provides the procedure for installing, configuring and verifying the operation of the GRL-DP21-SINK-AN software. It also helps you familiarize yourself with the basic operation of the software.

The software installer automatically creates shortcuts in the Desktop and Start Menu. To open the software application, follow the procedure in the following section.

3.1 Download and Set Up GRL-DP21-SINK-AN Software

Install, launch and set up the GRL-DP21-SINK-AN software on a PC or an oscilloscope (where GRL-DP21-SINK-AN is referred to as ‘Control PC’ or ‘Scope’ respectively in this MOI & User Guide):

1. Install VISA (Virtual Instrument Software Architecture) on to the PC/Scope where GRL-DP21-SINK-AN is to be used (see Section 2.1).
2. Download the GRL-DP21-SINK-AN ZIP file package from the GRL Platform Solutions support site.
3. The ZIP file contains:
 - a) **DPSink21_ANPatternFilesInstallationxxxxxxxxSetup** – Run this on the Anritsu MP1900A BERT to install the DisplayPort 2.1 test pattern setup files. This will place the DisplayPort Configuration and Pattern files on the MP1900A BERT in the ‘C:\Configurations\Anritsu DisplayPort Sink Test 2.1’ directory hierarchy.
 - b) **DPSinkTest21_ANApplicationxxxxxxxxSetup** – Run this on the Control PC or Oscilloscope to install the GRL-DP21-SINK-AN application. This application will create the ‘C:\GRL\Rx Test Solution\Applications\DPSinkTest20_AN’ directory hierarchy.
 - c) **DPSinkTest21_ANScopeSetupFilesInstallationxxxxxxxxSetup** – Run this on the Oscilloscope to install the Infiniium setup files. This will place the DisplayPort Setup and Filter folders in the ‘C:\GRL\Agilent\Setup\Anritsu DisplayPort Sink Test 2.1’ of the Keysight Scope or C:\TekApplications\DPOJET of the Tektronix Scope directory hierarchy.

3.1.1 On the Anritsu MP1900A BERT

1. Launch the Signal Quality Analyzer-R Control Software.
2. Select the “Expert BERT” button to turn on the Miscellaneous System. This will allow you to remotely control the MP1900A BERT.

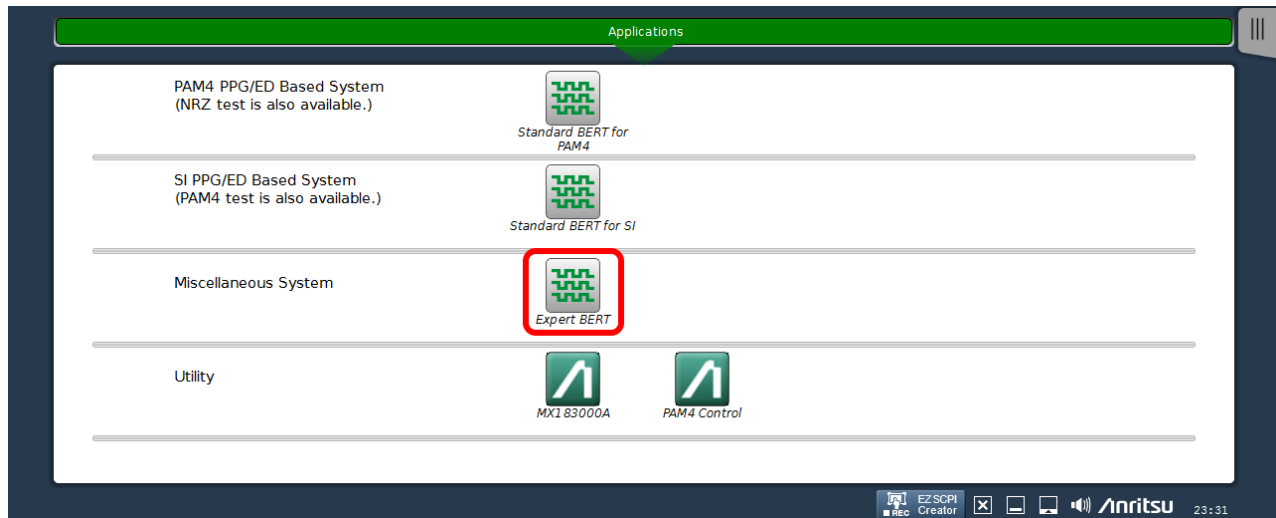


FIGURE 1. TURN ON MISCELLANEOUS SYSTEM

- Note the IP Address as it will be used to connect the MP1900A BERT with the GRL-DP21-SINK-AN software.

3.1.2 On the PC Used for GRL Platform Solutions Framework Installation

- Open the GRL folder from the Windows Start menu. Click on **GRL – Automated Test Solutions** within the GRL folder to launch the GRL Platform Solutions software framework.

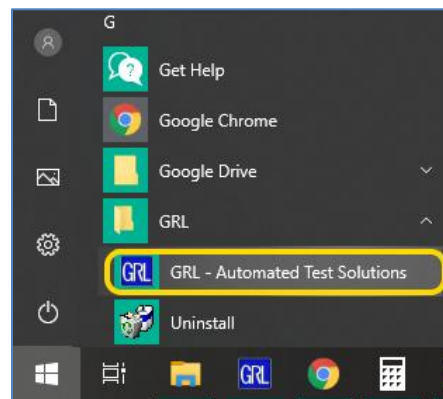


FIGURE 2. SELECT AND LAUNCH GRL PLATFORM SOLUTIONS FRAMEWORK

- From the **Application → Rx Test Solution** drop-down menu, select **Anritsu DisplayPort Sink Test 2.1** to start the application. If the selection is grayed out, it means that your license has expired.

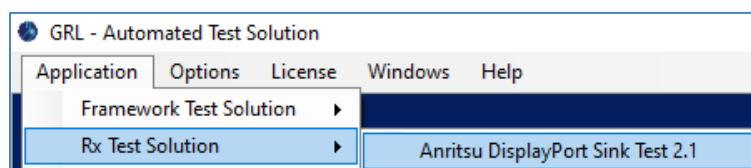


FIGURE 3. START DISPLAYPORT SINK TEST 2.1 APPLICATION

3. To enable license, go to License → License Info.

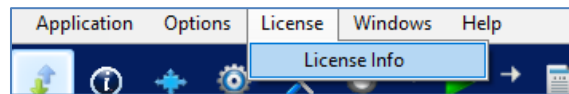


FIGURE 4. SEE LICENSE DETAILS

a) Check the license status for the installed application.

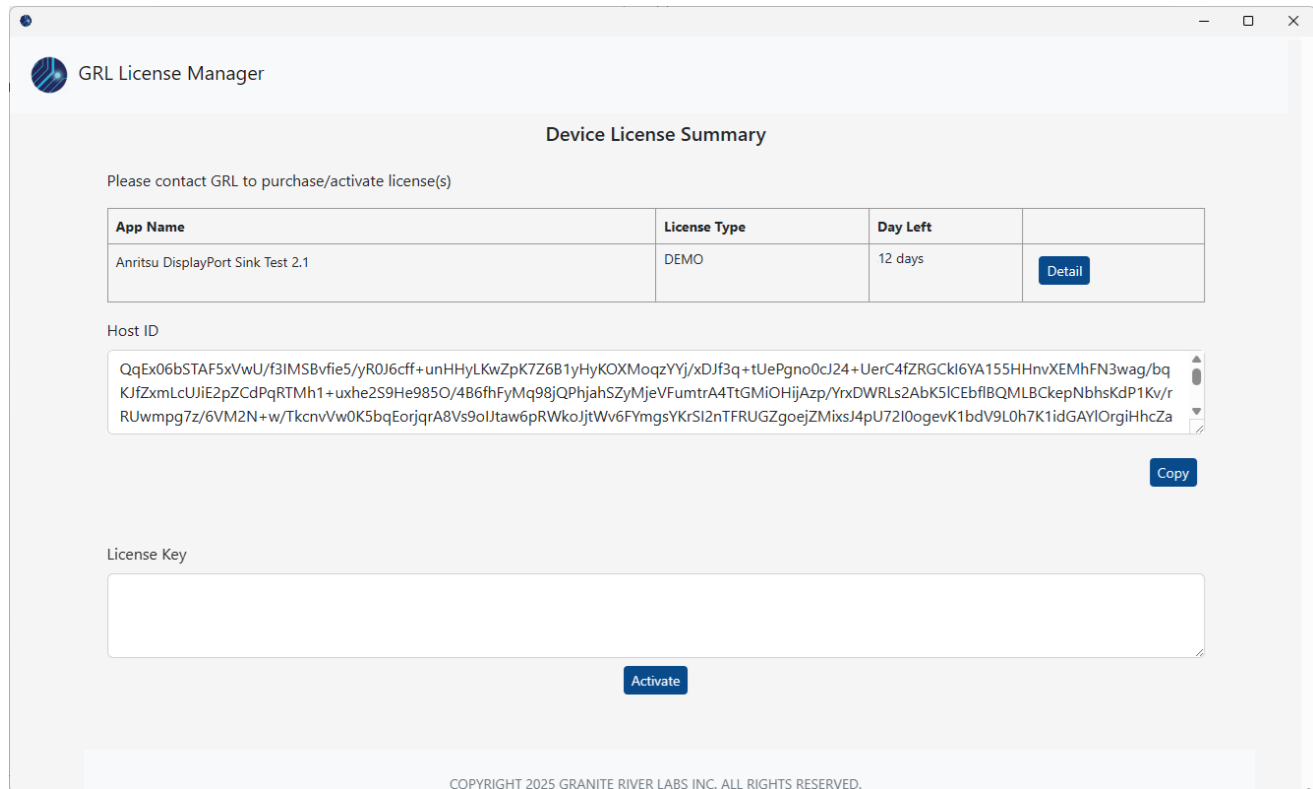


FIGURE 5. CHECK LICENSE FOR INSTALLED APPLICATION

4. Activate License:

- If you have an Activation Key, enter it in the **License Key** field provided and select **Activate**. The installed application is ready for use upon successful activation.
- If you do not have an Activation Key, close the above window to use a demo version of the application over a free 12-day trial period.

Note: Once the 12-day trial period ends, you will need to request an Activation Key to continue using the application on the same computer by contacting support@grlps.com.

- Select the Equipment Setup icon  on the DisplayPort Sink Test 2.1 Application menu.
- Connect the Anritsu MP1900A BERT via LAN to the GRL Platform Solutions automation control enabled Scope or PC. Enter the MP1900A IP address and Port number to match what is shown in the MP1900A *Remote Client* window in Section 3.1.1. For example, the BERT can be connected using a connection string in the following format: "TCPIP0::192.168.0.14::5001::SOCKET" or "192.168.0.14:5001". Note the IP address

listed is only example and should be changed according to the actual network connection being used.

7. On the Scope or control PC, obtain the network addresses for all the connected instruments from the device settings. Note these addresses as they will be used to connect the instruments to the GRL Platform Solutions automation software.

(Note: The Scope IP address can be obtained, if not known, by typing CMD → IPCONFIG on the Scope and observe the IP address listed. If the GRL Platform Solutions software is installed on the **Tektronix Scope**, ensure the Scope is connected via GPIB and type in the GPIB network address, for example “GPIB8::1::INSTR”). If the GRL Platform Solutions software is installed on the PC to control the Scope, type in the Scope IP address, for example “TCPIP0::192.168.0.110::inst0::INSTR”. Note to **omit** the Port number from the address.)

8. Then select the “lightning” button () for each connected instrument.

The “lightning” button should turn green () once the GRL Platform Solutions software has successfully established connection with each instrument.

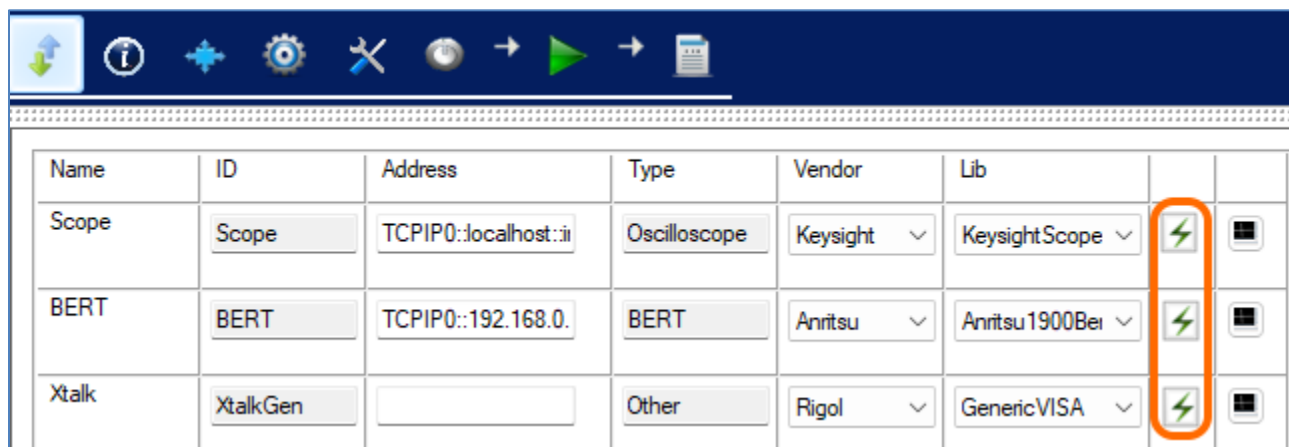


FIGURE 6. CONNECT INSTRUMENTS WITH GRL PLATFORM SOLUTIONS SOFTWARE

Note: Further information for connecting the Keysight and Tektronix oscilloscopes to the PC is provided in the Appendix of this document.

3.1.3 Set Up Remote File Server

1. The **GRLRemoteProxyServer.exe** will also be installed along with the **DPSinkTest21_ANScopeSetupFilesInstallationxxxxxxxxSetup** on the Scope. The GRLRemoteProxyServer.exe is installed under the “C:\GRL\GRLRemoteProxyServer” directory.

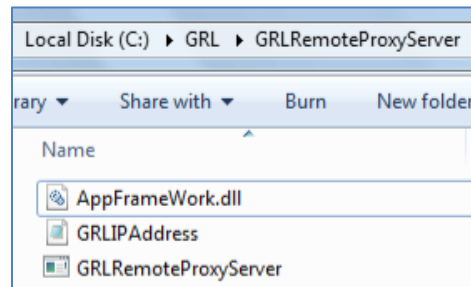


FIGURE 7. INSTALLED GRLREMOTEPROXYSERVER.EXE FILE DIRECTORY

2. If the GRL Platform Solutions software is installed on the PC to control the Scope and SigTest is selected as the calibration method to be used (refer Section 3.4), the GRLRemoteProxyServer.exe must be run on the Scope to move large waveform files back to the control PC. The GRL Platform Solutions software will then perform post-processing and analysis of these waveforms using SigTest.
3. When running the GRLRemoteProxyServer.exe, make sure that the control PC and Scope are connected to the same network, using IP addresses as in following example:
 - Control PC IP address: 192.168.100.8
 - Scope IP address: 192.168.100.35

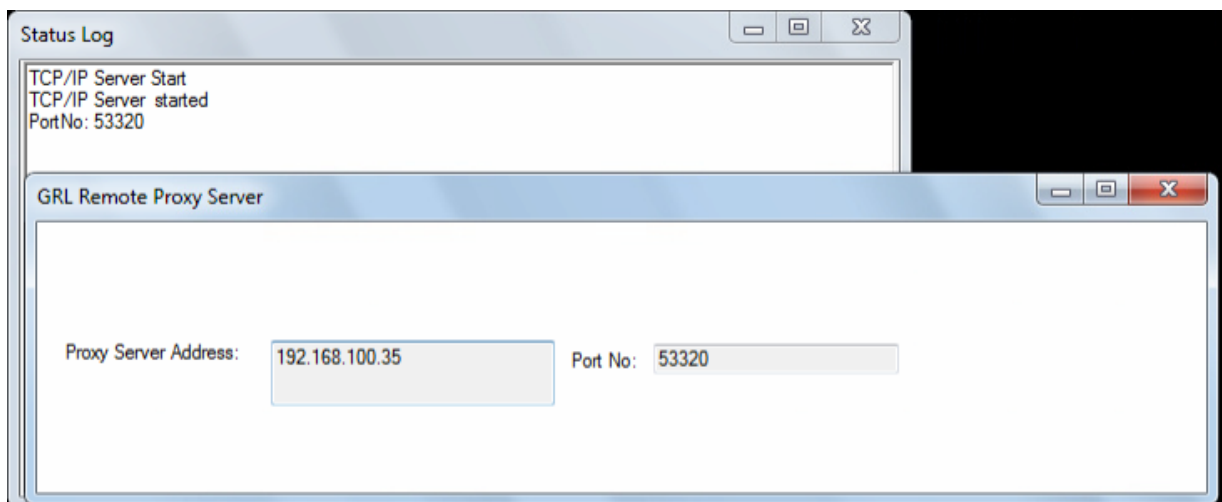


FIGURE 8. VERIFY PROXY SERVER CONNECTION FOR CONTROL PC AND SCOPE

4. On the GRL-DP21-SINK-AN application, configure the “Remote File Server IP Address” and “Remote File Server Port No” parameters on the Configurations  page to match the network settings of the Remote Proxy Server as shown in the example below:

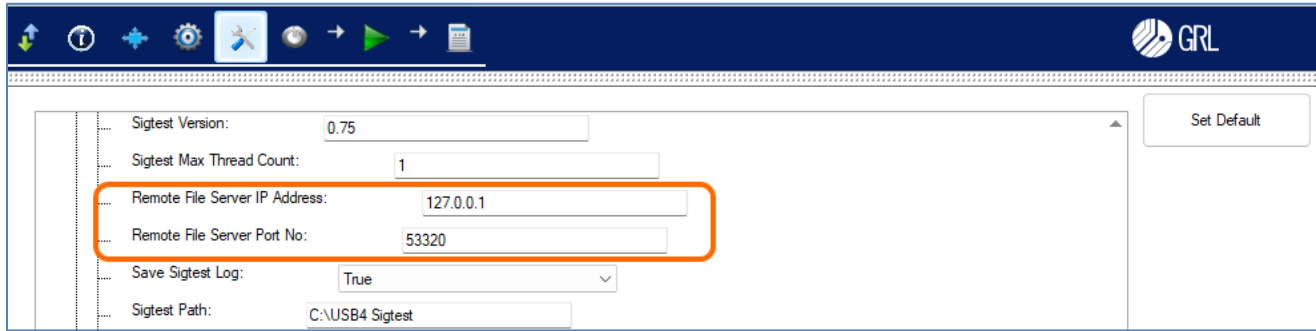


FIGURE 9. CONFIGURE REMOTE PROXY SERVER NETWORK SETTINGS ON GRL PLATFORM SOLUTIONS SOFTWARE

Refer Section 3.4 for more details on parameters available on the Configurations page.

3.2 Configure the GRL-DP21-SINK-AN Software Before Calibration and Testing

3.2.1 Enter Calibration/Test Session Information

Select  from the menu to access the **Session Info** page. Enter the information as required for the test session that is currently being run. The information provided will be included in the test report generated by the software once tests are completed.

- The fields under **DUT Info** and **Test Info** are defined by the user.
- The **Software Info** field is automatically populated by the software.

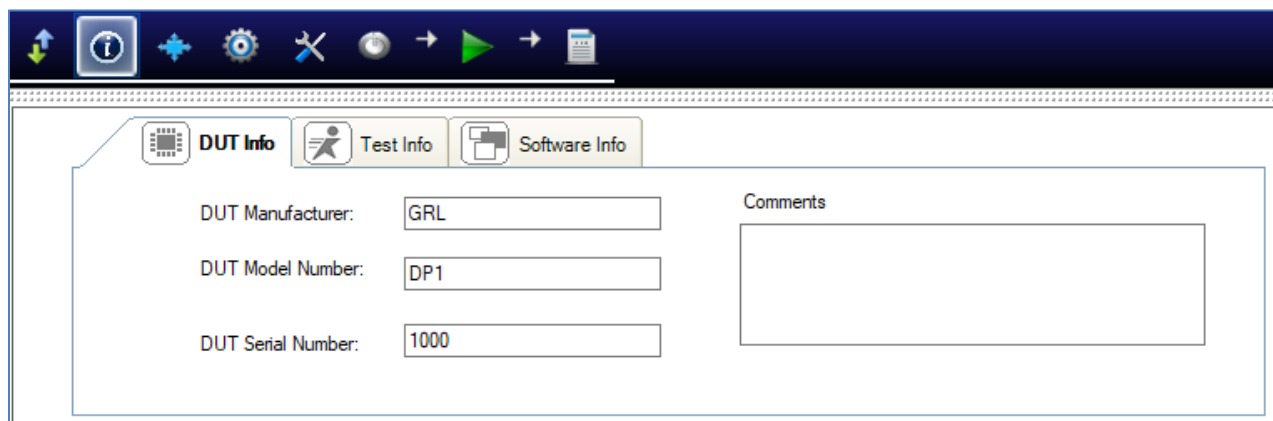


FIGURE 10. SESSION INFO PAGE

3.2.2 Set Up Conditions for Calibration/Testing

Select  from the menu to access the **Conditions** page to set the conditions for calibration and testing.

Recommended procedure:

- *Step 1:* When calibrating, select the desired conditions and perform the calibration tests.
 - *Step 2:* When ready for testing, re-select the desired test conditions. For example, if required to test only one Lane at one SJ Frequency for the UHBR10 Data Rate, then select the appropriate conditions for testing.
- a) **Lane tab:** Select the desired Lanes for testing. *[Note: This is only applicable for DUT compliance test and NOT for calibration.]*

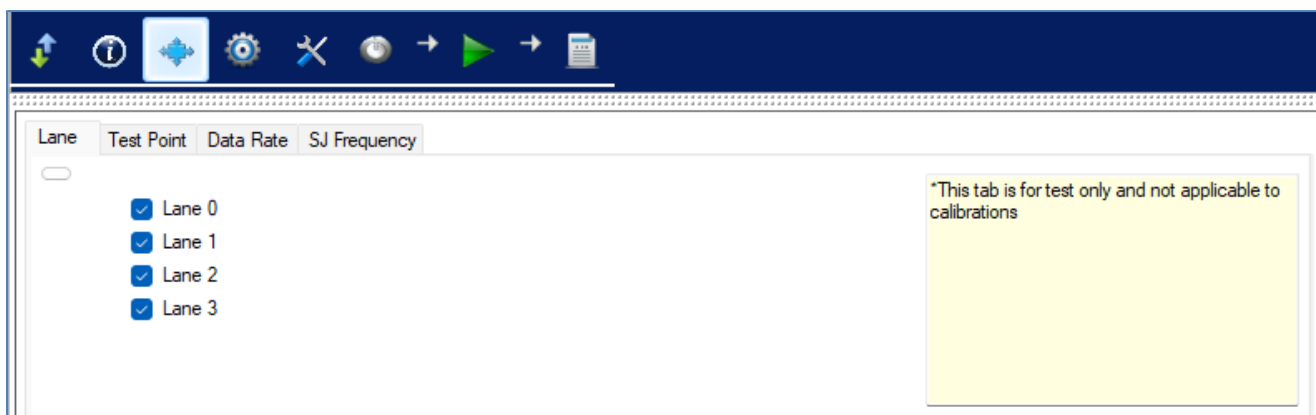


FIGURE 11. SELECT LANE UNDER TESTS

- b) **Test Point tab:** Select the test points for calibration and testing. *[Note: TP1 calibration (Total Jitter & Eye Height) must be performed first prior to TP3_EQ calibration (Optimized EQ Lookup, Eye Height & Eye Width).]*

The following flowchart provides a clearer view of the test conditions:

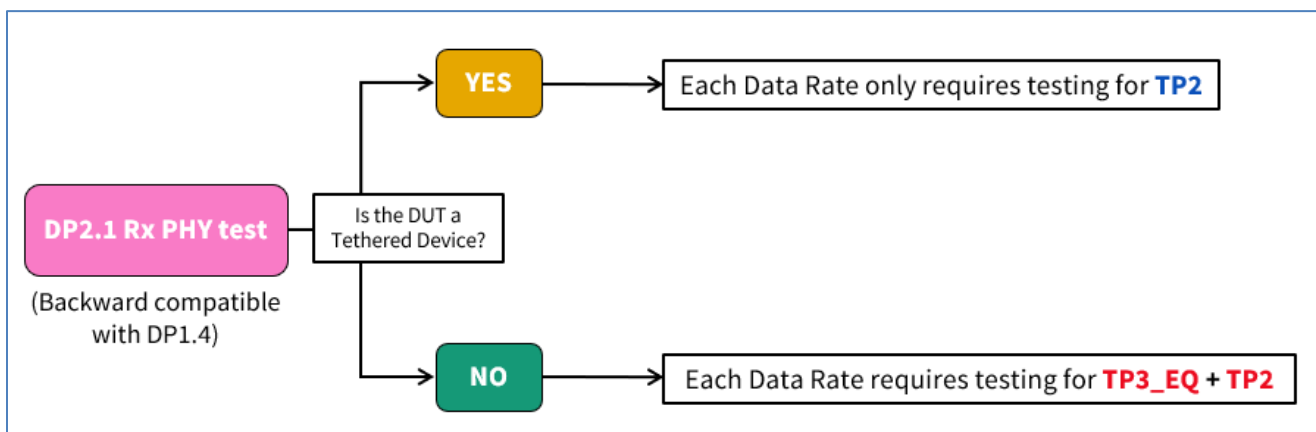


FIGURE 12. COMPLIANCE TEST CONDITIONS

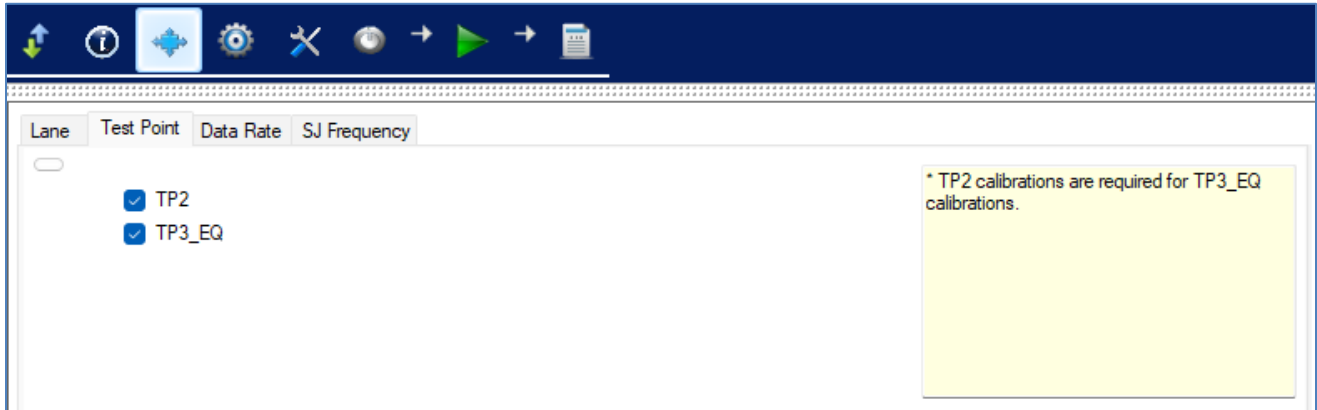


FIGURE 13. SELECT TEST POINTS

c) **Data Rate** tab: Select the desired data rates for calibration or testing:

- UHBR10 (10.0 Gbit/s per lane)
- UHBR13.5 (13.5 Gbit/s per lane)
- UHBR20 (20.0 Gbit/s per lane)

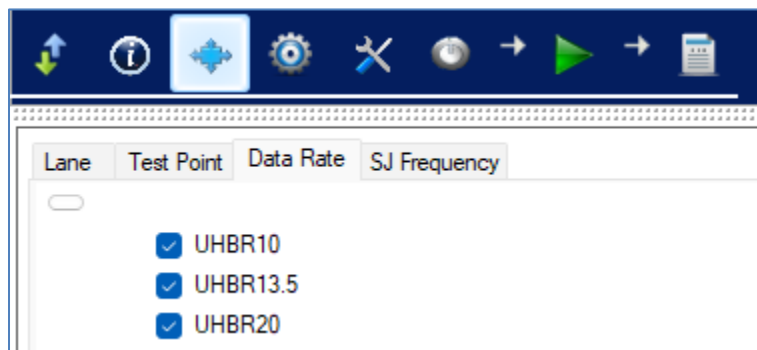


FIGURE 14. SELECT DATA RATES

d) **SJ Frequency** tab: Select the desired SJ frequencies for calibration or testing.

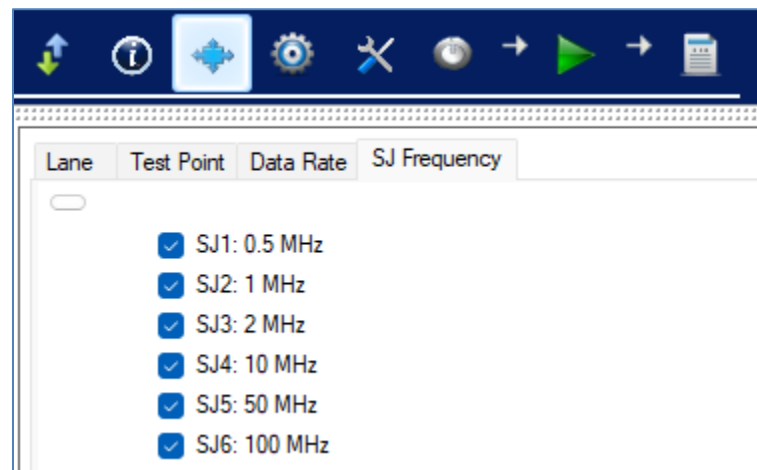


FIGURE 15. SELECT SJ FREQUENCIES

3.2.3 Set Up AUX Controller for DUT Test Automation

Select  from the menu to access the Setup Configuration page.

Select to use a supported AUX Controller in the test setup or select 'None' if not using an AUX Controller. Then enter the COM port number of the connected AUX controller.

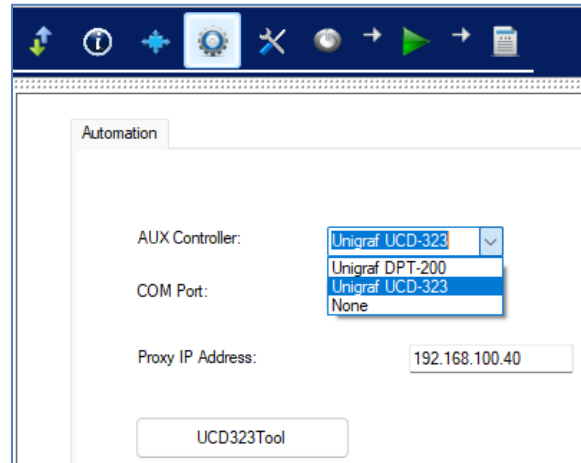


FIGURE 16. SELECT AUX CONTROLLER

If the Unigraf UCD-323 AUX controller is selected, the GRL-DP21-SINK-AN software allows the user to perform data read/write operations via the 'UCD323 DP Source Console'. *Note: This feature is available only after successful initialization and connection to the Unigraf UCD-323 AUX controller.*

Connect the Unigraf UCD-323 AUX controller to the target equipment (such as the Anritsu MP1900A BERT) via USB. The equipment must have its proxy server enabled, and the equipment's IP address should be entered in the "Proxy IP Address" field on the Setup Configuration page. Then click on the "UCD323 Tool" button. The IP address will be automatically populated in the UCD323 DP Source Console as shown in the example below:

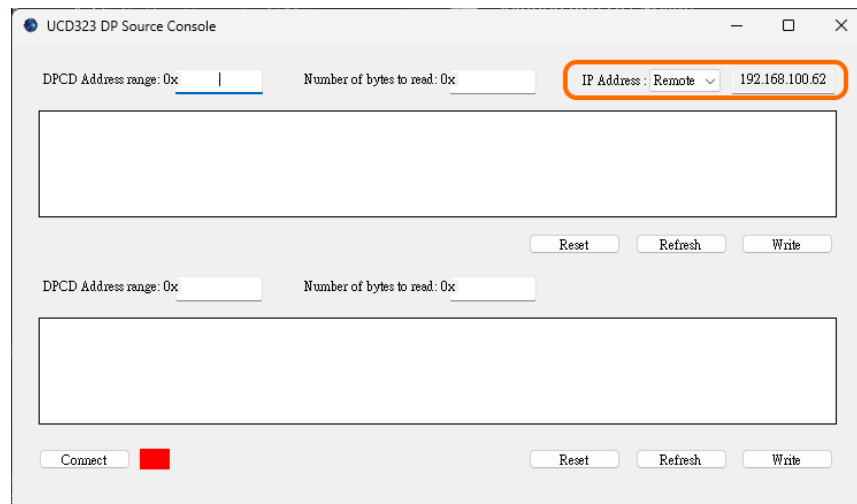


FIGURE 17. UCD323 DP SOURCE CONSOLE— #1

If initialization and connection to the Unigraf UCD-323 AUX controller have not been performed, the “Connect” button will appear red. The button will turn green once initialization is complete and the connection to the Unigraf UCD-323 AUX controller is established as shown in the example below:

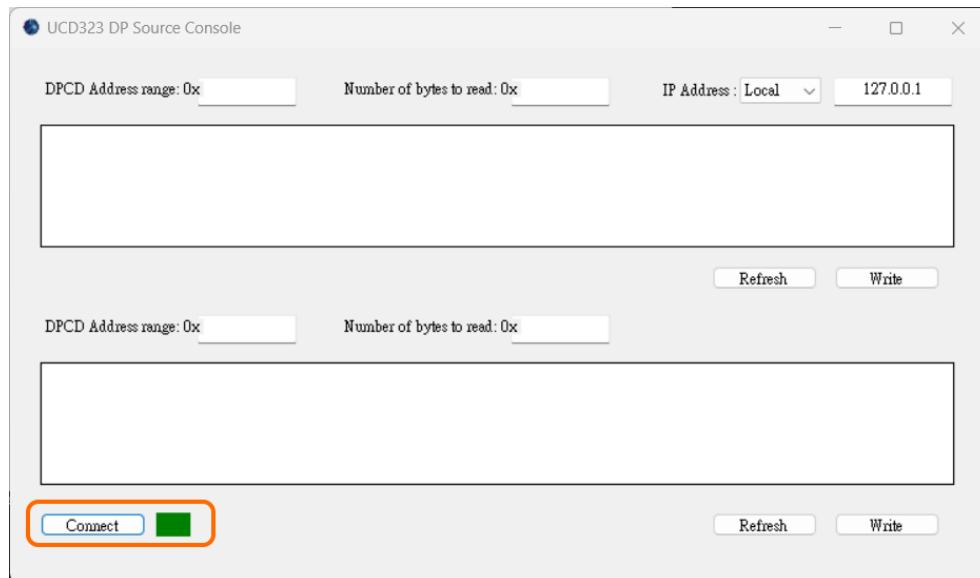


FIGURE 18. UCD323 DP SOURCE CONSOLE— #2

The “IP Address” field can be set to either “Local” or “Remote”. When Local mode is selected, the “IP Address” field will automatically populate with “127.0.0.1”.

To perform manual data read operations, enter the starting address and the number of bytes to read. Click on the “Refresh” button for the application to retrieve the data from the specified address range and display the corresponding values.

Click on the “Write” button for the application to write the specified values into the corresponding byte locations. See example below:

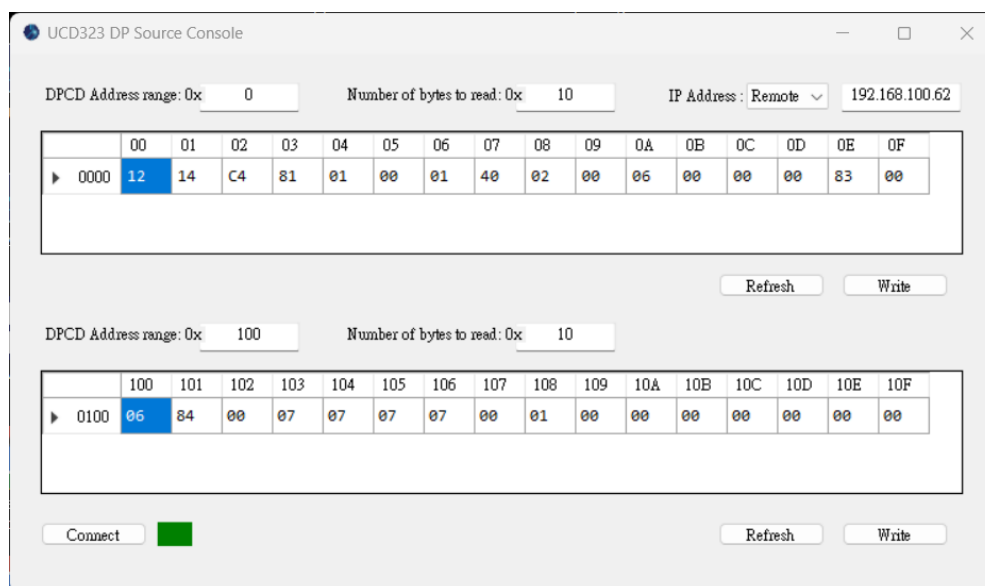


FIGURE 19. UCD323 DP SOURCE CONSOLE— #3

Note:

When the control PC detects the Unigraf UCD-323 Aux Controller, it should appear in the “Devices” list as shown in the example below. If it does not show up, select “Rescan” to search again.

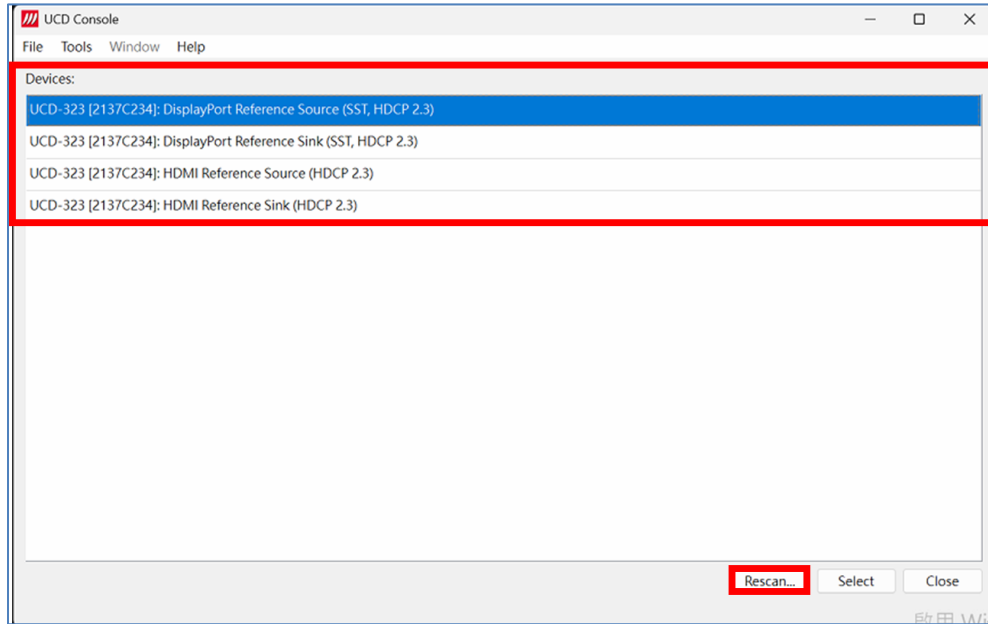


FIGURE 20. DETECT UNIGRAF UCD-323 AUX CONTROLLER IN CONTROL PC

To verify whether the Unigraf UCD-323 Aux Controller has the required license installed, follow these steps:

1. Open “License Manager” and go to “UCD License”.

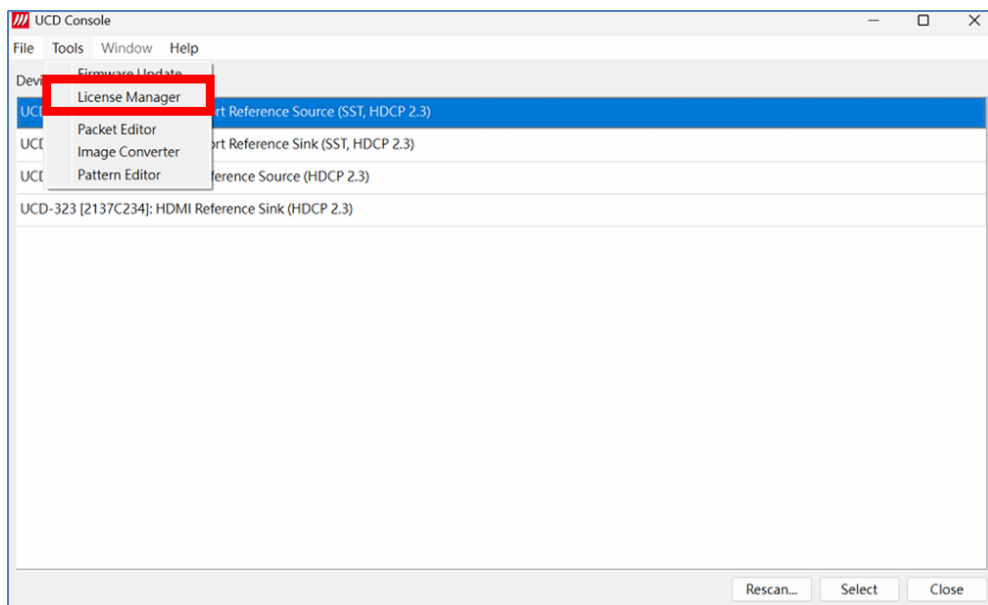


FIGURE 21. OPEN LICENSE MANAGER

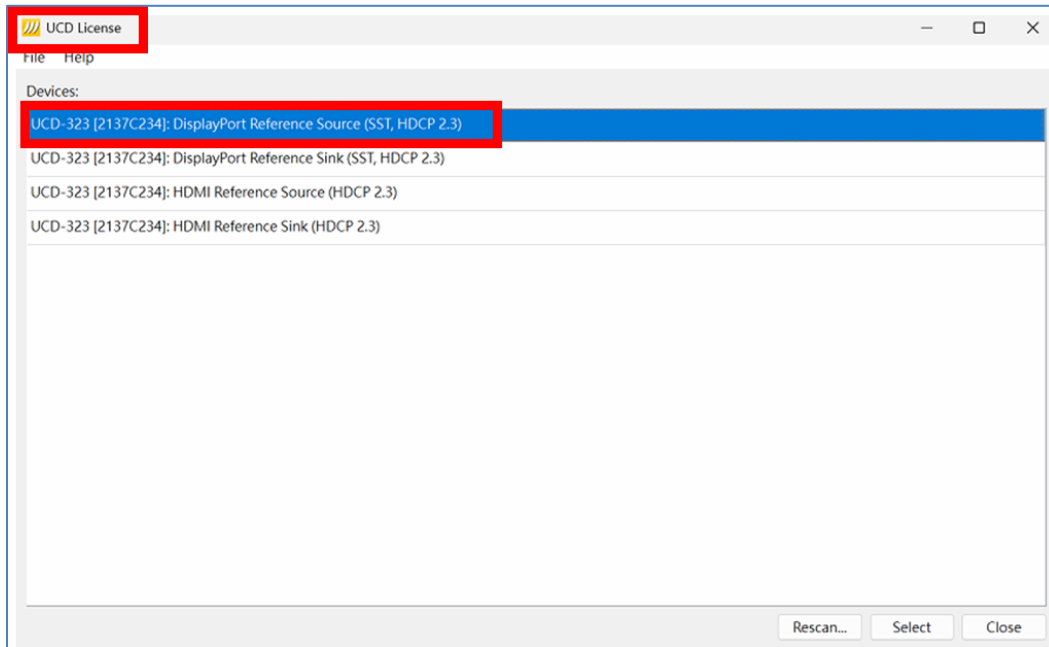


FIGURE 22. UCD LICENSE SCREEN

2. For Rx testing, the Unigraf UCD-323 Aux Controller requires the DisplayPort Reference Source License.
3. Enter the serial number of the Unigraf UCD-323 Aux Controller and click “Install”.

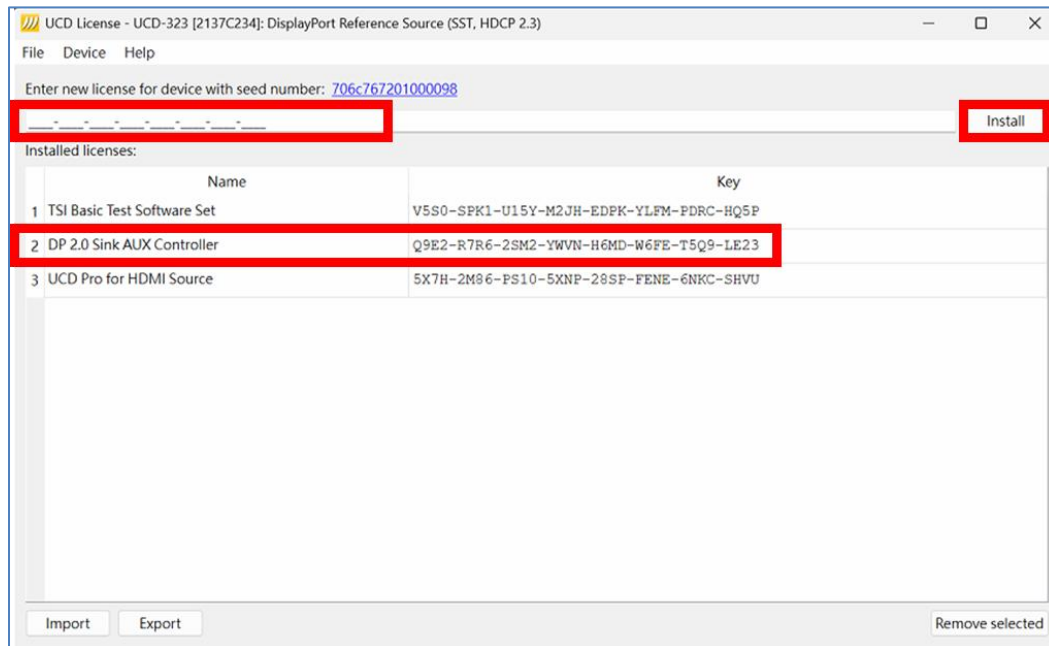


FIGURE 23. INSTALL DISPLAYPORT REFERENCE SOURCE LICENSE

4. After installation, the serial number will appear in the list.

3.3 Select Calibration/Test

Go to the **Select Tests** page on the left of the screen to select the available calibration or tests to be performed. Select the check box(s) of the desired calibration/test.

Initially, when starting for the first time or changing anything in the setup, it is suggested to run Calibration first. If the calibration is not completed, the Sink Tests will show an error message.

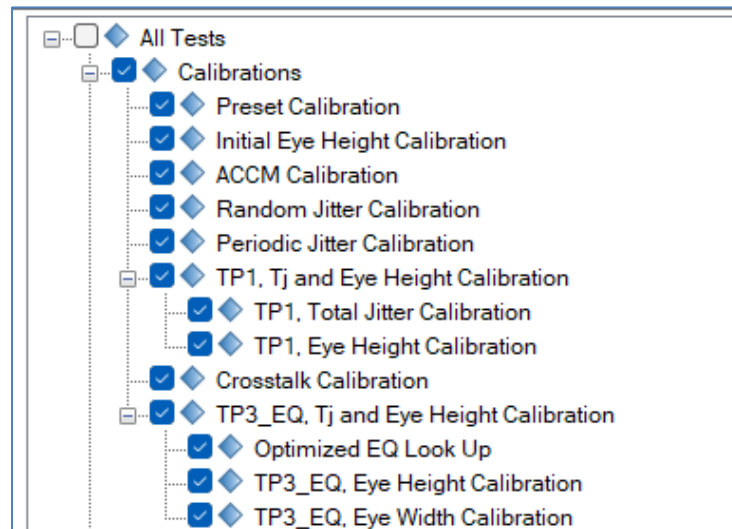


FIGURE 24. CALIBRATION SELECTION

Select the calibration groups to perform calibration for all DisplayPort Sink parameters. Note that while the user can select individual calibration parameters, it is possible that a particular calibration may require the previous calibration to be completed before it can proceed. Thus, it is advisable to complete all previous calibration before going on to the next calibration.

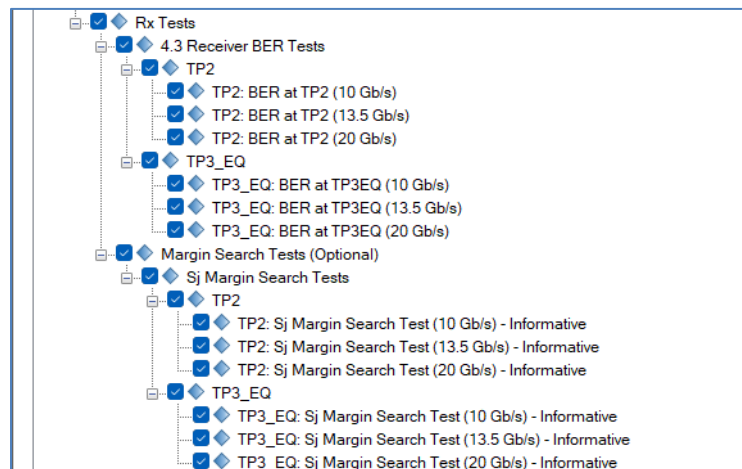


FIGURE 25. TESTS SELECTION

Select the test groups to perform DUT compliance tests for all DisplayPort Sink parameters.

3.4 Configure Calibration/Test Parameters

After selecting the desired calibration or test, select  from the menu to access the Configurations page. Set the required parameters for Sink calibration and testing as described in Table 4 below.

To return all parameters to their default values, select the ‘Set Default’ button.

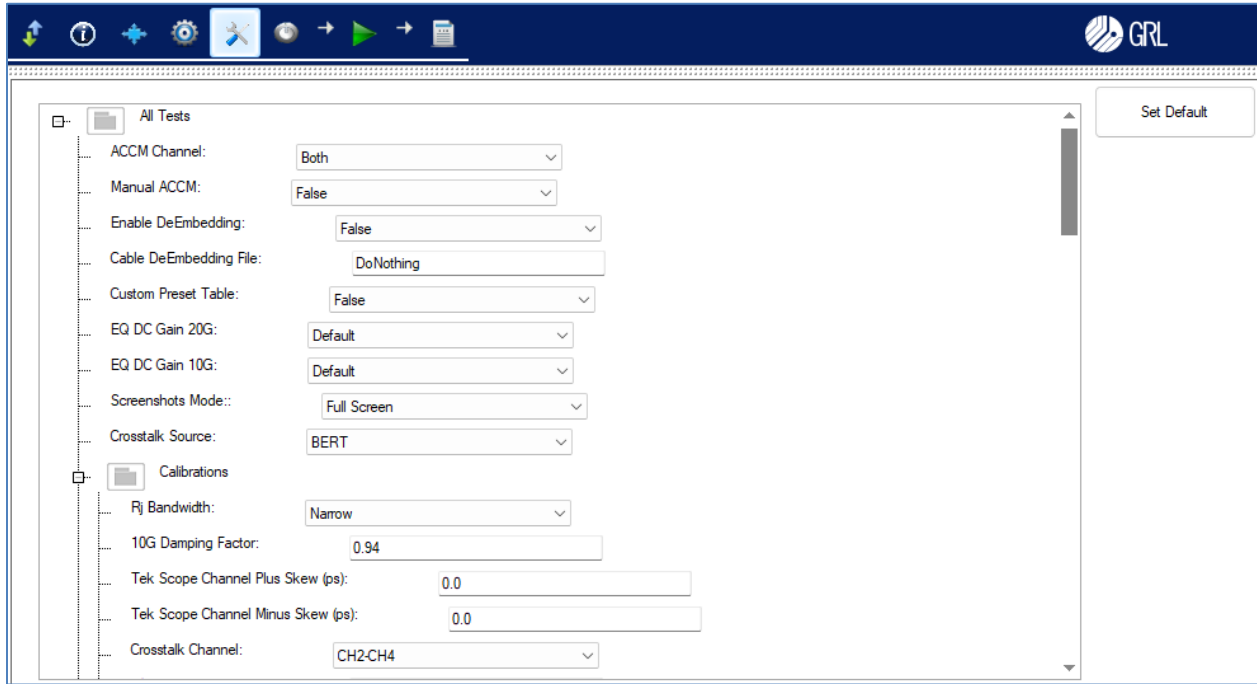
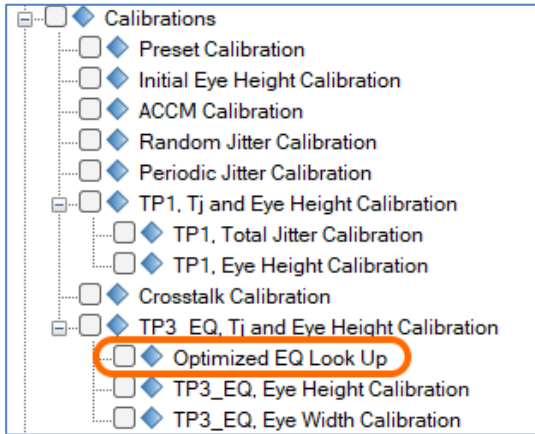


FIGURE 26. PARAMETERS CONFIGURATION PAGE

TABLE 4. CALIBRATION/TEST PARAMETERS DESCRIPTION

Parameter Name	Description
ACCM Channel	Select “Both” or single channel (splitter required) as the AC Common Mode (ACCM) source if used.
Manual ACCM	Set to “True” to manually set the ACCM source or “False” to apply calibrated values from ACCM calibration.
Enable DeEmbedding	Set to “True” to de-embed cable while calibrating.
Cable DeEmbedding File	Define the cable transfer function file. Applicable only when the “Enable DeEmbedding” field is set to “True”.
Custom Preset Table	Set to “True” to use the list of user-defined measurement preset values for calibration.
EQ DC Gain (20G & 10G)	Select the DC Gain setting index for the 10G and 20G TP3_EQ systems.
Screenshots Mode	Select the type of screenshots to be captured when saving test results to a test report: “Full Screen”: Image of the waveform along with the

	measurement area. “Grid”: Image of only the waveform without showing the measurement area.
Crosstalk Source	Select to use the MP1900A “BERT”, “Rigol” RF Signal Generator or an “External” source to generate crosstalk.
Rj Bandwidth	Select to use “Narrow” or “Wide” band for jitter decomposition algorithm to separate random jitter.
10G Damping Factor	For UHBR10, define the 10G damping factor rate to be applied in calibration.
Tek Scope Channel Plus Skew (ps)	If using the Tektronix scope, set the scope channel 1 deskew value.
Tek Scope Channel Minus Skew (ps)	If using the Tektronix scope, set the scope channel 3 deskew value.
Crosstalk Channel	Select the scope channel pair for crosstalk signal input.
20G Damping Factor	For UHBR20, define the 20G damping factor rate to be applied in calibration.
Tj Adjust Param (<100MHz) & (100MHz)	Select whether to use “Rj” or “Sj” for total jitter calibration for both <100 MHz and 100 MHz cases.
Eye Height Acquisition	Enter the number of measurements to acquire for Eye Height calibration.
Eye Mask Validation	Set to “True” to perform an eye mask validation test during calibration.
Eye Mask Max Violation Points	Define the maximum number of hits/violations that occur in the mask for eye mask validation.
EQ Eye Height Tolerance (mV)	Define the target tolerance value for equalization in mV during eye height validation.
Eye Width Tuning	Select “Retune” to repeat the tuning cycle or “Retry” to retry the current tuning procedure when measuring eye width.
Align Eye Mask Delay	Set to “True” to perform alignment for the delay in between validating the eye mask.
Maximum Retry	Enter the number of times to repeat calibration for pass/fail condition.
TP1 Calibration Method	Select the method to be used to perform post processing waveform analysis for TP1 stressed eye calibration. Select the SigTest signal quality test method or “Vendor Specific” to use other supported vendor specific methods (Keysight or Tektronix scope measurement tools).
TP3_EQ Calibration Method	Select the method to be used to perform post processing waveform analysis for TP3_EQ stressed eye calibration. Select the SigTest signal quality test method or “Vendor Specific” to use other supported vendor specific methods (Keysight or

	Tektronix scope measurement tools). <i>Note: Selecting “Vendor Specific” will enable the “Optimized EQ Look Up” calibration option under the TP3_EQ, TJ and Eye Height Calibration group.</i> 
SigTest Version	Enter the Version number of the SigTest signal quality test to be run during calibration to ensure waveform compliance. Make sure that the SigTest application is already installed in the test controller system.
SigTest Max Thread Count	Set the maximum process threads to generate for checking the Rx device functionality when running SigTest.
Remote File Server IP Address	Enter the IP address for the GRL Platform Solutions Remote Proxy Server. See Section 3.1.3 on how to set up the remote file server.
Remote File Server Port No	Enter the Port number for the GRL Platform Solutions Remote Proxy Server. See Section 3.1.3 on how to set up the remote file server.
Save SigTest Log	Set to “True” to generate a detailed log of all activities during the SigTest run.
SigTest Path	Enter the full path of the SigTest location in the test controller system.
TP3 Eye Average Times	Select the average number of times to measure the stressed eye at TP3_EQ.
Save BERT Setup Only	“False” is usually the case. Set to “True” if you are sure that you only want to save the BERT test setup in the Rx test.
Prompt Before Link Training	“False” is usually the case. Set to “True” if you want to be prompted prior to start running link training.
Skip DUT Reset	“False” is usually the case. Set to “True” if you want to reset the DUT when performing tests.
PreEmphasis/Swing Loop Method	Select whether to use the incremental or DisplayPort Configuration Data (DPCD) register method for adjusting the Pre-emphasis and Swing voltage.

Initialize Training Lane Set	Set to “True” to reset HDCP register(0x102) before sending training pattern.
Symbol Lock Initial Preset	Select the initial preset setting for symbol lock.
Reset Link Register	Set to “True” to perform link register reset during testing.
Ignore Error Count Mismatch	Set to “True” to ignore any differences in the error counts obtained during testing.
Always Initialize BERT	Set to “True” to bypass BERT initialization during testing.
Skip Link Training When SJ Changed	Set to “True” to skip the loopback link training sequence when there is a change in the SJ frequency.
Interval Time Factor	Specify the factor value for bit errors to be counted over a specified time interval.
Change Preset	Set to “True” to enable the preset setting to be adjusted during link training.
Skip Frequency Lock	“False” is usually the case. Set to “True” if you are sure that you want to skip frequency lock after performing link training for frequency.
Skip Symbol Lock	“False” is usually the case. Set to “True” if you are sure that you want to skip symbol lock during link training.
Scrambling Disable	Set to “True” to disable scrambling during link training.
Enhanced Frame Enable Register	“False” is usually the case. Set to “True” if you are sure that you want to enable the enhanced framing symbol mode.
Check Inter Lane Align (0x204)	“False” is usually the case. Set to “True” if you want to make sure that all lanes are aligned by reading register 0x204.
Write 0x108 after 0x100	“False” is usually the case. Set to “True” if you are sure that you want to write register 0x108 after register 0x100.
Use Calibration Preset	“False” is usually the case. Set to “True” if you want to use a specific preset from calibration to run the signal quality test.
Link Training Signal Logic	Select to use a positive (POS) or a negative (NEG) logic level for the link training signals.
BER Test Signal Logic	Select to use a positive (POS) or a negative (NEG) logic level for the BER measurement signals.
TBT5 20G Disable SSC	“False” is usually the case. Set to “True” to disable Spread Spectrum Clocking (SSC) on a Thunderbolt 5 20G connection.
BERT Type	Select whether the BERT supports NRZ (Non-Return-to-Zero) or PAM4 (Pulse Amplitude Modulation 4-level) signaling.
Symbol Lock EQ Timeout	“False” is usually the case. Set to “True” to enable symbol lock equalization timeout which is the maximum amount of time allowed for the receiver to achieve symbol lock and complete the equalization procedure before an error is declared.

Enable CDS Flow	“True” is usually the case. Set to “False” to disable Continuous Data Scrambling (CDS) for UHBR modes.
10G, 13.5G & 20G Compliance Test Duration (s)	Set how long it would take (in seconds) to test the DUT for 10G, 13.5G or 20G compliance.
Maximum Compliance Error	Define the maximum error count for error checking during compliance tests.
Margin Step Size (%)	Set the step size for stepping through SJ or amplitude margins when running the optional margin search tests.
Maximum Margin Test Error	Define the maximum error count for error checking during margin search tests.
Maximum Steps	Define the maximum number of steps to step through margins.
20G, 13.5G & 10G Margin Test Minimum Bits (E9)	Set the minimum number of bits to run margin search tests for the 20 Gb/s, 13.5 Gb/s and 10 Gb/s data rates.
Margin Start (%)	Set the start point for the margin search test.
Prompt to Reset DUT	“False” is usually the case. Set to “True” if you want to be prompted to reset the DUT when performing tests.
SJ1, SJ2, SJ3, SJ4, SJ5 & SJ6 Margin Step Size (%)	Set the step size for stepping through each defined SJ# margin when running the optional margin search tests.

3.5 Configure Calibration Target Values

For debugging purposes ONLY, the default calibration target values can be changed for

certain calibration. To do this, select  from the menu to access the Calibration Target page.

By default, the calibration target values are those defined in the specification. To change the values, un-select the ‘Use Default Value’ checkbox. In case the default values are required again, just select the checkbox to allow all existing values to be reset to default.

Note: The PID Control setting is used to adjust the step width for steps calculation if the target measurement cannot be met with the current step. To adjust, use a lower PID Control value to reduce the subsequent step or increase the control value to make the subsequent step bigger.

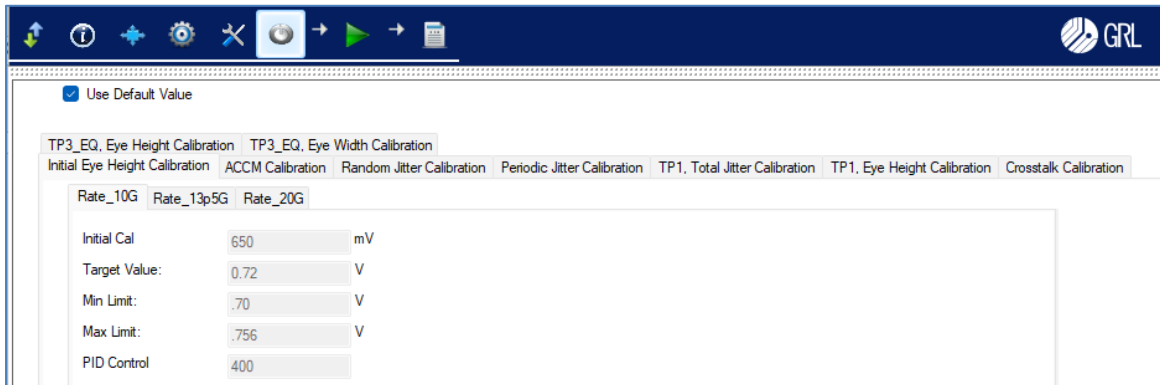


FIGURE 27. CALIBRATION OVERWRITE

3.6 Run Calibration/Tests

Select  from the menu to access the Run Tests page. The GRL Platform Solutions software automatically runs the selected calibration or tests when initiated.

Before running the calibration or tests, select the option to:

- **Skip Test if Result Exists** – If results from previous calibration/tests exist, the software will *skip* those calibration/tests.
- **Replace if Result Exists** – If results from previous calibration/tests exist, the software will *replace* those calibration/tests with new results.

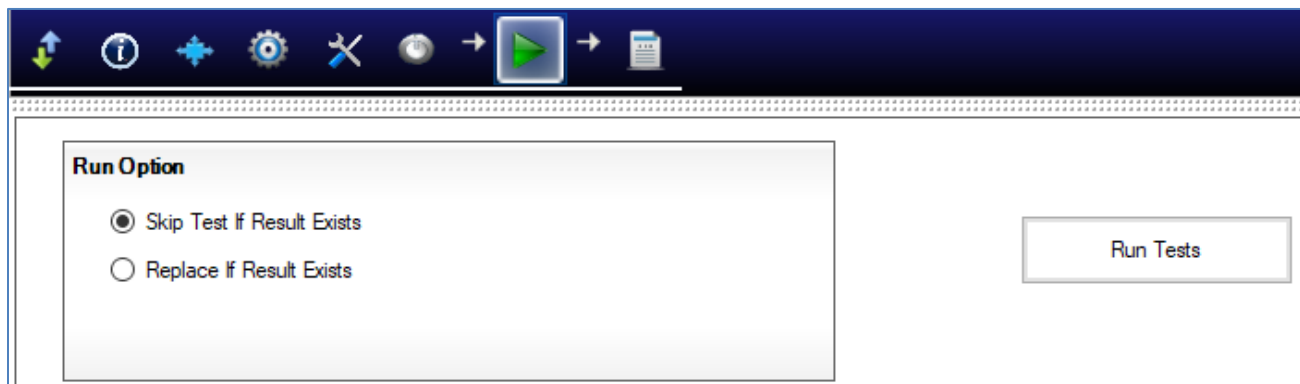


FIGURE 28. RUN TESTS PAGE

Select the **Run Tests** button to start running the selected calibration or tests. The connection diagram for the calibration or test being run will initially appear to allow the user to make sure that the calibration/test environment has been properly set up before calibration/test can proceed.

If you need to re-run only certain calibration or tests on certain conditions, please delete the calibration or tests from the Report page and Run with **Skip Test if Result Exists**. The GRL Platform Solutions software will keep track of the missing calibration or tests in the report and perform those calibration or tests only. See Section 6 for more information on Test Reports.

4 Sink Calibration Connection Setups

This section shows the typical connection setups to perform automated Sink Test Calibration.

4.1 Pre-Calibration/Test Procedures

Prior to running any calibration or test, the following steps must be taken to assure accurate measurements:

1. Allow a minimum of 20 minutes warm-up time for the Oscilloscope and MP1900A BERT.
2. Run the Scope's SPC calibration routine. It is necessary to remove all probes from the Scope before running SPC.
3. Make sure you use a torque wrench with the proper torque specification to make all SMA connections.

4.2 Connection Setup for Anritsu MP1900A BERT Generator Set

Figure 29 shows the connection setup between each module of the Anritsu MP1900A BERT Generator Set.

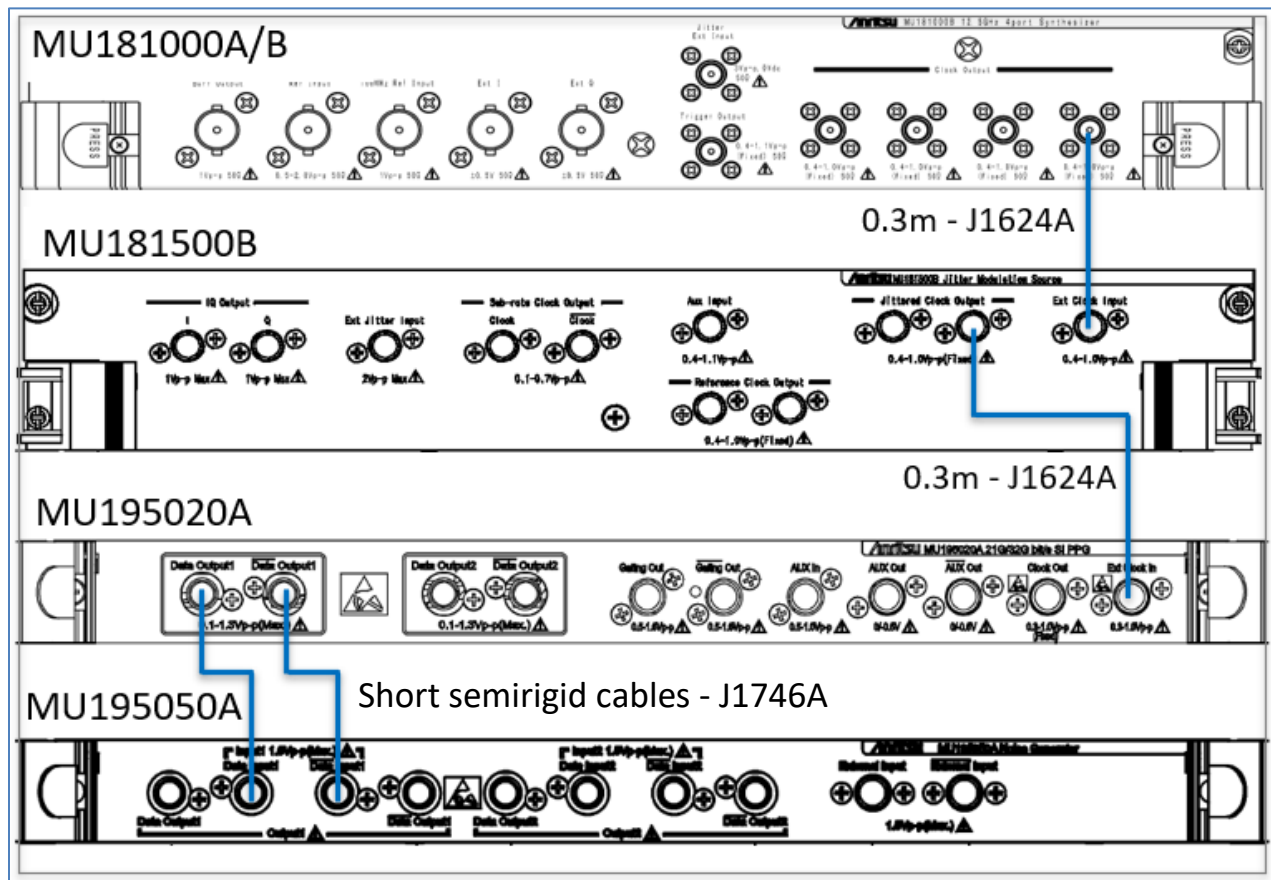


FIGURE 29. CONNECTION SETUP FOR MP1900A BERT GENERATOR SET MODULES

Connection Steps:

1. Using the J1624A SMA-SMA (0.3m) cable, connect the Clock Output of the MU181000A/B Synthesizer to the Ext Clock Input of the MU181500B Jitter Modulator.
2. Using the J1624A SMA-SMA (0.3m) cable, connect the Jittered Clock Output of the MU181500B Jitter Modulator to the Ext Clock Input of the MU195020A Pulse Pattern Generator.
3. Using the J1746A K-K skew matched pair short semirigid cable, connect the MU195020A Data Output1's to the MU195050A Data Input1's.

4.3 DisplayPort USB Type-C Fixture Connector Pin Assignments

Figure 30 shows the pin assignments/ID for each connector pin of the DisplayPort USB Type-C Receptacle Fixture.

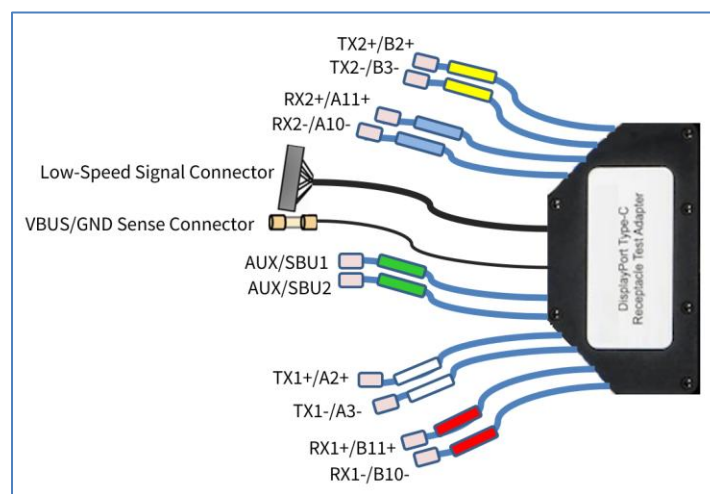


FIGURE 30. DISPLAYPORT USB TYPE-C RECEPTACLE FIXTURE CONNECTOR PIN ASSIGNMENTS

Figure 31 shows the pin assignments/ID for each connector pin of the DisplayPort USB Type-C Plug Fixture.

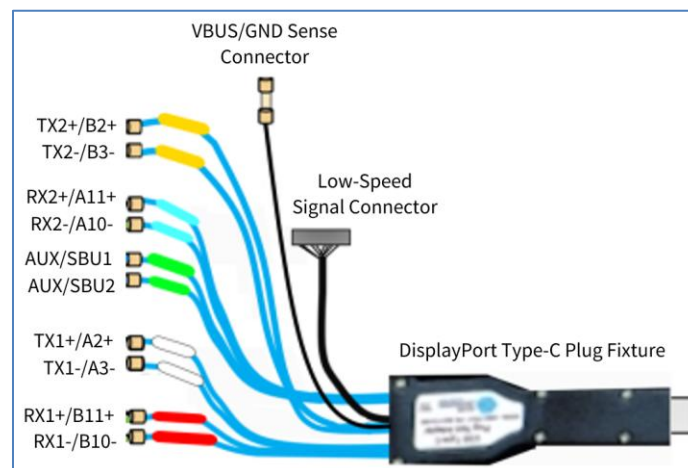


FIGURE 31. DISPLAYPORT USB TYPE-C PLUG FIXTURE CONNECTOR PIN ASSIGNMENTS

4.4 Standard/Mini DisplayPort Fixture Connector Pin Assignments

Figure 32 shows the pin assignments/ID for each connector pin of the Standard/Mini DisplayPort Receptacle Fixture.

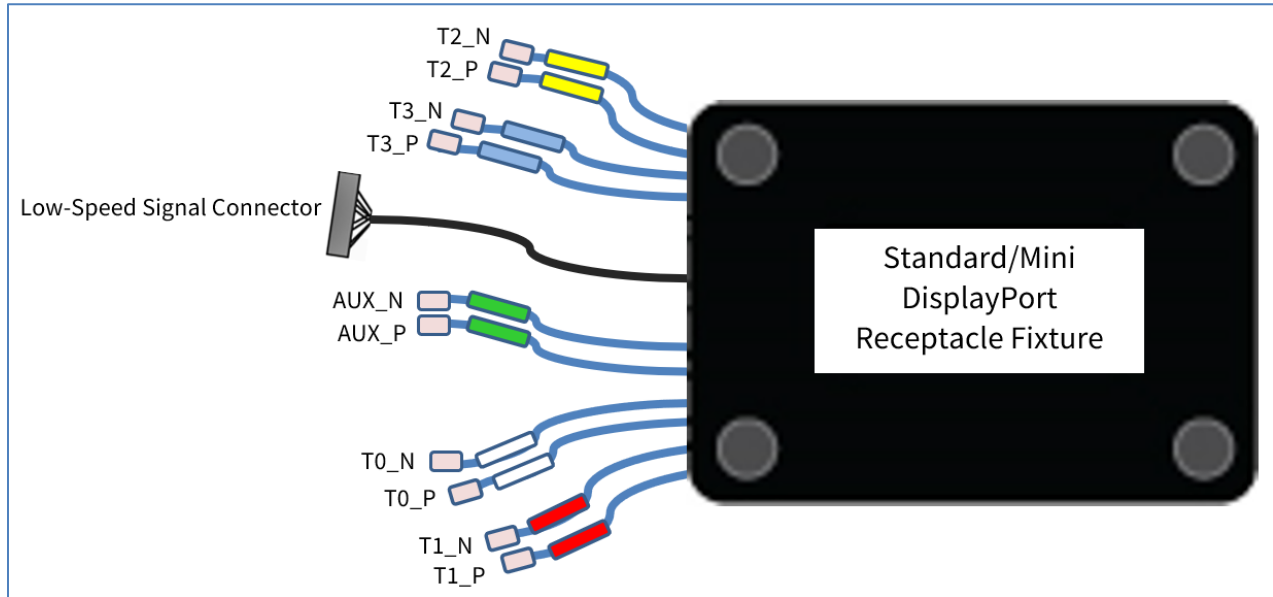


FIGURE 32. STANDARD/MINI DISPLAYPORT RECEPTACLE FIXTURE CONNECTOR PIN ASSIGNMENTS

Figure 33 shows the pin assignments/ID for each connector pin of the Standard/Mini DisplayPort Plug Fixture.

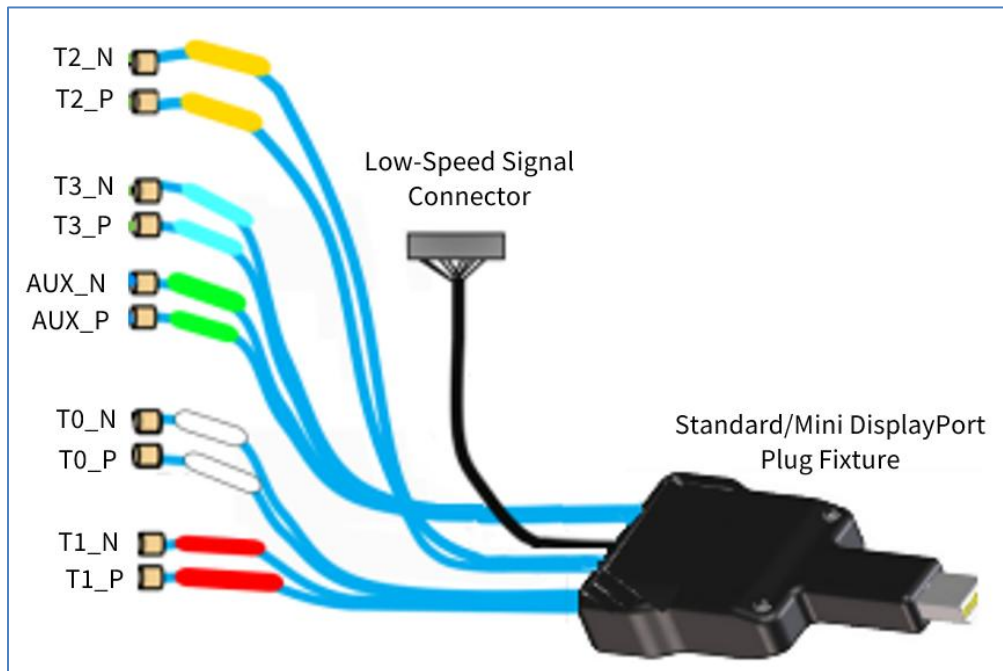


FIGURE 33. STANDARD/MINI DISPLAYPORT PLUG FIXTURE CONNECTOR PIN ASSIGNMENTS

4.5 Calibration Connection Setups

4.5.1 Calibration Setup at TP1

Figure 34 below shows the typical setup for Sink signal calibration at Test Point 1.

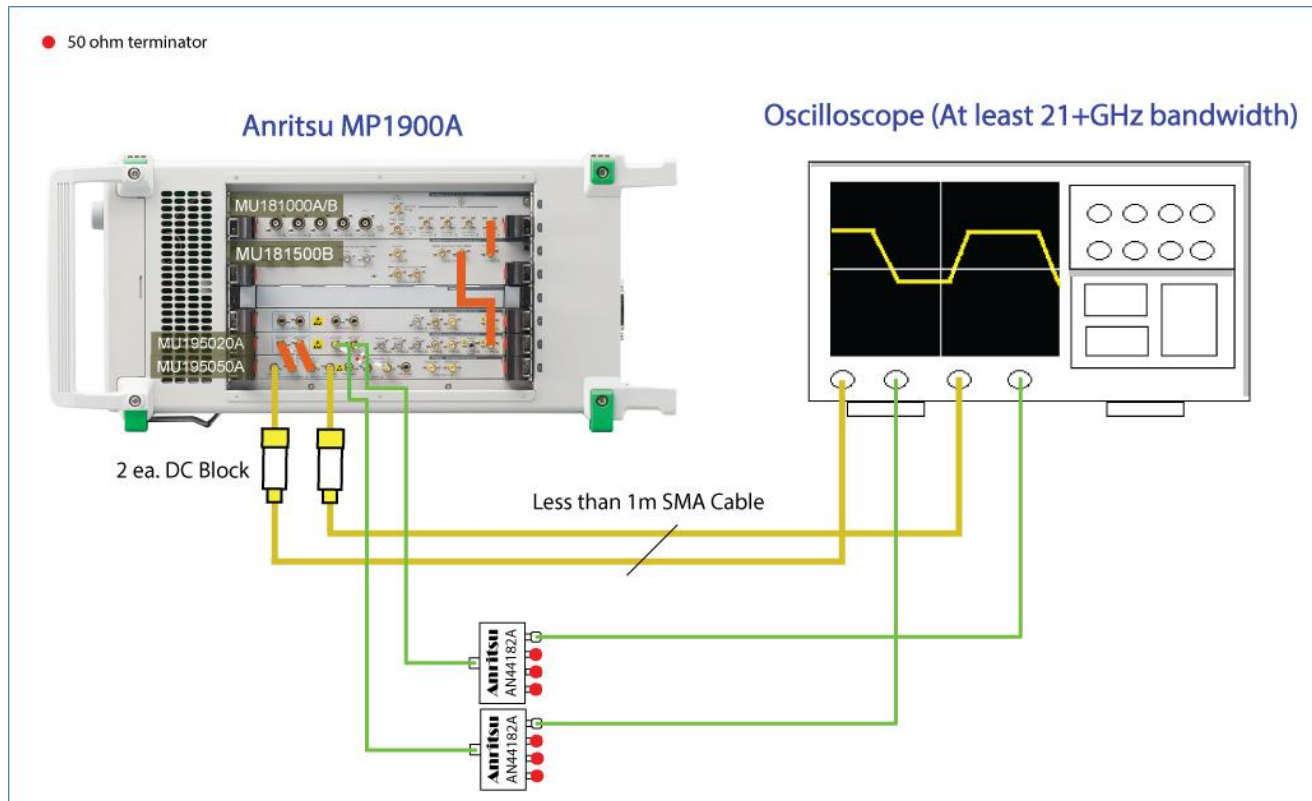


FIGURE 34. TYPICAL TP1 SINK CALIBRATION SETUP

Connection Steps:

1. Using the MP1900A BERT setup connections (Section 4.2), connect the MU195050A first data outputs through DC blocks to Channels 1 and 3 on the Scope using phase matched K-K coaxial cables.
2. Connect the MU195020A second data outputs through the AN44182A Power Dividers to Channels 2 and 4 on the Scope using phase matched K-K coaxial cables to inject crosstalk. *Note: The unused output lanes of the power dividers must be terminated with 50 Ω terminators.*

4.5.2 Calibration Setup at TP3_EQ for DisplayPort USB Type-C Mode

Figure 35, Figure 36 and Figure 37 below show the DisplayPort USB Type-C mode typical setup for Sink signal calibration at Test Point 3 with Equalizer applied. TP3_EQ is a physical test point that will affect the eye opening due to the sum of a fixed channel length (representing the fixed ISI on the transmitter side of a host or device) and a physical USB Type-C Cable.

- For the UHBR10 (10 Gb/s) data rate, the total Insertion Loss is -19 dB at 5 GHz, which uses a 2M USB Type-C cable.
- For the UHBR13.5 (13.5 Gb/s) data rate, the total Insertion Loss is -17.5 dB at 6.75 GHz, which uses a 0.8M USB Type-C cable.
- For the UHBR20 (20 Gb/s) data rate, the total Insertion Loss is -16.5 dB at 10 GHz, which uses a 0.8M USB Type-C cable.

The cable's downstream plug connector is connected to a DisplayPort 2.1 receptacle adapter fixture to measure the signal with the scope. The scope uses software equalization to open the eye for calibration.

Note: Cables connecting the signal to the Scope should be de-embedded and $\leq 1m$.

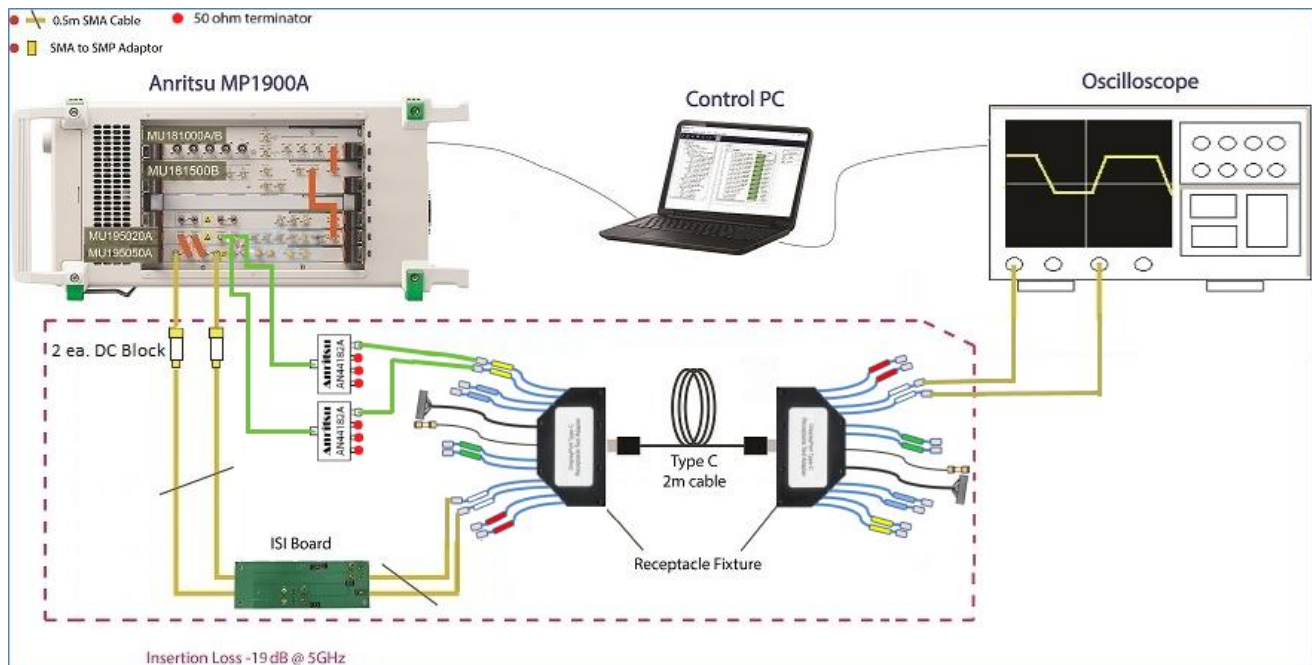


FIGURE 35. SETUP FOR TP3_EQ CALIBRATION AT 10G FOR DISPLAYPORT USB TYPE-C MODE

Connection Steps:

1. Continuing from the MP1900A BERT TP1 calibration setup (Section 4.5.1), disconnect the MU195050A data outputs from the scope channels.
2. Connect the MU195050A first data outputs through DC blocks to ISI channels (for 10 Gb/s) and then to the receptacle adapter fixtures (at TX1+/A2+ and TX1-/A3- pins) with a 2M USB Type-C cable, and then to Channels 1 and 3 on the scope.
3. Connect the MU195020A second data outputs through the AN44182A Power Dividers to the Rx lanes of the receptacle adapter fixture that are not under test (for example, at

TX2+/B2+ and TX2-/B3- pins) to inject crosstalk. *Note: The unused output lanes of the power dividers must be terminated with 50 Ω terminators.*

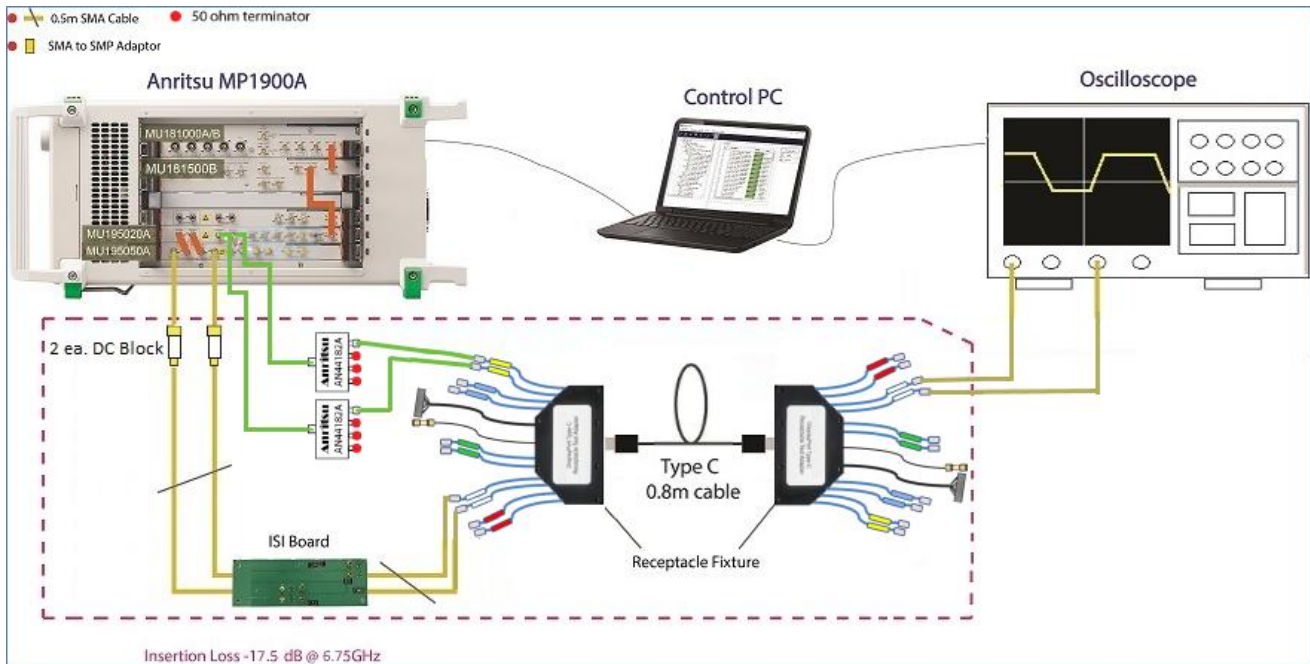


FIGURE 36. SETUP FOR TP3_EQ CALIBRATION AT 13.5G FOR DISPLAYPORT USB TYPE-C MODE

Connection Steps:

1. Continuing from the MP1900A BERT TP1 calibration setup (Section 4.5.1), disconnect the MU195050A data outputs from the scope channels.
2. Connect the MU195050A data outputs through DC blocks to ISI channels (for 13.5Gb/s) and then to the receptacle adapter fixtures (at TX1+/A2+ and TX1-/A3- pins) with a 0.8M USB Type-C cable, and then to Channels 1 and 3 on the scope.
3. Connect the MU195020A second data outputs through the AN44182A Power Dividers to the Rx lanes of the receptacle adapter fixture that are not under test (for example, at TX2+/B2+ and TX2-/B3- pins) to inject crosstalk. *Note: The unused output lanes of the power dividers must be terminated with 50 Ω terminators.*

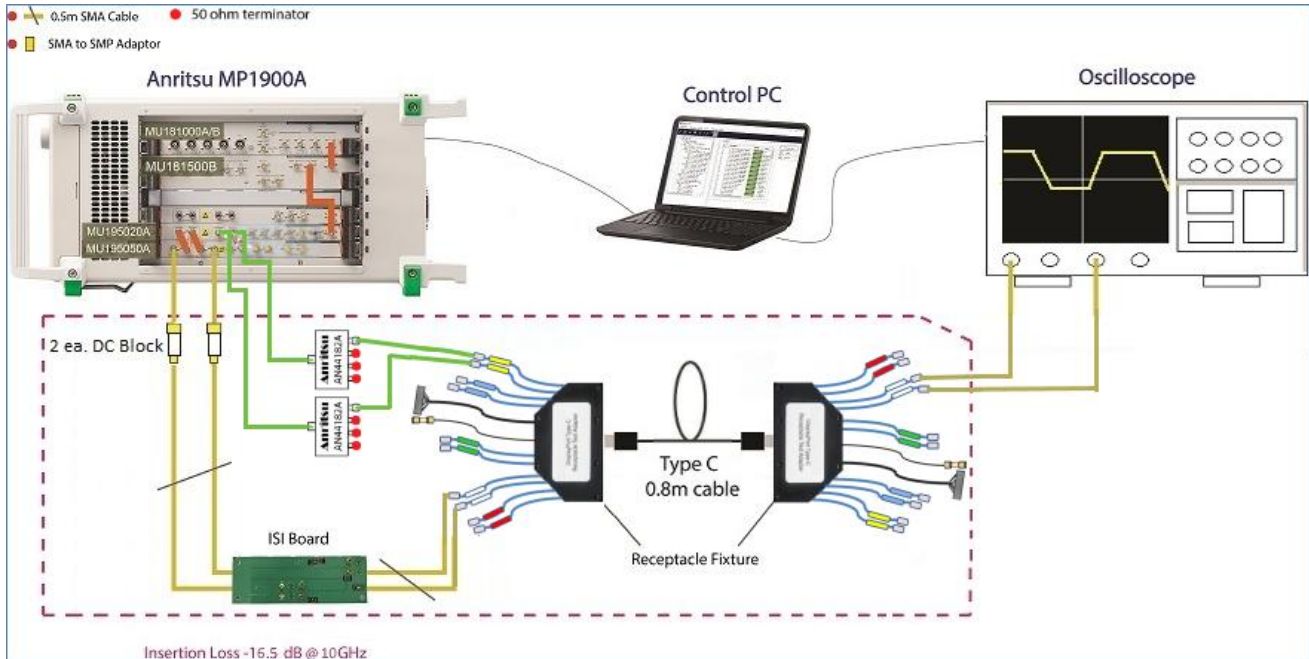


FIGURE 37. SETUP FOR TP3_EQ CALIBRATION AT 20G FOR DISPLAYPORT USB TYPE-C MODE

Connection Steps:

1. Continuing from the MP1900A BERT TP1 calibration setup (Section 4.5.1), disconnect the MU195050A data outputs from the scope channels.
2. Connect the MU195050A data outputs through DC blocks to ISI channels (for 20Gb/s) and then to the receptacle adapter fixtures (at TX1+/A2+ and TX1-/A3- pins) with a 0.8M USB Type-C cable, and then to Channels 1 and 3 on the scope.
3. Connect the MU195020A second data outputs through the AN44182A Power Dividers to the Rx lanes of the receptacle adapter fixture that are not under test (for example, at TX2+/B2+ and TX2-/B3- pins) to inject crosstalk. *Note: The unused output lanes of the power dividers must be terminated with 50 Ω terminators.*

4.5.3 Calibration Setup at TP3_EQ for Standard/Mini DisplayPort Mode

Figure 38, Figure 39 and Figure 40 below show the Standard/Mini DisplayPort mode typical setup for Sink signal calibration at Test Point 3 with Equalizer applied. TP3_EQ is a physical test point that will affect the eye opening due to the sum of a fixed channel length (representing the fixed ISI on the transmitter side of a host or device) and a physical USB Type-C Cable.

- For the UHBR10 (10 Gb/s) data rate, the total Insertion Loss is -19 dB at 5 GHz, which uses a 2M Standard/Mini DisplayPort cable.
- For the UHBR13.5 (13.5 Gb/s) data rate, the total Insertion Loss is -16.5 dB at 6.75 GHz, which uses a 0.8M Standard/Mini DisplayPort cable.
- For the UHBR20 (20 Gb/s) data rate, the total Insertion Loss is -16.5 dB at 10 GHz, which uses a 0.8M Standard/Mini DisplayPort cable.

The cable's downstream plug connector is connected to a Standard/Mini DisplayPort receptacle adapter fixture to measure the signal with the scope. The scope uses software equalization to open the eye for calibration.

Note: Cables connecting the signal to the Scope should be de-embedded and $\leq 1\text{m}$.

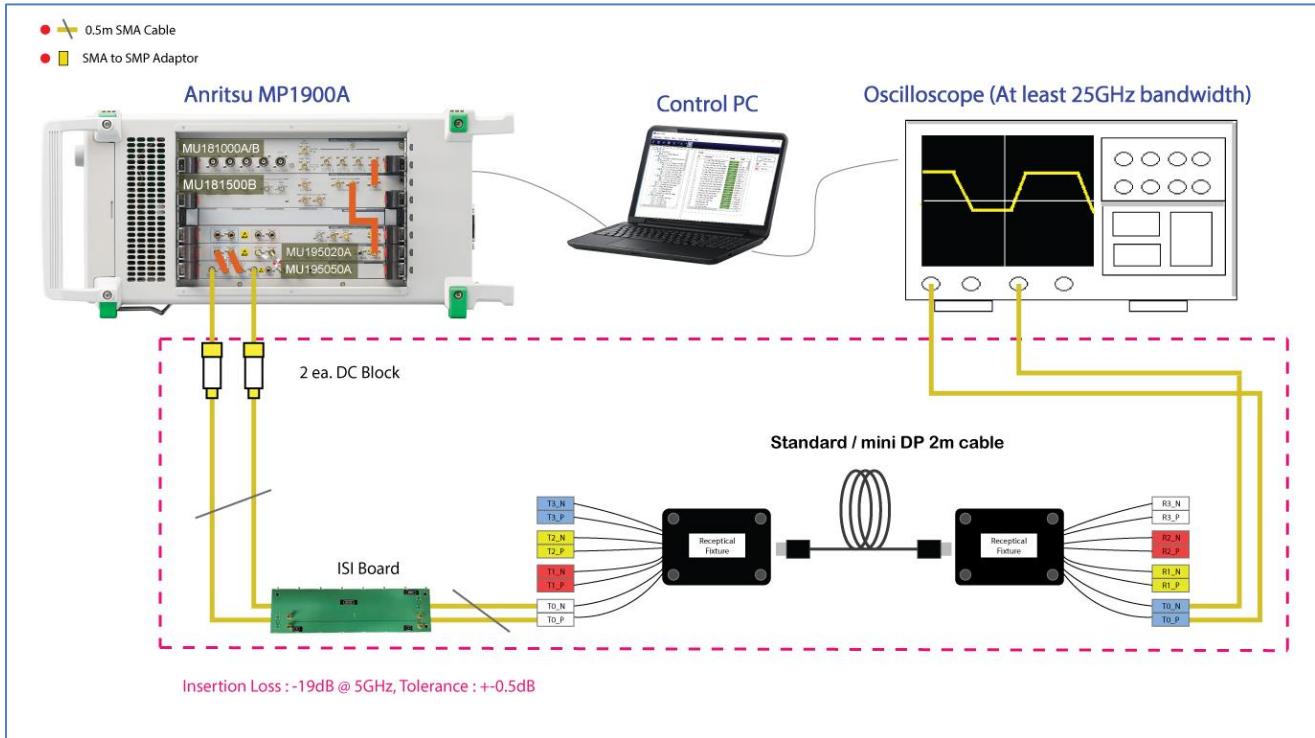


FIGURE 38. SETUP FOR TP3_EQ CALIBRATION AT 10G FOR STANDARD/MINI DISPLAYPORT MODE

Connection Steps:

1. Continuing from the MP1900A BERT TP1 calibration setup (Section 4.5.1), disconnect the MU195050A data outputs from the scope channels.
2. Connect the MU195050A data outputs through DC blocks to ISI channels (for 10 Gb/s) and then to the receptacle adapter fixtures (at T0_N and T0_P pins) with a 2M Standard/Mini DisplayPort cable, and then to Channels 1 and 3 on the scope.

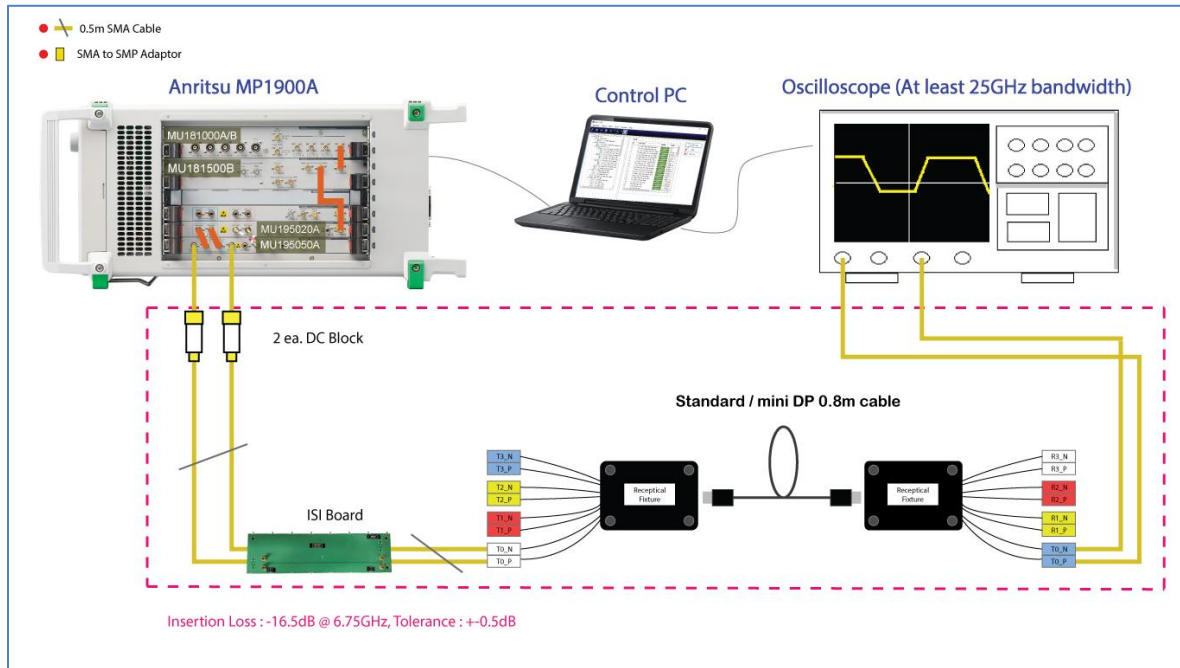


FIGURE 39. SETUP FOR TP3_EQ CALIBRATION AT 13.5G FOR STANDARD/MINI DISPLAYPORT MODE

Connection Steps:

1. Continuing from the MP1900A BERT TP1 calibration setup (Section 4.5.1), disconnect the MU195050A data outputs from the scope channels.
2. Connect the MU195050A data outputs through DC blocks to ISI channels (for 13.5Gb/s) and then to the receptacle adapter fixtures (at T0_N and T0_P pins) with a 0.8M Standard/Mini DisplayPort cable, and then to Channels 1 and 3 on the scope.

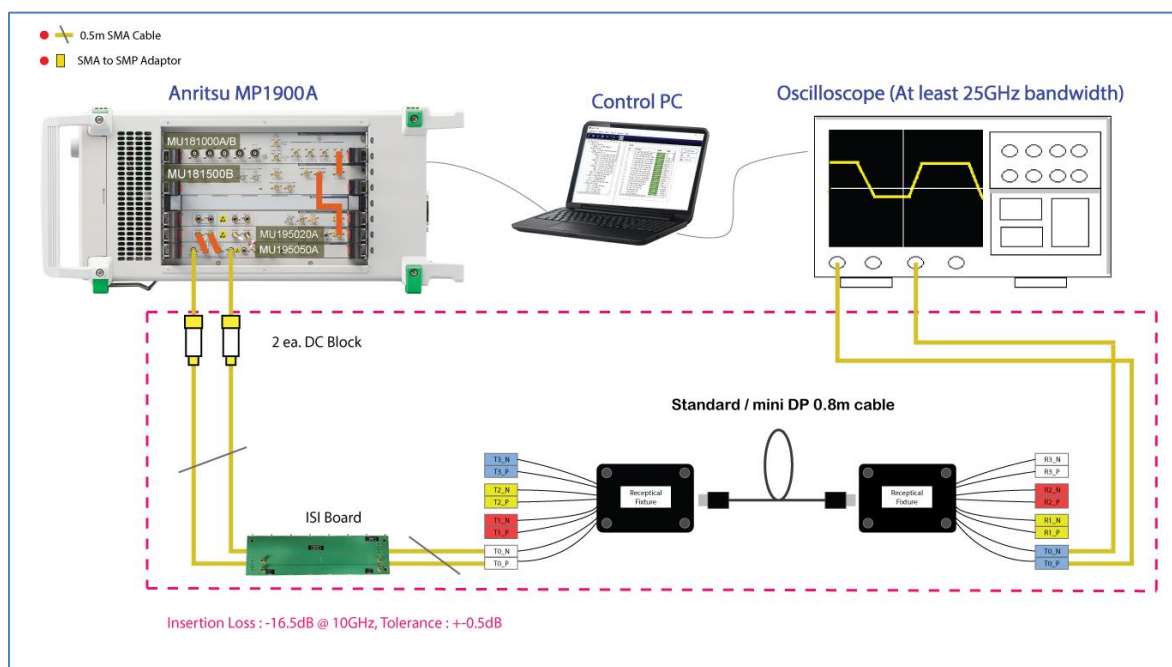


FIGURE 40. SETUP FOR TP3_EQ CALIBRATION AT 20G FOR STANDARD/MINI DISPLAYPORT MODE

Connection Steps:

1. Continuing from the MP1900A BERT TP1 calibration setup (Section 4.5.1), disconnect the MU195050A data outputs from the scope channels.
2. Connect the MU195050A data outputs through DC blocks to ISI channels (for 20Gb/s) and then to the receptacle adapter fixtures (at T0_N and T0_P pins) with a 0.8M Standard/Mini DisplayPort cable, and then to Channels 1 and 3 on the scope.

5 Sink DUT Compliance Test Setups

After calibration has completed, testing the DisplayPort Sink DUT for CTS compliance can be performed. The GRL-DP21-SINK-AN application supports automated testing of a DisplayPort Sink device if the device supports standard DPCD through the AUX channel or a compatible AUX controller is connected.

5.1 Test Connection Setups

5.1.1 DUT BER Compliance Test Setup at TP2 for DisplayPort USB Type-C Mode

Figure 41 below shows the DisplayPort USB Type-C mode physical setup for the DisplayPort Sink DUT BER test at Test Point 2. The calibrated stressed signal is attached to a DisplayPort 2.1 USB Type-C plug fixture and crosstalk is added to the fixture from the MP1900A BERT. The AUX controller is connected to a DisplayPort 2.1 control board which is also connected to a USB Type-C Host and is used to directly control the DUT by executing test scripts.

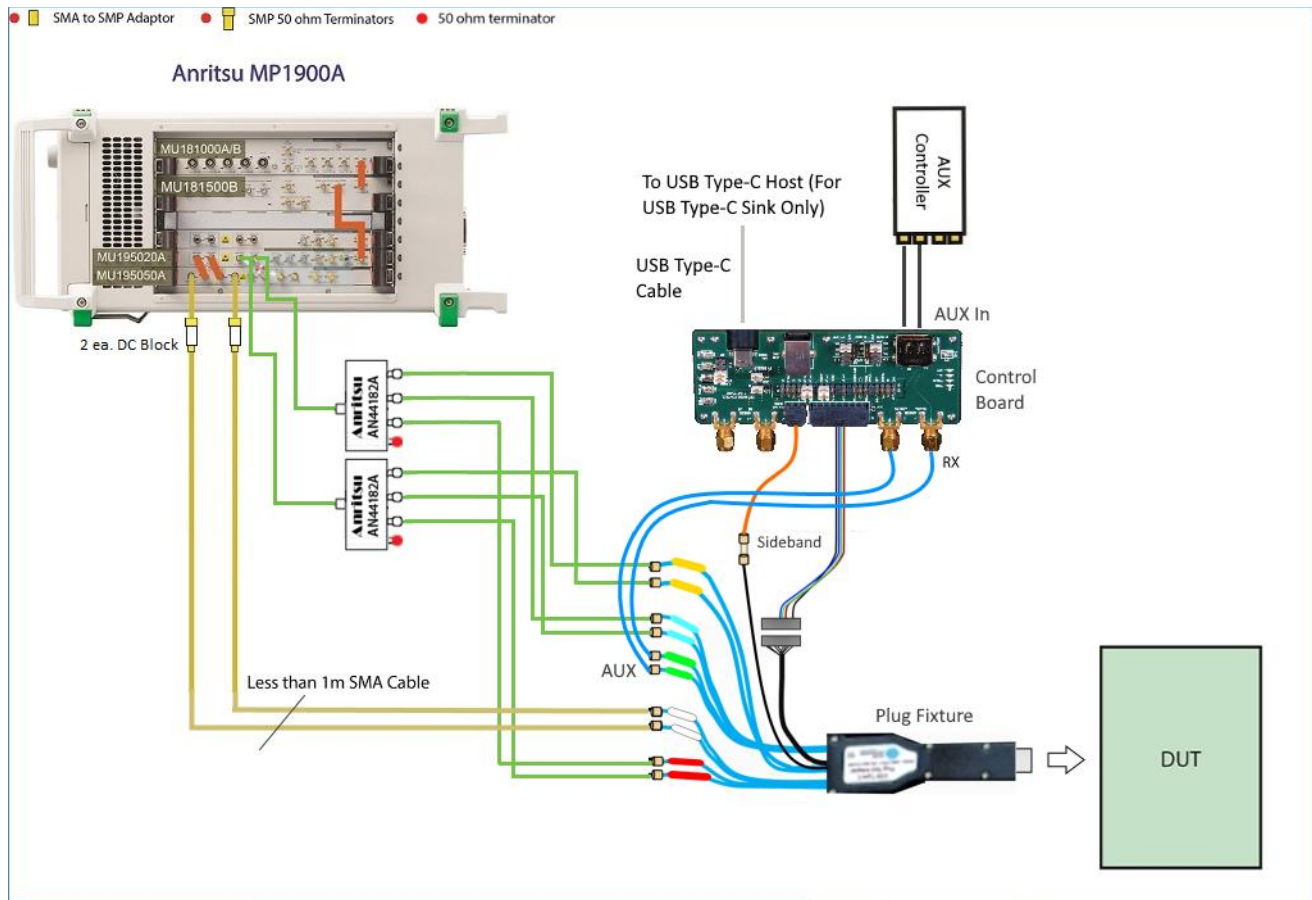


FIGURE 41. BER COMPLIANCE TEST SETUP FOR DP SINK DUT AT TP2 FOR DISPLAYPORT USB TYPE-C MODE

Connection Steps:

1. Attach the USB Type-C connector of the DisplayPort 2.1 plug fixture to the DUT's USB Type-C receptacle connector.

2. Using the MP1900A BERT TP1 calibration setup (Section 4.5.1), disconnect the MU195050A data outputs from the scope channels.
3. Connect the MU195050A first data outputs through DC blocks to Rx Lane0/Lane1 of the DUT through the DisplayPort 2.1 plug fixture (at TX1+/A2+ and TX1-/A3- pins).
4. Connect the MU195020A second data outputs through the AN44182A Power Dividers to the Rx lanes of the DUT that are not under test through the plug fixture (for example, at TX2+/B2+ & TX2-/B3- pins, RX2+/A11+ & RX2-/A10- pins, and RX1+/B11+ & RX1-/B10- pins respectively) to inject crosstalk. *Note: The unused output lanes of the power dividers must be terminated with 50 Ω terminators.*
5. Connect the green AUX cable pair of the plug fixture to the Rx lanes of the DisplayPort 2.1 control board.
6. Connect the sideband cables of the plug fixture to their allocated slots on the control board.
7. Connect the AUX controller to power supply.
8. Connect the AUX controller output to the AUX input connector of the control board.
9. Connect the control board to a USB Type-C Host using a USB Type-C cable.
10. Run the AUX controller test scripts from the USB Type-C Host to control the DUT.

5.1.2 DUT BER Compliance Test Setup at TP2 for Standard/Mini DisplayPort Mode

Figure 42 below shows the Standard/Mini DisplayPort mode physical setup for the DisplayPort Sink DUT BER test at Test Point 2. The calibrated stressed signal is attached to a Standard/Mini DisplayPort plug fixture and crosstalk is added to the fixture from the MP1900A BERT. The AUX controller is connected to a DisplayPort 2.1 control board which is also connected to a USB Type-C Host and is used to directly control the DUT by executing test scripts.

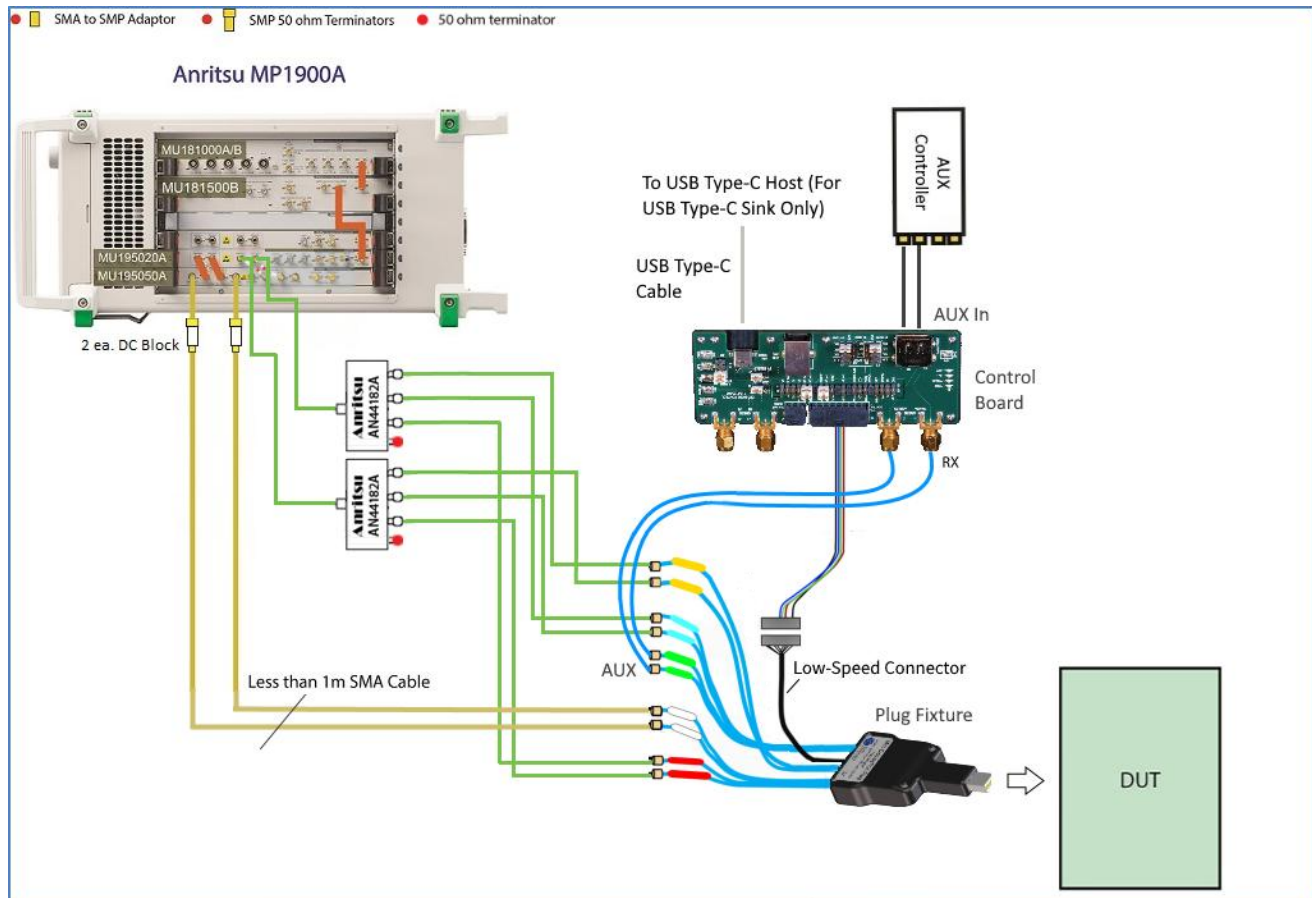


FIGURE 42. BER COMPLIANCE TEST SETUP FOR DP SINK DUT AT TP2 FOR STANDARD/MINI DISPLAYPORT MODE

Connection Steps:

1. Attach the Standard/Mini DisplayPort connector of the DisplayPort plug fixture to the DUT's Standard/Mini DisplayPort receptacle connector.
2. Using the MP1900A BERT TP1 calibration setup (Section 4.5.1), disconnect the MU195050A data outputs from the scope channels.
3. Connect the MU195050A first data outputs through DC blocks to Rx Lane0/Lane1 of the DUT through the DisplayPort 2.1 plug fixture (at T0_P and T0_N pins).
4. Connect the MU195020A second data outputs through the AN44182A Power Dividers to the Rx lanes of the DUT that are not under test through the plug fixture (for example, at T2_P & T2_N pins, T3_P & T3_N pins, and T1_P & T1_N pins respectively) to inject

crosstalk. *Note: The unused output lanes of the power dividers must be terminated with 50 Ω terminators.*

5. Connect the green AUX cable pair of the plug fixture to the Rx lanes of the DisplayPort 2.1 control board.
6. Connect the low-speed connector cable of the receptacle adapter to the allocated slot on the control board.
7. Connect the AUX controller to power supply.
8. Connect the AUX controller output to the AUX input connector of the control board.
9. Connect the control board to a USB Type-C Host using a USB Type-C cable.
10. Run the AUX controller test scripts from the USB Type-C Host to control the DUT.

5.1.3 DUT BER Compliance Test Setup at TP3_EQ for DisplayPort USB Type-C Mode

Figure 43 and Figure 44 show the DisplayPort USB Type-C Mode physical setups for the DisplayPort Sink DUT BER test at Test Point 3 with Equalizer applied.

The calibrated stressed signal (with ISI) is attached to a DisplayPort 2.1 USB Type-C receptacle adapter and crosstalk is added to the adapter from the MP1900A BERT. The AUX controller is connected to a DisplayPort 2.1 control board which is also connected to a USB Type-C Host and is used to directly control the DUT by executing test scripts. A USB Type-C cable is connected between the DisplayPort 2.1 receptacle adapter and the DUT's USB Type-C receptacle connector as follows:

- For the UHBR10 (10 Gb/s) data rate, the setup uses a 2M USB Type-C cable.
- For the UHBR13.5 (13.5 Gb/s) and UHBR20 (20 Gb/s) data rates, the setup uses a 0.8M USB Type-C cable.

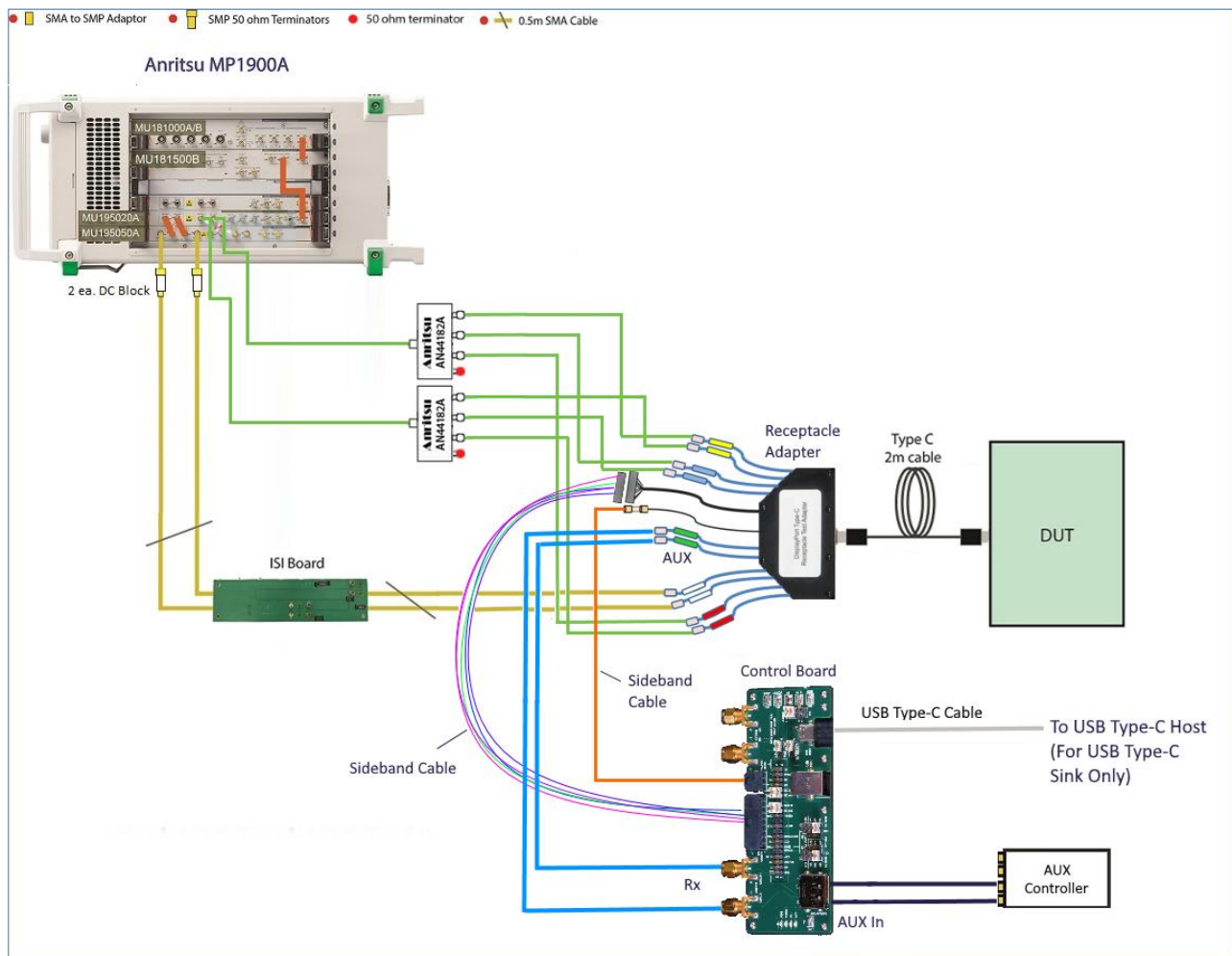


FIGURE 43. DISPLAYPORT USB TYPE-C MODE BER COMPLIANCE TEST SETUP FOR DP SINK DUT AT TP3_EQ AT 10G

Connection Steps:

1. Using the MP1900A BERT TP3_EQ calibration setup (Section 4.5.2), disconnect the DisplayPort 2.1 receptacle adapter fixture that connects to the scope.

2. Attach the 2M USB Type-C cable to the DUT's USB Type-C receptacle connector.
3. Connect the ISI channels to Rx Lane0/Lane1 of the DisplayPort 2.1 receptacle adapter (at TX1+/A2+ and TX1-/A3- pins).
4. Connect the AN44182A Power Dividers to the Rx lanes of the receptacle adapter that are not under test (for example, at TX2+/B2+ & TX2-/B3- pins, RX2+/A11+ & RX2-/A10- pins, and RX1+/B11+ & RX1-/B10- pins respectively) to inject crosstalk. *Note: The unused output lanes of the power dividers must be terminated with 50 Ω terminators.*
5. Connect the green AUX cable pair of the receptacle adapter to the Rx lanes of the DisplayPort 2.1 control board.
6. Connect the sideband cables of the receptacle adapter to their allocated slots on the control board.
7. Connect the AUX controller to power supply.
8. Connect the AUX controller output to the AUX input connector of the control board.
9. Connect the control board to a USB Type-C Host using a USB Type-C cable.
10. Run the AUX controller test scripts from the USB Type-C Host to control the DUT.

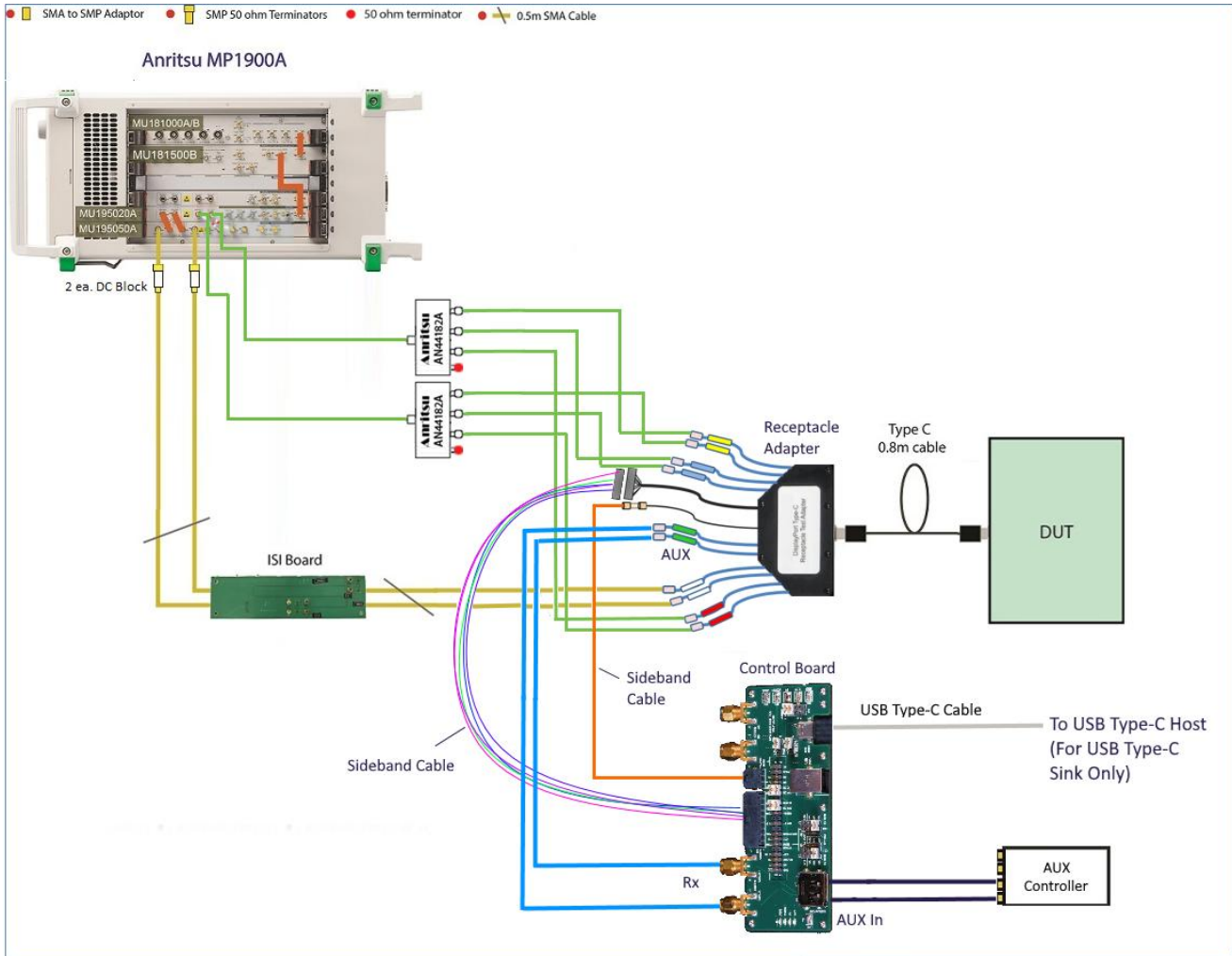


FIGURE 44. DISPLAYPORT USB TYPE-C MODE BER COMPLIANCE TEST SETUP FOR DP SINK DUT AT TP3_EQ AT 13.5G AND 20G

Connection Step:

Using the same setup for TP3_EQ at 10G in Figure 43, replace the 2M USB Type-C cable with the 0.8M USB Type-C cable to the DUT's USB Type-C receptacle connector.

5.1.4 DUT BER Compliance Test Setup at TP3_EQ for Standard/Mini DisplayPort Mode

Figure 45 and Figure 46 below show the Standard/Mini DisplayPort Mode physical setups for the DisplayPort Sink DUT BER test at Test Point 3 with Equalizer applied.

The calibrated stressed signal (with ISI) is attached to a Standard/Mini DisplayPort receptacle adapter and crosstalk is added to the adapter from the MP1900A BERT. The AUX controller is connected to a DisplayPort 2.1 control board which is also connected to a USB Type-C Host and is used to directly control the DUT by executing test scripts. A Standard/Mini DisplayPort cable is connected between the Standard/Mini DisplayPort receptacle adapter and the DUT's Standard/Mini DisplayPort receptacle connector as follows:

- For the UHBR10 (10 Gb/s) data rate, the setup uses a 2M USB Type-C cable.
- For the UHBR13.5 (13.5 Gb/s) and UHBR20 (20 Gb/s) data rates, the setup uses a 0.8M USB Type-C cable.

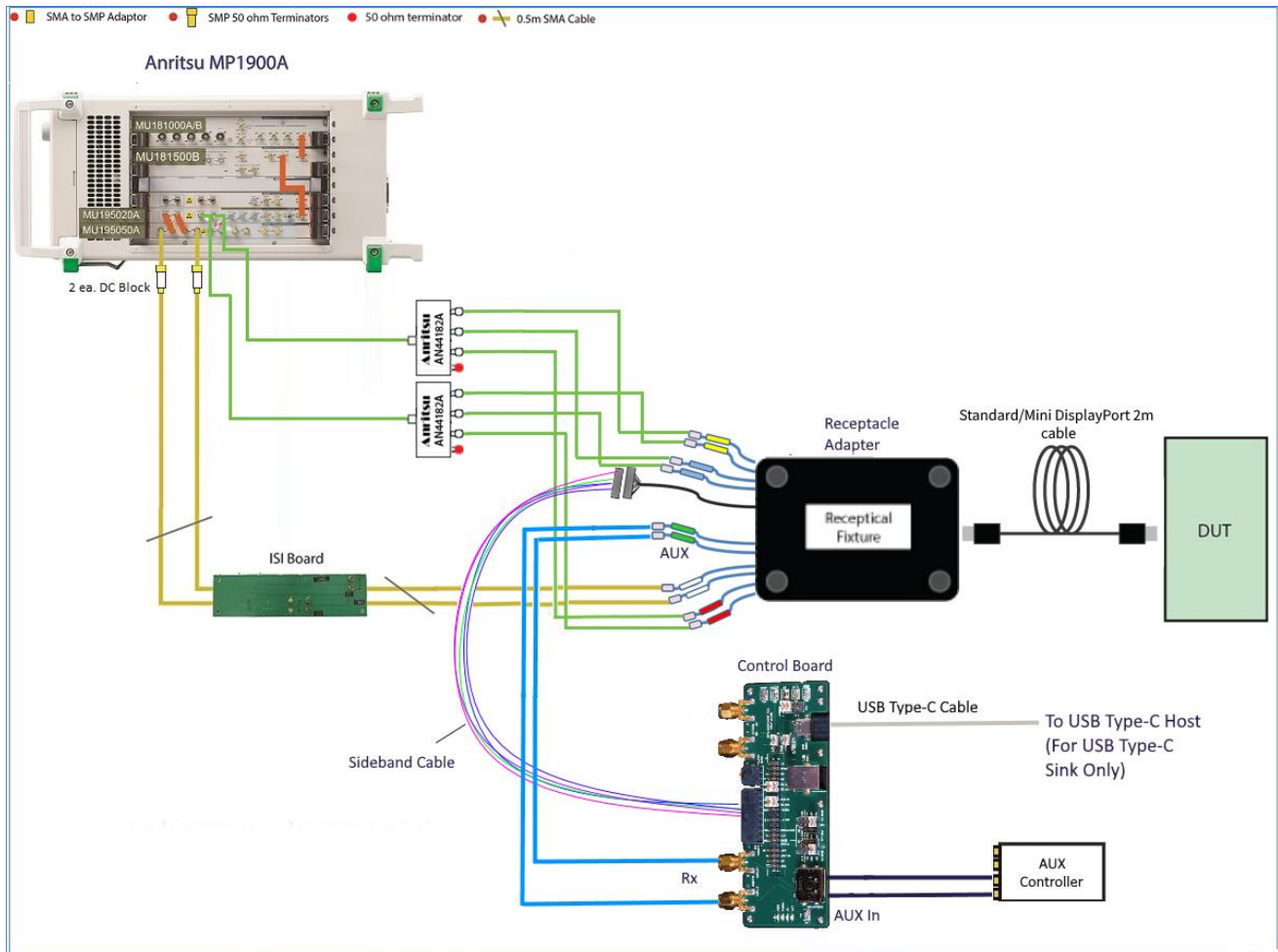


FIGURE 45. STANDARD/MINI DISPLAYPORT MODE BER COMPLIANCE TEST SETUP FOR DP SINK DUT AT TP3_EQ AT 10G

Connection Steps:

1. Using the MP1900A BERT TP3_EQ calibration setup (Section 4.5.3), disconnect the DisplayPort receptacle adapter fixture that connects to the scope.
2. Connect the MU195020A second data outputs through the AN44182A Power Dividers to the Rx lanes of the receptacle adapter fixture that are not under test (for example, at T2_P & T2_N pins, T3_P & T3_N pins, and T1_P & T1_N pins respectively) to inject

crosstalk. *Note: The unused output lanes of the power dividers must be terminated with 50 Ω terminators.*

3. Attach the 2M Standard/Mini DisplayPort cable to the DUT's receptacle connector.
4. Connect the ISI channels to Rx Lane0/Lane1 of the Standard/Mini DisplayPort receptacle adapter (at T0_P and T0_N pins).
5. Connect the green AUX cable pair of the receptacle adapter to the Rx lanes of the DisplayPort 2.1 control board.
6. Connect the low-speed connector cable of the receptacle adapter to the allocated slot on the control board.
7. Connect the AUX controller to power supply.
8. Connect the AUX controller output to the AUX input connector of the control board.
9. Connect the control board to a USB Type-C Host using a USB Type-C cable.
10. Run the AUX controller test scripts from the USB Type-C Host to control the DUT.

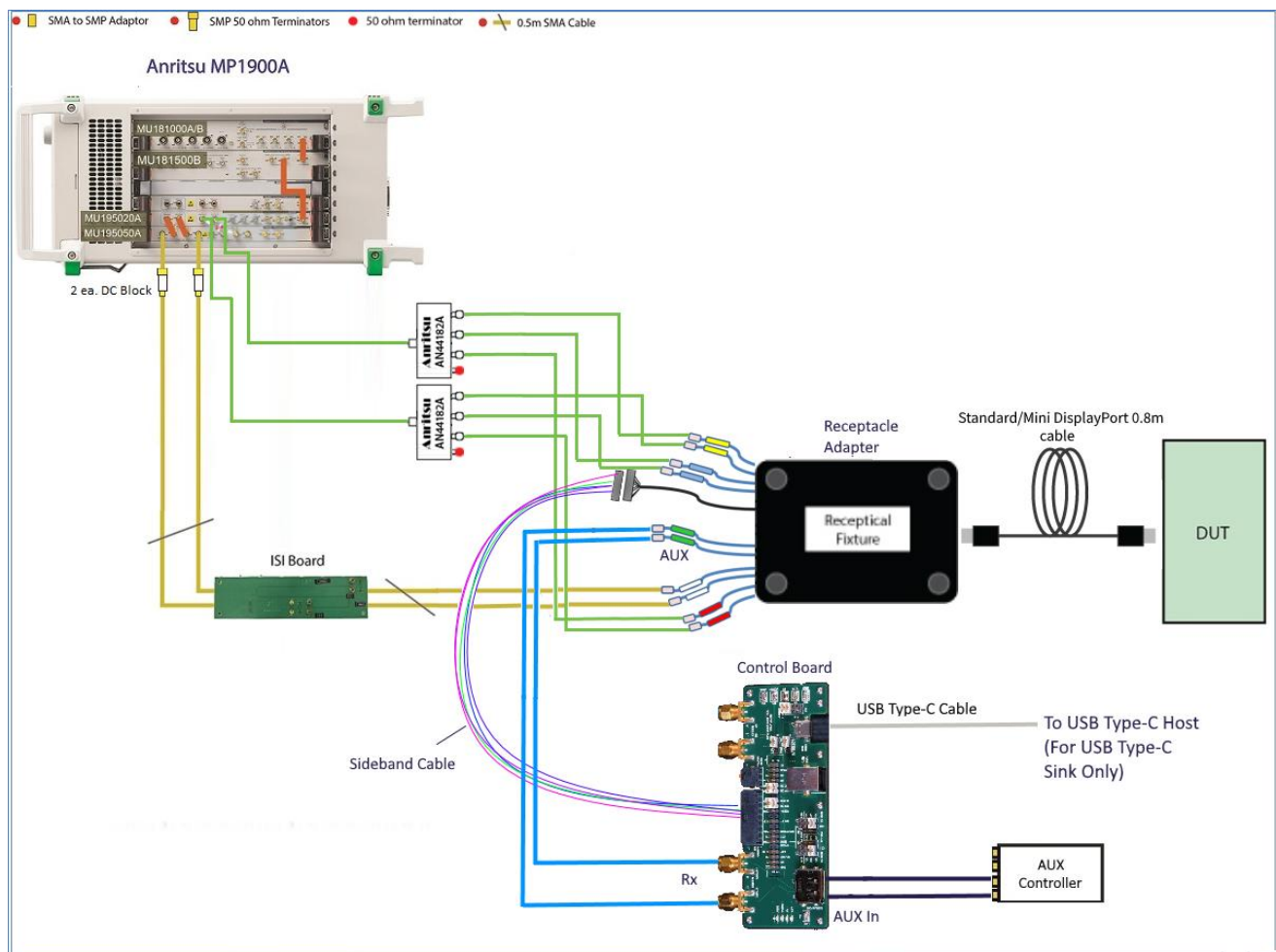


FIGURE 46. STANDARD/MINI DISPLAYPORT MODE BER COMPLIANCE TEST SETUP FOR DP SINK DUT AT TP3_EQ AT 13.5G AND 20G

Connection Step:

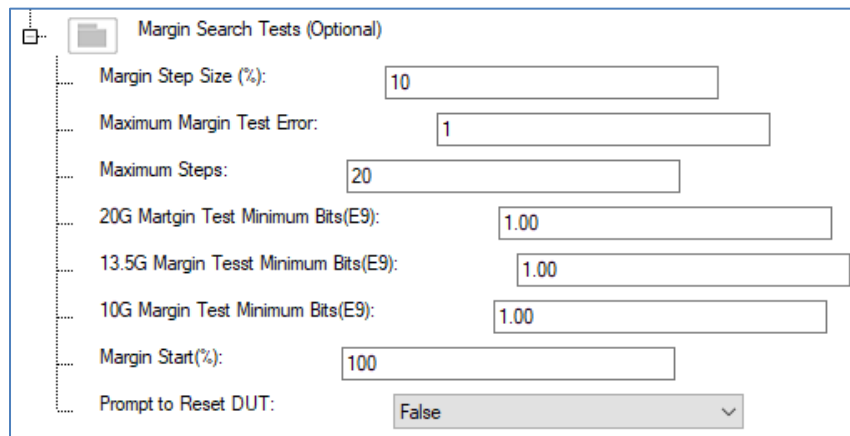
Using the same setup for TP3_EQ at 10G in Figure 45, replace the 2M Standard/Mini DisplayPort cable with the 0.8M Standard/Mini DisplayPort cable to the DUT's receptacle connector.

5.1.5 Margin Testing

While it is sufficient to perform the BER Compliance Test for each test condition to meet compliance specifications, it is also useful to determine how much Margin your design contains.

The Margin for each test condition can be verified as follows:

- In the Configurations  page, set up the following margin test parameters. Refer to Section 3.4 for the description of each parameter.

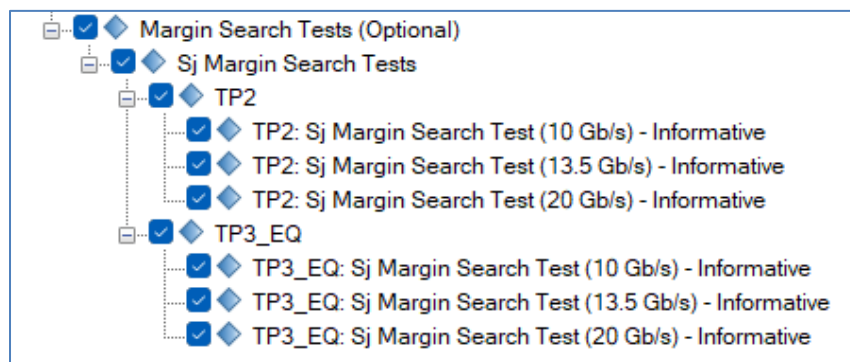


Margin Search Tests (Optional)

Margin Step Size (%):	10
Maximum Margin Test Error:	1
Maximum Steps:	20
20G Margin Test Minimum Bits(E9):	1.00
13.5G Margin Test Minimum Bits(E9):	1.00
10G Margin Test Minimum Bits(E9):	1.00
Margin Start(%):	100
Prompt to Reset DUT:	False

FIGURE 47. MARGIN TEST CONFIGURATION

- Once configured, select and run the “Sink Margin Test” for the test point(s) and data rate(s) as required.



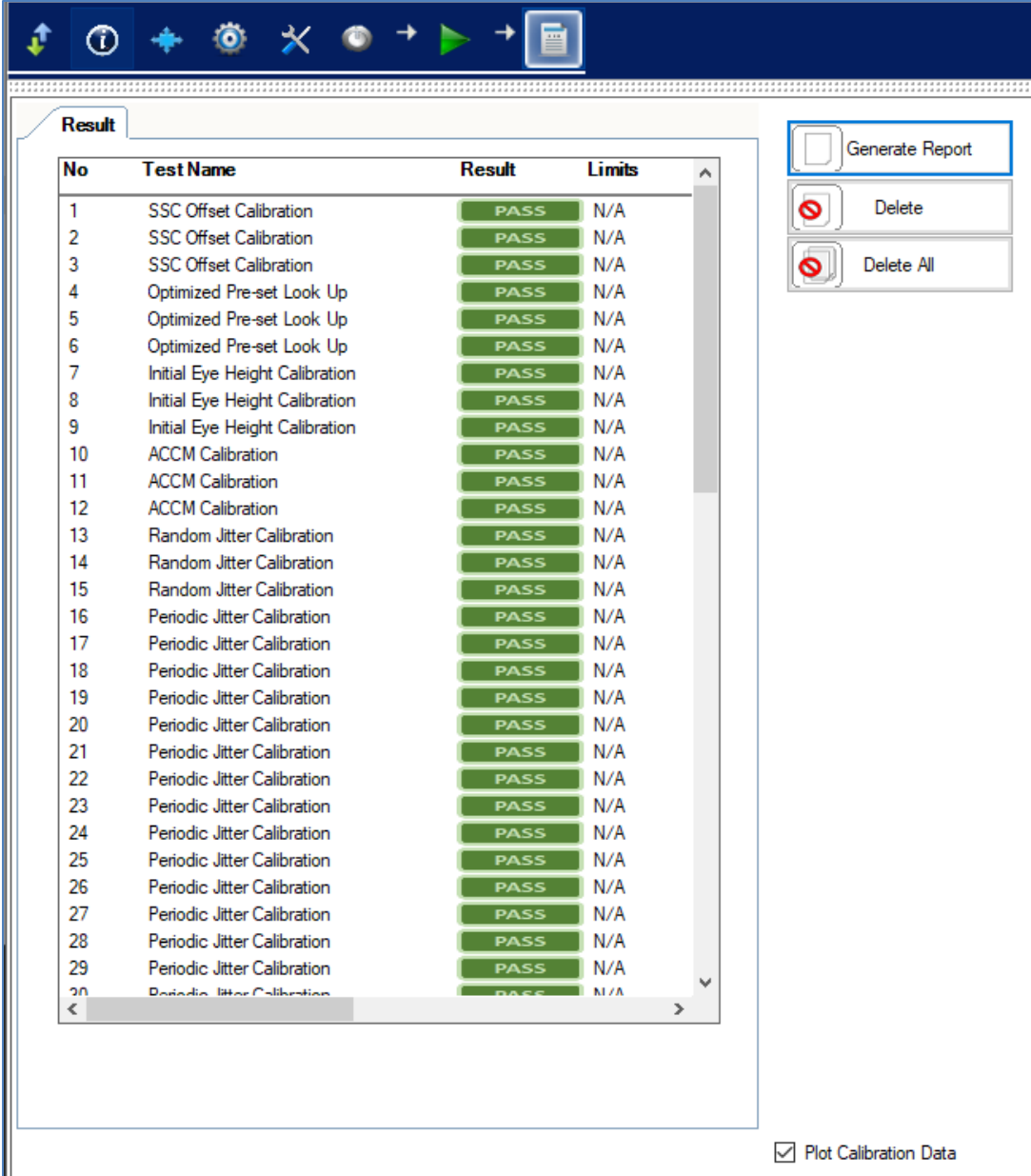
Margin Search Tests (Optional)

- Sj Margin Search Tests
 - TP2
 - TP2: Sj Margin Search Test (10 Gb/s) - Informative
 - TP2: Sj Margin Search Test (13.5 Gb/s) - Informative
 - TP2: Sj Margin Search Test (20 Gb/s) - Informative
 - TP3_EQ
 - TP3_EQ: Sj Margin Search Test (10 Gb/s) - Informative
 - TP3_EQ: Sj Margin Search Test (13.5 Gb/s) - Informative
 - TP3_EQ: Sj Margin Search Test (20 Gb/s) - Informative

FIGURE 48. SINK MARGIN TEST SELECTION

6 Test Results and Reports Using GRL-DP21-SINK-AN

The **Report**  page has all the results from all the test runs displayed. If some of the results are not desired, they can be individually deleted by using the **Delete** button. Also for a PDF report, select the **Generate report** button. To have the calibration data plotted in the report, make sure the **Plot Calibration Data** box is checked.



The screenshot shows the 'Result' tab of the software interface. It features a table with four columns: 'No', 'Test Name', 'Result', and 'Limits'. The table lists 30 test runs, all of which have a 'PASS' result. To the right of the table are three buttons: 'Generate Report', 'Delete', and 'Delete All'. At the bottom right, there is a checkbox labeled 'Plot Calibration Data' which is checked.

No	Test Name	Result	Limits
1	SSC Offset Calibration	PASS	N/A
2	SSC Offset Calibration	PASS	N/A
3	SSC Offset Calibration	PASS	N/A
4	Optimized Pre-set Look Up	PASS	N/A
5	Optimized Pre-set Look Up	PASS	N/A
6	Optimized Pre-set Look Up	PASS	N/A
7	Initial Eye Height Calibration	PASS	N/A
8	Initial Eye Height Calibration	PASS	N/A
9	Initial Eye Height Calibration	PASS	N/A
10	ACCM Calibration	PASS	N/A
11	ACCM Calibration	PASS	N/A
12	ACCM Calibration	PASS	N/A
13	Random Jitter Calibration	PASS	N/A
14	Random Jitter Calibration	PASS	N/A
15	Random Jitter Calibration	PASS	N/A
16	Periodic Jitter Calibration	PASS	N/A
17	Periodic Jitter Calibration	PASS	N/A
18	Periodic Jitter Calibration	PASS	N/A
19	Periodic Jitter Calibration	PASS	N/A
20	Periodic Jitter Calibration	PASS	N/A
21	Periodic Jitter Calibration	PASS	N/A
22	Periodic Jitter Calibration	PASS	N/A
23	Periodic Jitter Calibration	PASS	N/A
24	Periodic Jitter Calibration	PASS	N/A
25	Periodic Jitter Calibration	PASS	N/A
26	Periodic Jitter Calibration	PASS	N/A
27	Periodic Jitter Calibration	PASS	N/A
28	Periodic Jitter Calibration	PASS	N/A
29	Periodic Jitter Calibration	PASS	N/A
30	Periodic Jitter Calibration	PASS	N/A

FIGURE 49. REPORT RESULTS PAGE

6.1.1 DUT Information

This portion is populated from the information in the DUT tab on the **Session Info** page.

Anritsu DisplayPort Sink Test 2.1 Report

DUT Information

DUT Manufacturer : GRL

DUT Model Number : DPSINK21

DUT Serial Number : A0002

DUT Comments :

Test Information

Test Lab : Granite River Labs

Test Operator : David

Test Date : 1 February 2022

Software Version

Software Revision : 0.00.12

FIGURE 50. DUT INFORMATION

6.1.2 Results Summary Table

This portion is populated from the calibration and tests performed with their respective results. This gives an overall view of all the results and test conditions.

No	TestName	Limits	Value	Results	Lane	Test Point	Data Rate	SJ Frequency
1	SSC Offset Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	N/A
2	SSC Offset Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	N/A
3	SSC Offset Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	N/A
4	Optimized Pre-set Look Up	N/A	N/A	Pass	N/A	TP2	Rate_10G	N/A
5	Optimized Pre-set Look Up	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	N/A
6	Optimized Pre-set Look Up	N/A	N/A	Pass	N/A	TP2	Rate_20G	N/A
7	Initial Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	N/A
8	Initial Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	N/A
9	Initial Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	N/A
10	ACCM Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	N/A
11	ACCM Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	N/A
12	ACCM Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	N/A
13	Random Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	N/A
14	Random Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	N/A
15	Random Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	N/A
16	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ1
17	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ2
18	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ3
19	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ4
20	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ5
21	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ6
22	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ1
23	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ2
24	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ3
25	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ4
26	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ5
27	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_13p5G	SJ6
28	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ1
29	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ2
30	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ3
31	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ4
32	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ5
33	Periodic Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_20G	SJ6
34	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ1
35	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate_10G	SJ2

No	TestName	Limits	Value	Results	Lane	Test Point	Data Rate	SJ Frequency
36	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate 10G	SJ3
37	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate 10G	SJ4
38	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate 10G	SJ5
39	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate 10G	SJ6
40	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate 13p5G	SJ1
41	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate 13p5G	SJ2
42	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate 13p5G	SJ3
43	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate 13p5G	SJ4
44	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate 13p5G	SJ5
45	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate 13p5G	SJ6
46	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate 20G	SJ1
47	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate 20G	SJ2
48	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate 20G	SJ3
49	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate 20G	SJ4
50	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate 20G	SJ5
51	TP1, Total Jitter Calibration	N/A	N/A	Pass	N/A	TP2	Rate 20G	SJ6
52	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 10G	SJ1
53	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 10G	SJ2
54	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 10G	SJ3
55	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 10G	SJ4
56	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 10G	SJ5
57	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 10G	SJ6
58	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 13p5G	SJ1
59	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 13p5G	SJ2
60	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 13p5G	SJ3
61	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 13p5G	SJ4
62	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 13p5G	SJ5
63	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 13p5G	SJ6
64	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 20G	SJ1
65	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 20G	SJ2
66	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 20G	SJ3
67	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 20G	SJ4
68	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 20G	SJ5
69	TP1, Eye Height Calibration	N/A	N/A	Pass	N/A	TP2	Rate 20G	SJ6
70	Crosstalk Calibration	N/A	N/A	Pass	N/A	N/A	Rate 10G	N/A
71	Crosstalk Calibration	N/A	N/A	Pass	N/A	N/A	Rate 13p5G	N/A
72	Crosstalk Calibration	N/A	N/A	Pass	N/A	N/A	Rate 20G	N/A
73	Optimized EQ Look Up	N/A	N/A	Pass	N/A	TP3	Rate 13p5G	N/A
74	TP3, EQ, Eye Height Calibration	N/A	N/A	Pass	N/A	TP3	Rate 13p5G	SJ5

FIGURE 51. RESULTS SUMMARY TABLE EXAMPLE

6.1.3 Calibration & Test Result Details

This portion is populated with results from each of the calibration and test runs. Here the results are explained in depth with supporting data points and screenshots. If the Plot Calibration Data checkbox is selected, then the plots are also displayed.

74. TP3_EQ, Eye Height Calibration [TP3_EQ,Rate_13p5G,SJ5]

Pass/Fail Stats	: Pass
Cal Parameter	: Final Eye Height_Rate_13p5G_TP3_SJ5
Settings Parameter	: Eye Amplitude
Settings	: 1060.0000 mV
Measured Parameter	: Eye Height
Measured Value	: 106.0000 mV
Sj Frequency	: 50.0000 MHz
Test completed time	: 23 December 2021 16:03:11 PM

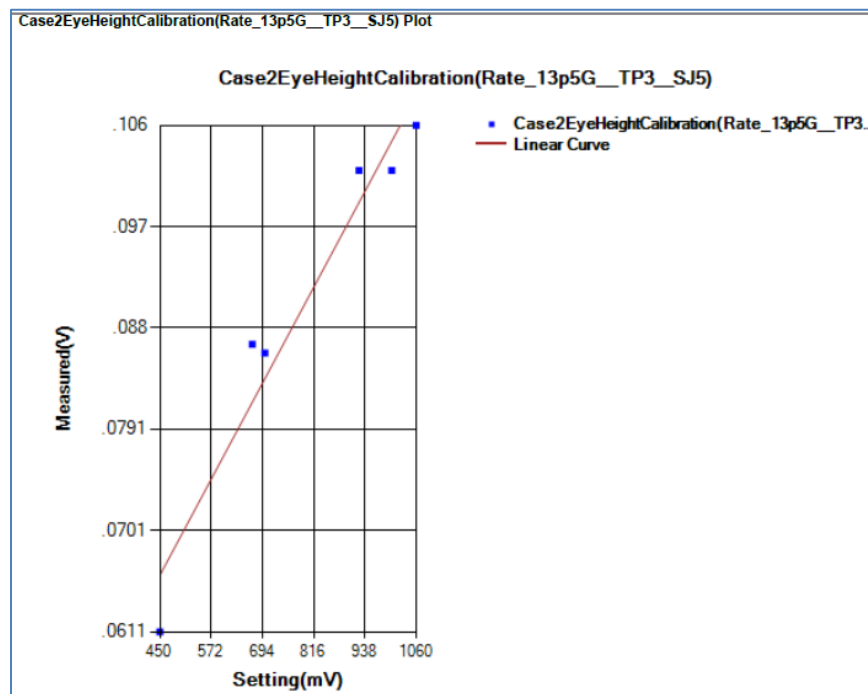
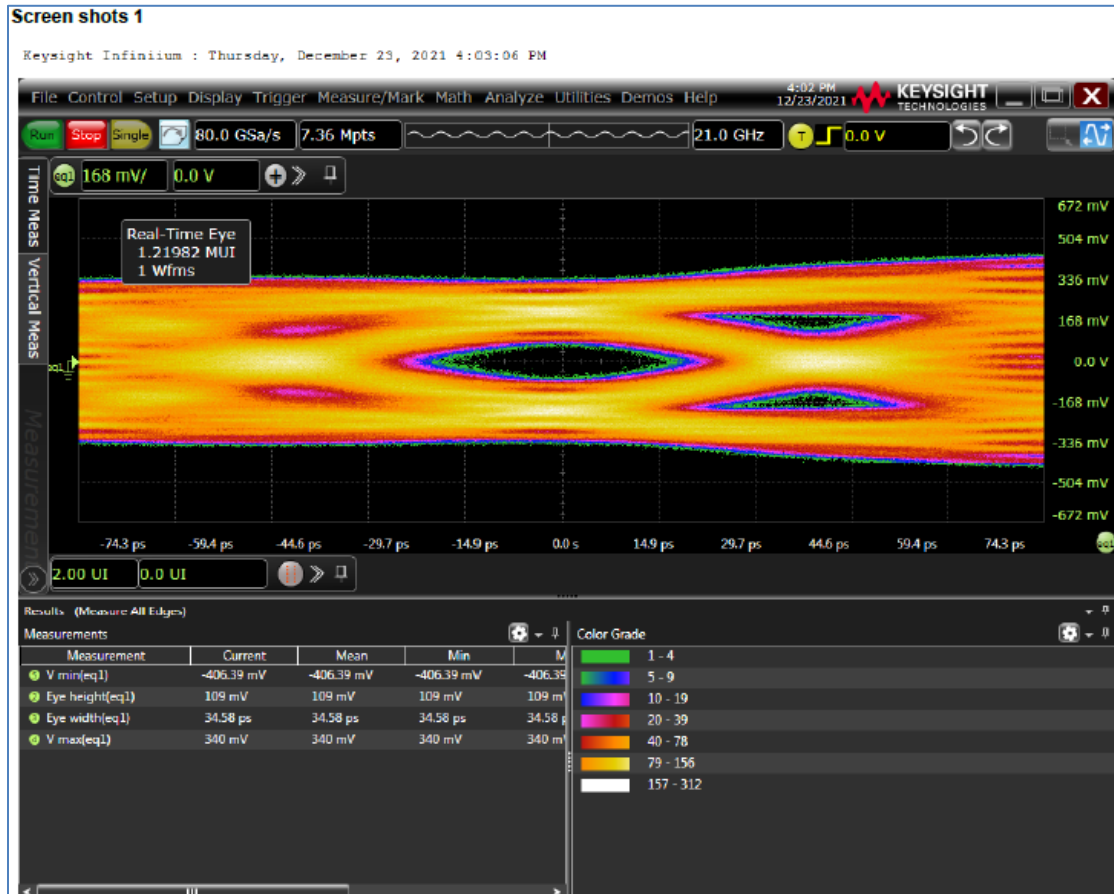


FIGURE 52. CALIBRATION/TEST RESULT DETAILS EXAMPLE

6.2 Delete Test Results

If some of the results are not desired, they can be individually deleted by selecting the **Delete** button.

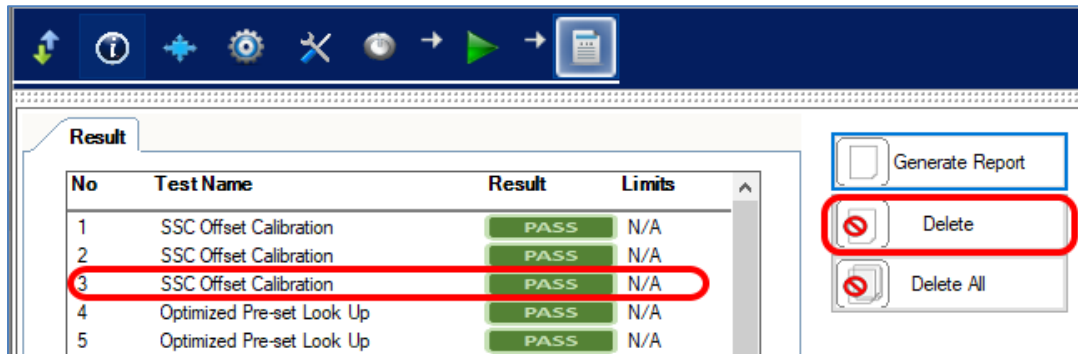


FIGURE 53. DELETE INDIVIDUAL CALIBRATION/TEST RESULTS EXAMPLE

To remove all results, select the **Delete All** button.

7 Saving and Loading Test Sessions

The GRL-DP21-SINK-AN software enables Calibration and Test Results to be created and maintained as a ‘Live Session’ in the application. This allows you to quit the application and return later to continue where you left off.

Save and Load Sessions are used to Save a Test Session that you may want to recall later. You can ‘switch’ between different sessions by Saving and Loading them when needed.

To save a session, with all of the parameter information, the test results, and any waveforms, use the “Options” command on the menu bar, then the “Save Session” command.

To load a session back into the software, including the saved parameter settings, use the “Options” command on the menu bar, then the “Load Session” command.

To create a New session and return the application back to a default configuration, use “Options” command on the menu bar, then the “New Session” command.

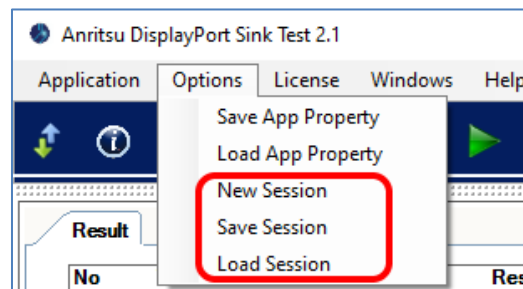


FIGURE 54. SAVING AND LOADING CALIBRATION AND TEST SESSIONS

The configuration and session results are saved in a file with the extension ‘.ses’, which is a compressed zip-style file, containing a variety of information.

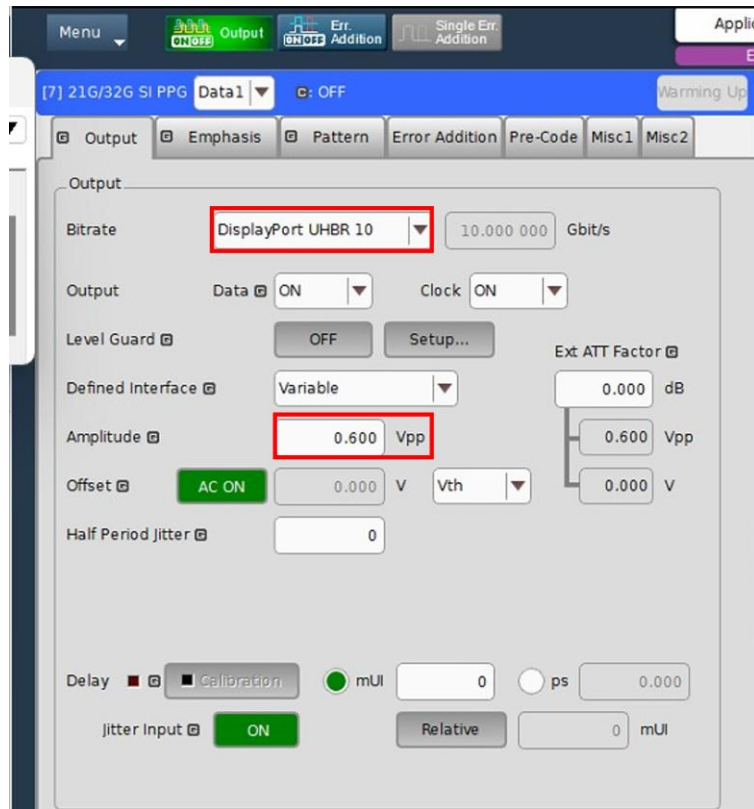
8 Appendix A: Manual CTS Sink Calibration and Test Procedure

The DisplayPort 2.1 PHY CTS outlines the requirements for manual DisplayPort 2.1 PHY CTS UHBRx Sink Calibration and Testing in this section.

Note: See Section 2, Resource Requirements for equipment required in the following setups.

8.1 Preset Calibration for UHBR10, UHBR13.5 and UHBR20

1. Set up the physical equipment connections, as per Figure 34.
2. Set up the MP1900A BERT as follows:
 - a) Go to Menu Bar → File → Initialize.
 - b) Go to PPG → Output.
 - c) Set Bitrate to “DisplayPort UHBR 10” (using 10G as example) and set Amplitude to 0.6 Vpp. See Figure 69.
 - d) Set Test Pattern on PPG to “Data” and Length to “128” bits (64 1s and 64 0s) to output SQ64 pattern. See Figure 56.
 - e) Turn on PPG Data Output.
 - f) Go to PPG → Emphasis tab.
 - g) Turn on “Manual Setting” and set Standard/Preset pattern to “USER”, “De-Emphasis”. See Figure 57.
 - h) Go to Jitter Modulation Source tab and turn off SJ1, SJ2, SSC, BUJ, RJ and Ext. See Figure 69.
 - i) Go to Noise Generator tab and turn off the CM. See Figure 70.



Menu Output Err. Addition Single Err. Addition Applic

[7] 21G/32G SI PPG Data1 c: OFF Warming Up

Output Emphasis Pattern Error Addition Pre-Code Misc1 Misc2

Output

Bitrate DisplayPort UHBR 10 10.000 000 Gbit/s

Output Data ON Clock ON

Level Guard OFF Setup... Ext ATT Factor 0.000 dB

Defined Interface Variable 0.600 Vpp

Amplitude 0.600 Vpp

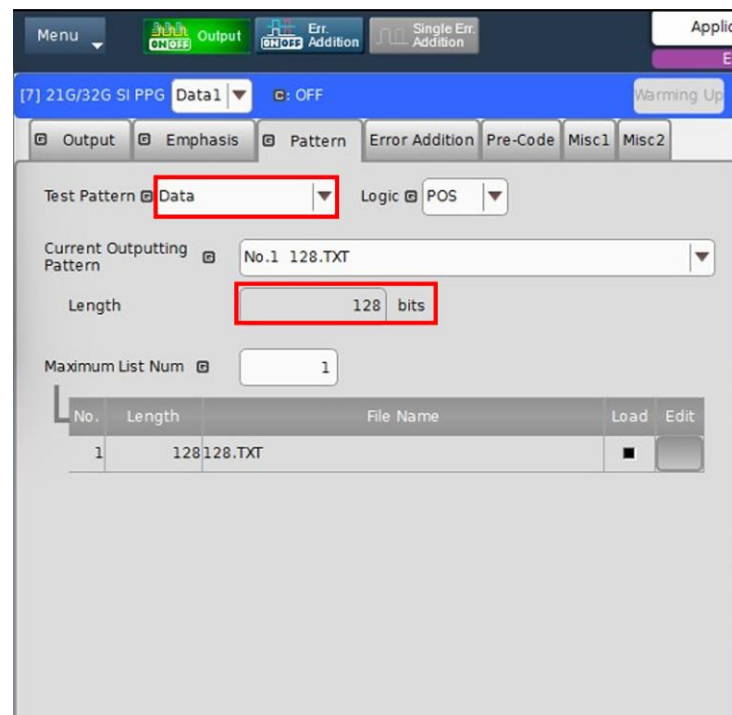
Offset AC ON 0.000 V Vth 0.000 V

Half Period Jitter 0

Delay Calibration mUI 0 ps 0.000

Jitter Input ON Relative 0 mUI

FIGURE 55. PPG OUTPUT SETTING



Menu Output Err. Addition Single Err. Addition Applic

[7] 21G/32G SI PPG Data1 c: OFF Warming Up

Output Emphasis Pattern Error Addition Pre-Code Misc1 Misc2

Test Pattern Data Logic POS

Current Outputting Pattern No.1 128.TXT

Length 128 bits

Maximum List Num 1

No.	Length	File Name	Load	Edit
1	128	128.TXT	☐	☐

FIGURE 56. PATTERN SETTING

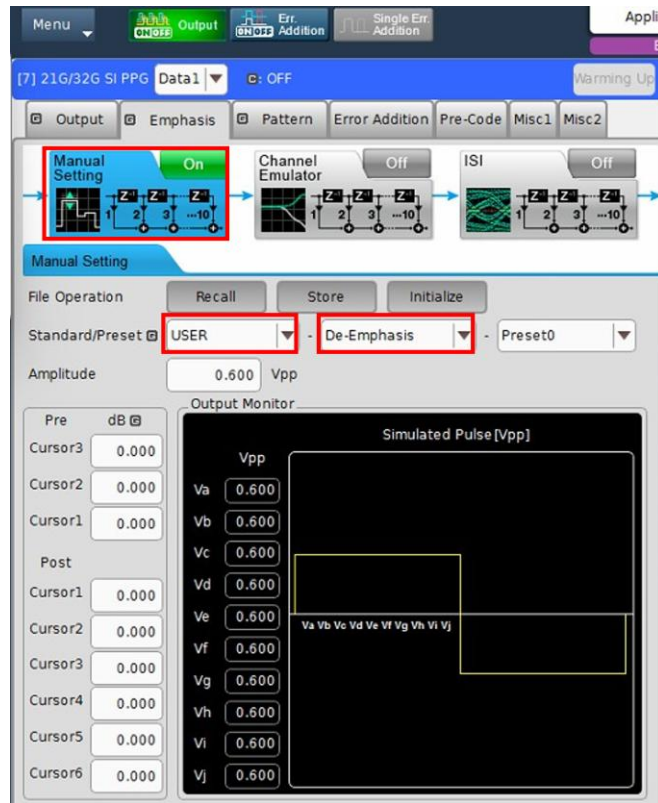


FIGURE 57. PPG EMPHASIS SETTING

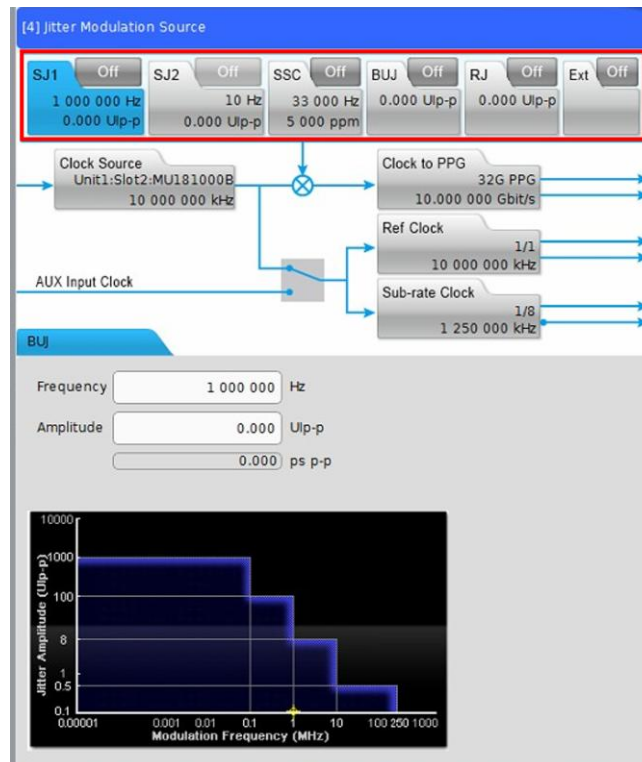


FIGURE 58. JITTER SOURCE SETTING

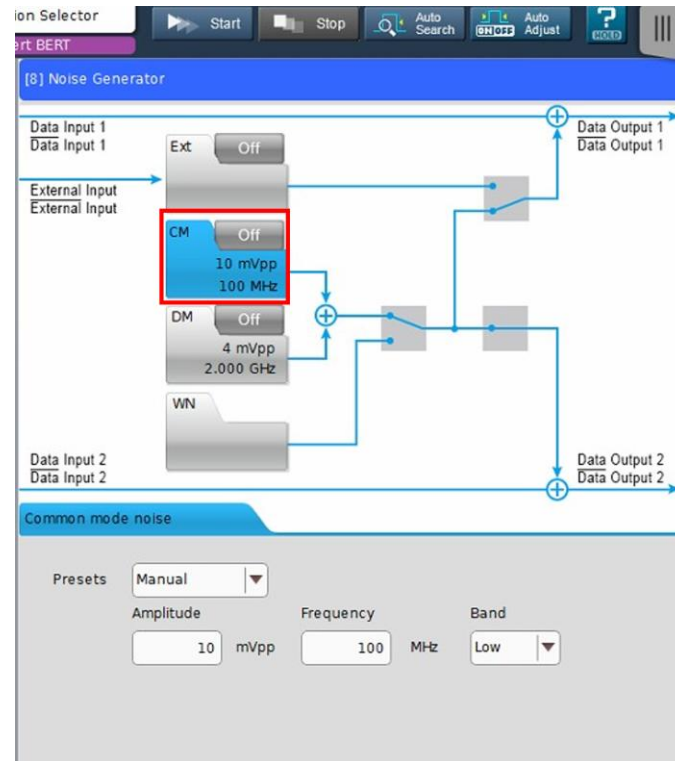


FIGURE 59. CM SETTING

8.1.1 Set Up Oscilloscope

8.1.1.1 Keysight Oscilloscope Vertical and Horizontal Setup

Set up the Keysight Scope as listed in Table 9.

TABLE 5. KEYSIGHT OSCILLOSCOPE VERTICAL AND HORIZONTAL SETUP

Setting	Setup
Vertical	Ch1-Ch3 (using the full range of the Scope's D/A)
Record Length	12.5 M in a single acquisition
Sample Rate	80Gs/s
Averaging	ON (Average of 150 cycles)
Sample Mode	Real Time
Bandwidth	16GHz (UHBR10) / 21GHz (UHBR13.5) / 21GHz (UHBR20)
Vertical Scale	Set to full screen without clipping
Sin x/x	OFF



FIGURE 60. KEYSIGHT OSCILLOSCOPE VERTICAL AND HORIZONTAL SETUP

8.1.1.2 Tektronix Oscilloscope Setup

Set up the Tektronix Scope as listed in Table 9.

TABLE 6. TEKTRONIX OSCILLOSCOPE SETUP

Setting	Setup
Vertical	Math 1 (Ch1-Ch3)
Record Length	12.5M in a single acquisition
Sample Rate	100Gs/s
Averaging	ON (Average of 150 cycles)
Sample Mode	Real Time
Bandwidth	16GHz (UHBR10) / 21GHz (UHBR13.5) / 21GHz (UHBR20)
Vertical Scale	Set to full screen without clipping
Sin x/x	OFF

8.1.1.3 Keysight or Tektronix Oscilloscope Histogram Setup

Set up the Scope as listed in Table 9.

TABLE 7. KEYSIGHT OR TEKTRONIX OSCILLOSCOPE HISTOGRAM SETUP

Setting	Setup
UI	10Gbps 100ps (UHBR10) / 13.5Gbps 74ps (UHBR13.5) / 20Gbps 50ps (UHBR20)
Amplitude Voltage	Measure differential amplitude of bits 57 and 62 (64 bits of 1s) – differential amplitude of bits 57 and 62 (64 bits of 0s)

8.1.2 Record Preset Measurements

1. In the Emphasis tab, create 15 Presets with Deemphasis which match the Table in the DisplayPort 2.1 Specification. On the BERT, go to the PPG Emphasis tab and set the DUT preset to 0. See Figure 61 below.
2. Measure the differential amplitude voltage:
 - a) For DUT Configuration (1) – Enable Preshoot, Deemphasis and measure differential amplitude voltage of bits 57-62 ($|V_{bits(57-62)}|$ (64 bits of 1s) – $V_{bits(57-62)}$ (64 bits of 0s)); mark it as V1.
 - b) For DUT Configuration (2) – Set Preshoot to 0 as disabled and enable Deemphasis. Measure differential amplitude voltage of bits 57-62 ($|V_{bits(57-62)}|$ (64 bits of 1s) – $V_{bits(57-62)}$ (64 bits of 0s)); mark it as V2.
 - c) For DUT Configuration (3) – Enable Preshoot and set Deemphasis to 0 as disabled. Measure differential amplitude voltage of bits 57-62 ($|V_{bits(57-62)}|$ (64 bits of 1s) – $V_{bits(57-62)}$ (64 bits of 0s)); mark it as V3.
3. Calculate Preshoot to be $20 * \log_{10} \left(\frac{V_2}{V_1} \right)$
4. Calculate Deemphasis be $20 * \log_{10} \left(\frac{V_2}{V_1} \right)$
5. Gradually adjust the Preshoot, Deemphasis and confirm whether the measured value minus the Spec value is less than or equal to +/- 0.3 dB. When this condition is fulfilled, record them and calculate their corresponding coefficient values. Then repeat the above steps until preset0~preset15 of all data rates (UHBR10, UHBR13.5, UHBR20) are calculated.

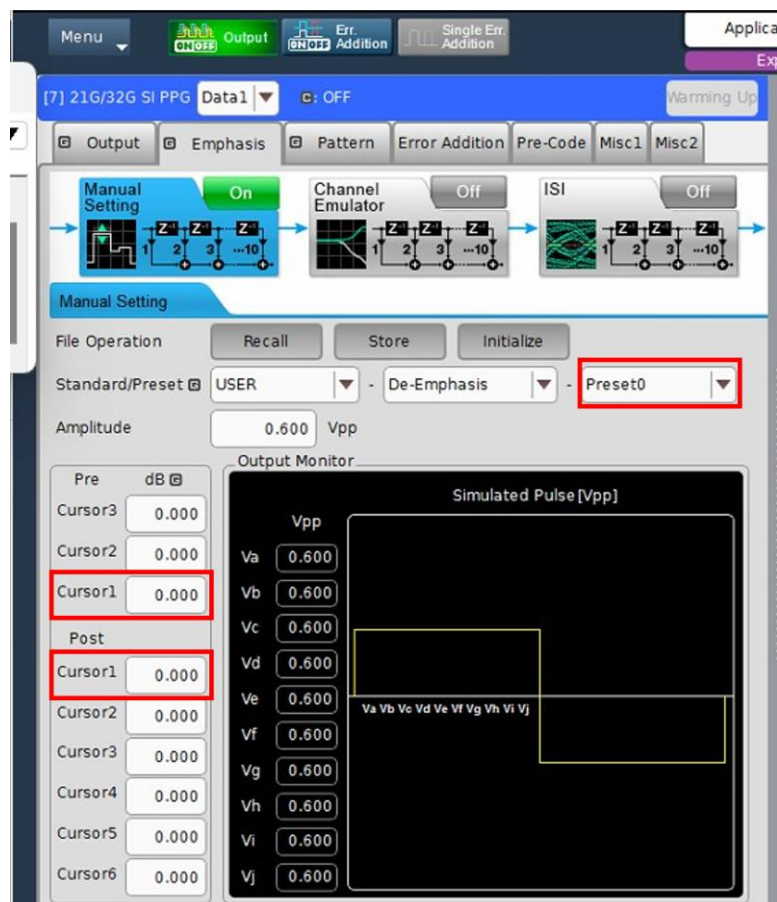


FIGURE 61. EMPHASIS CH1 INTERFACE

6. Table 8 below describes the Deemphasis configuration.

TABLE 8. DEEMPHASIS CONFIGURATION

Setting	Setup
Deemphasis Configuration (1)	Preshoot Enabled, Deemphasis Enabled. See Figure 62.
Deemphasis Configuration (2)	Preshoot Disabled, Deemphasis Enabled. See Figure 63.
Deemphasis Configuration (3)	Preshoot Enabled, Deemphasis Disabled. See Figure 64.

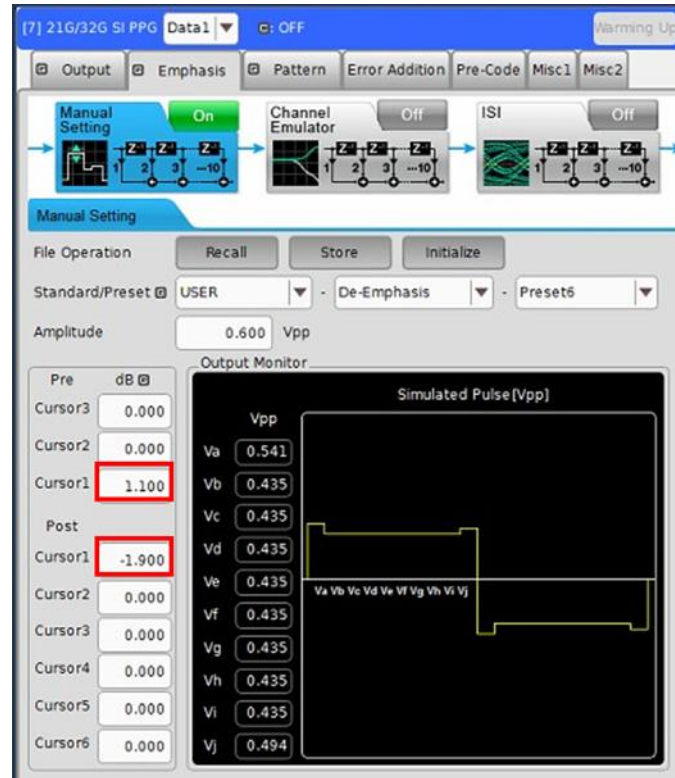


FIGURE 62. DEEMPHASIS CONFIGURATION (1)

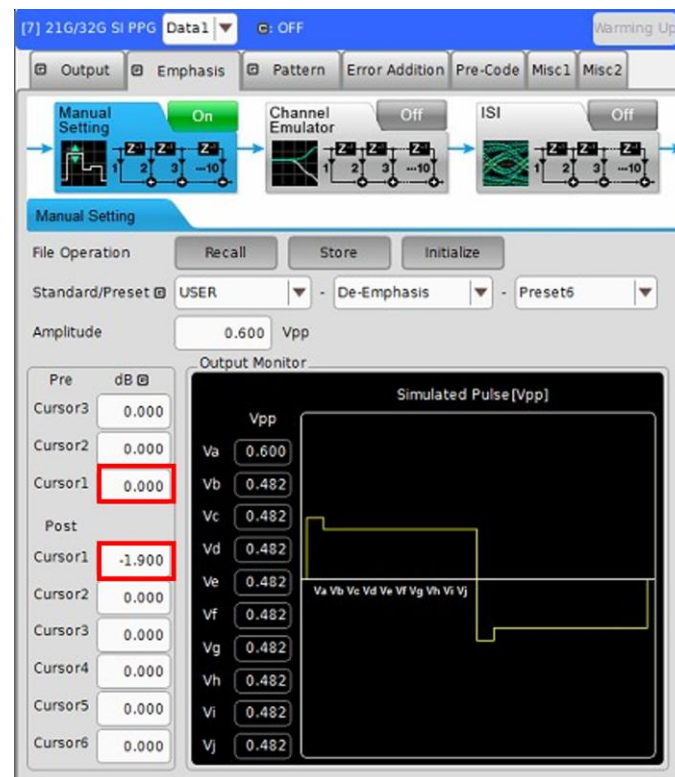


FIGURE 63. DEEMPHASIS CONFIGURATION (2)

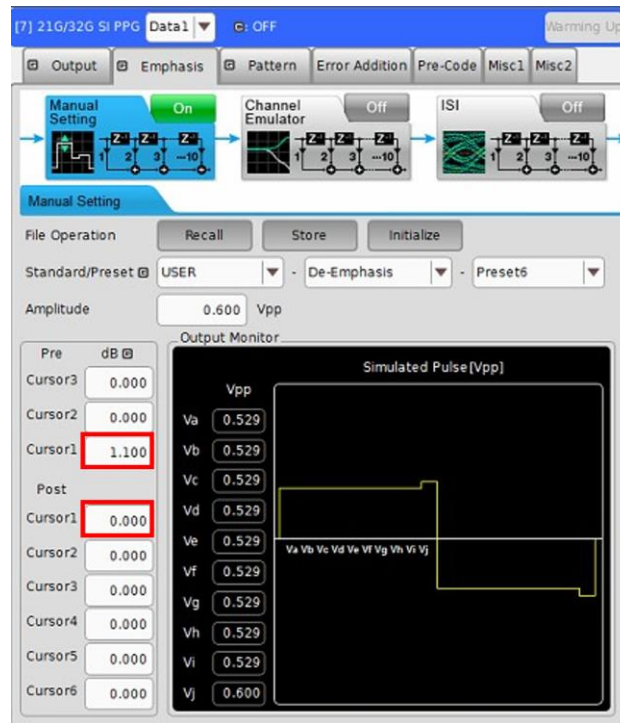


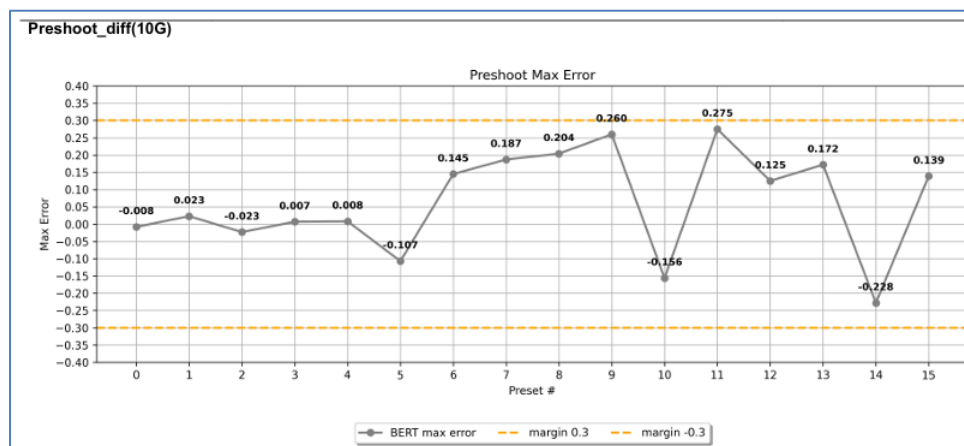
FIGURE 64. DEEMPHASIS CONFIGURATION (3)

7. The following results summary table is populated from the calibration and tests performed with their respective results. This gives an overall view of all the results and test conditions.

No	TestName	Limits	Value	Results	Lane	Test Point	Data Rate	SJ Frequency
1	Preset Calibration	N/A	N/A	Pass	N/A	N/A	UHBR10	N/A
2	Preset Calibration	N/A	N/A	Pass	N/A	N/A	UHBR13.5	N/A
3	Preset Calibration	N/A	N/A	Pass	N/A	N/A	UHBR20	N/A

FIGURE 65. RESULTS SUMMARY TABLE EXAMPLE

When you click on the “Generate Report” button, you can view the results of each calibration and test run in the report along with correlated trace plots.



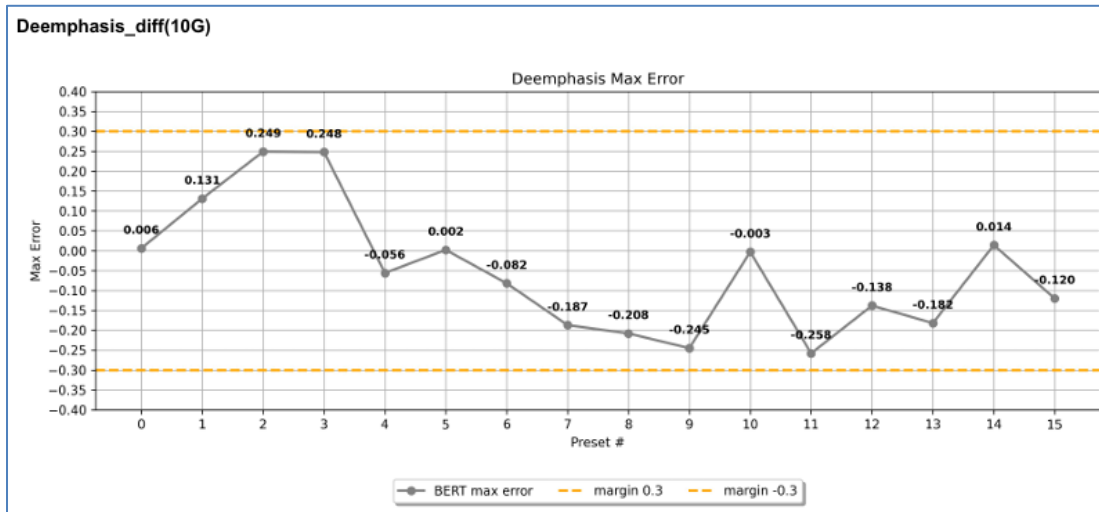


FIGURE 66. 10G PRESHOOT AND DEEMPHASIS PRESET CALIBRATION RESULT DIAGRAM EXAMPLE

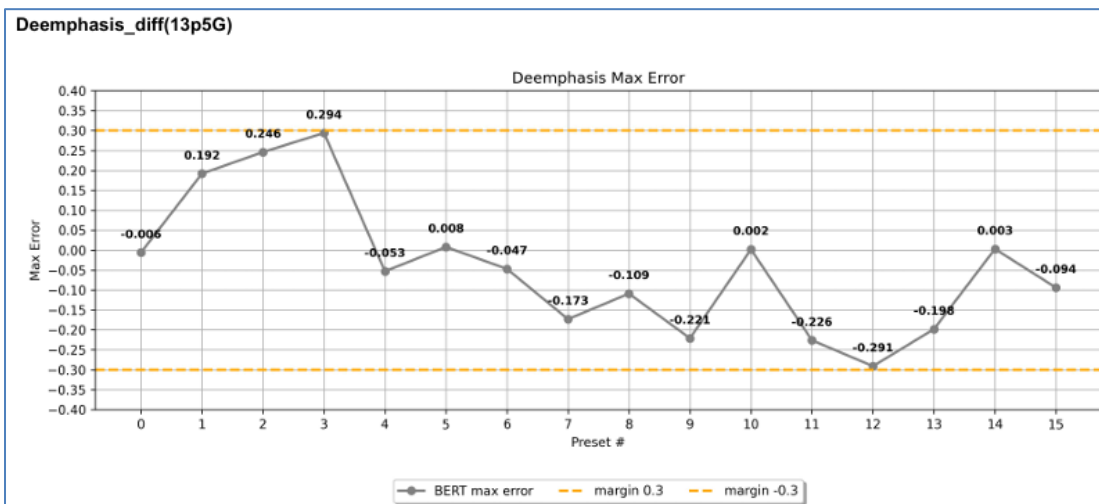
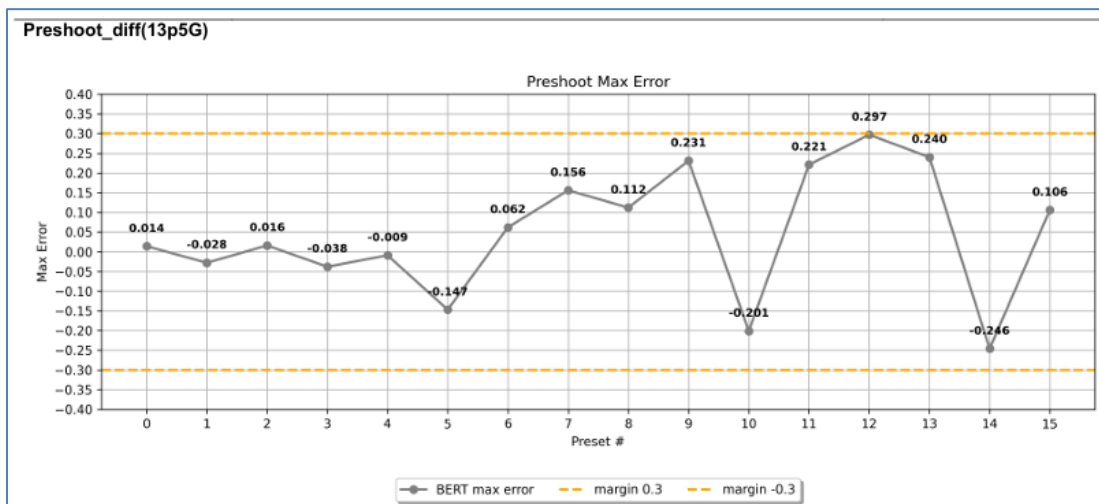


FIGURE 67. 13p5G PRESHOOT AND DEEMPHASIS PRESET CALIBRATION RESULT DIAGRAM EXAMPLE

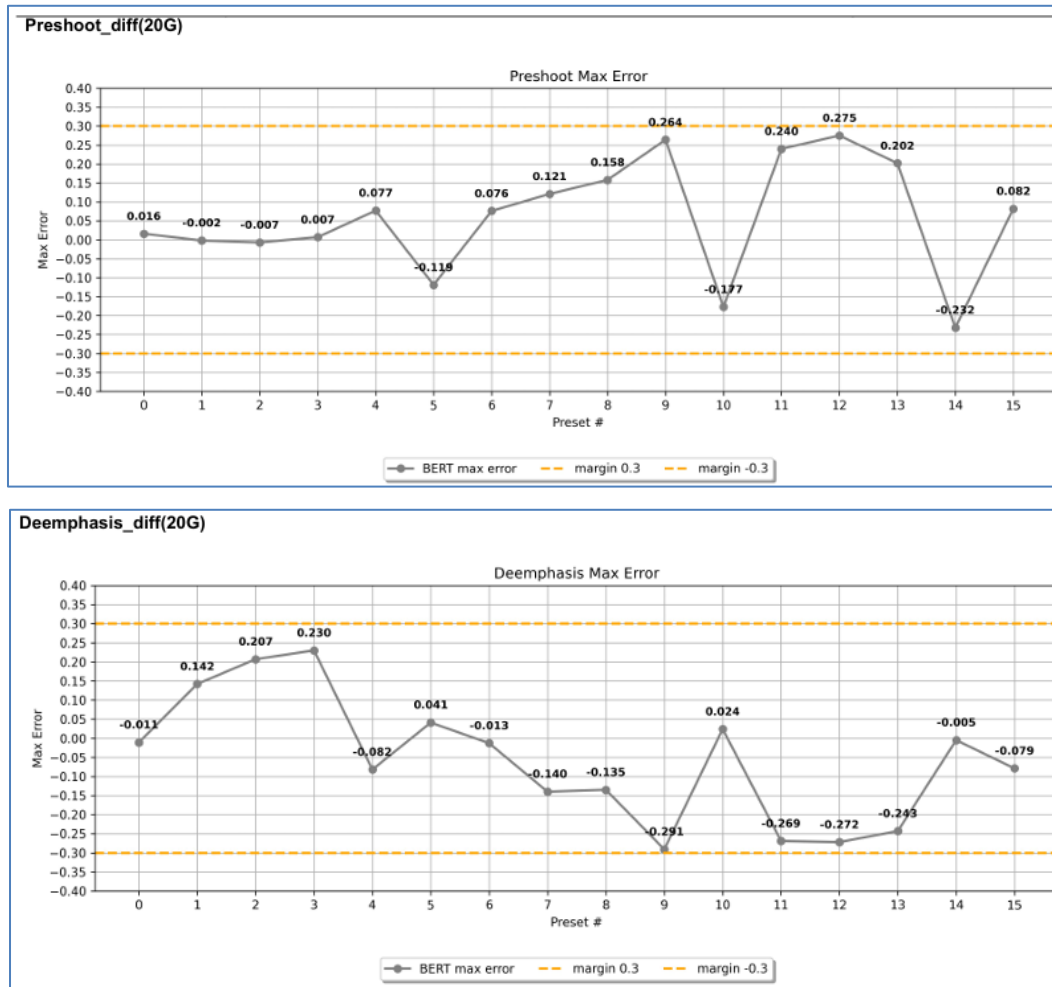


FIGURE 68. 20G PRESBOOT AND DEEMPHASIS PRESET CALIBRATION RESULT DIAGRAM EXAMPLE

8.2 Calibrate Receiver Stressed Eye for UHBR10 (10.0 Gbit/s) at TP1

1. Set up the physical equipment connections without the ISI channel, as per Figure 34.
2. Set up the MP1900A BERT as follows:
 - a) Go to Menu Bar → File → Initialize.
 - b) Go to Jitter tab and set Clock Source to “Unit1:Slot2:MU181000B”. See Figure 69.
 - c) Go to PPG → Misc2.
 - d) Set Clock Source to “Unit1:Slot4:MU181500B”. See Figure 70.
 - e) Set Bit Rate to 10Gbit/s. See Figure 70.
 - f) Set Offset (ppm) to 300ppm for 10G. See Figure 70.
 - g) Set Output Clock Rate to “Fullrate”. See Figure 70.
 - h) Set Test Pattern on PPG to “PRBS” and Length to “2¹⁵-1” bits. See Figure 71.
 - i) Turn on PPG Data Output.
 - j) Go to PPG → Emphasis tab and turn on “Manual Setting”. See Figure 72.
 - k) Turn on “SSC”, with settings of 33kHz (for 10G) with 5300ppm (for 10G) triangle down spread. (SSC will remain ON for all of the following steps.) See Figure 73.

- l) Set DATA+ amplitude to 620mV. A differential amplitude just over the 700mV EH should show as an initial value. (See the lower left in Figure 74.)
- m) Set initial CM frequency to 400MHz. See Figure 75.
- n) Turn the CM output to “Off” until the CM Calibration Step.

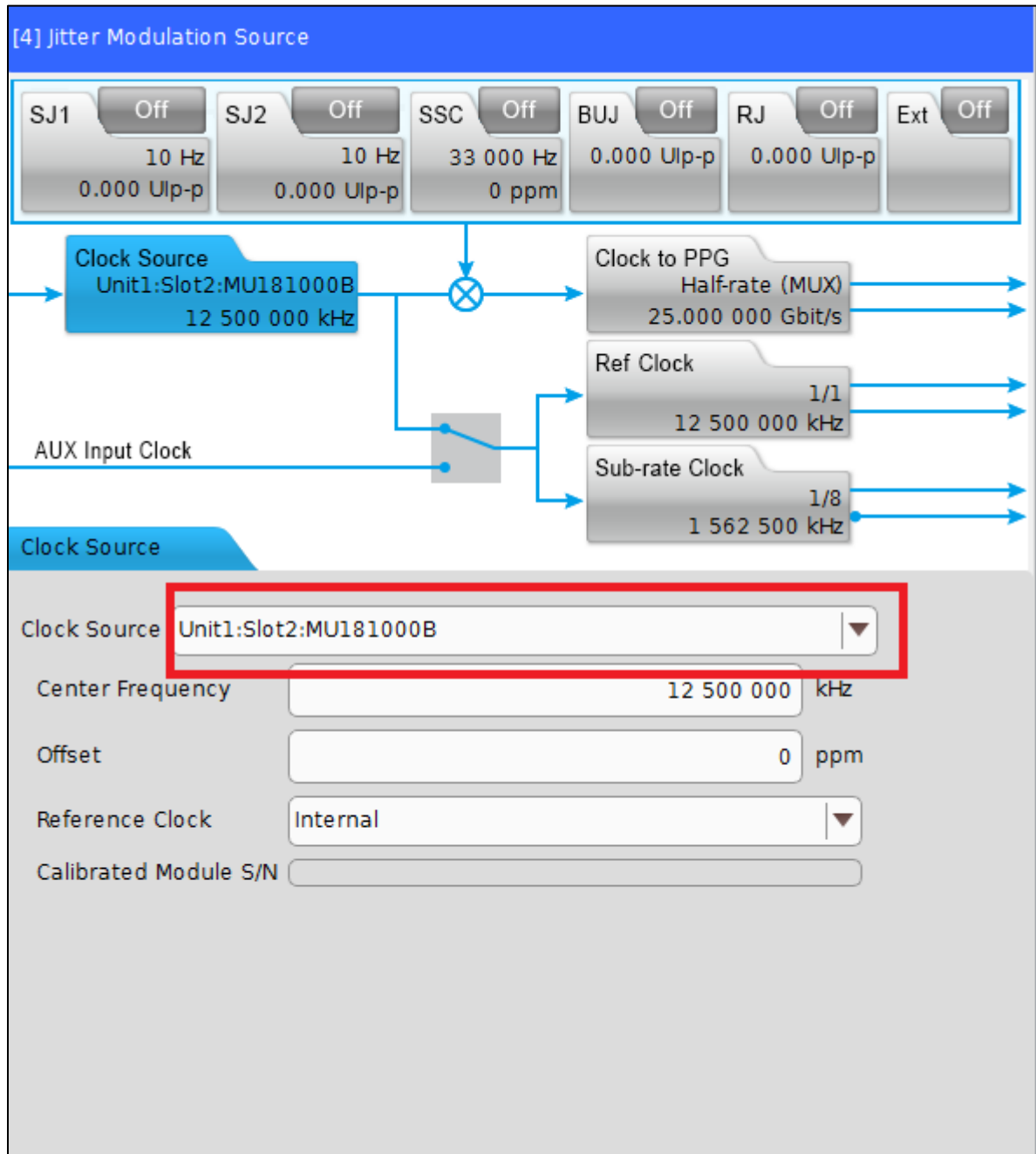


FIGURE 69. JITTER CLOCK SOURCE SETTING

[7] 21G/32G SI PPG Data1 ▼ OFF

Output Emphasis Pattern Error Addition Misc1 Misc2

Clock Setting

Clock Source

Unit1:Slot4:MU181500B ▼

Bit Rate

Variable ▼

10 Gbit/s

Output Clock Rate

Fullrate ▼

Offset

300 ppm

Reference Clock

Internal ▼

Noise Setting

Noise Generator

Not use ▼

Offset

0.000 dB

FIGURE 70. PPG Misc2 SETTINGS

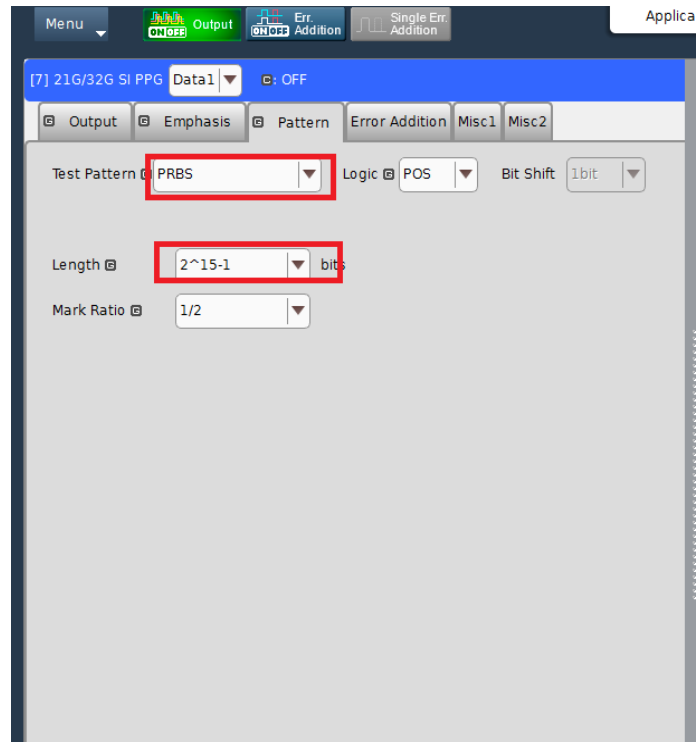


FIGURE 71. PATTERN SETTING

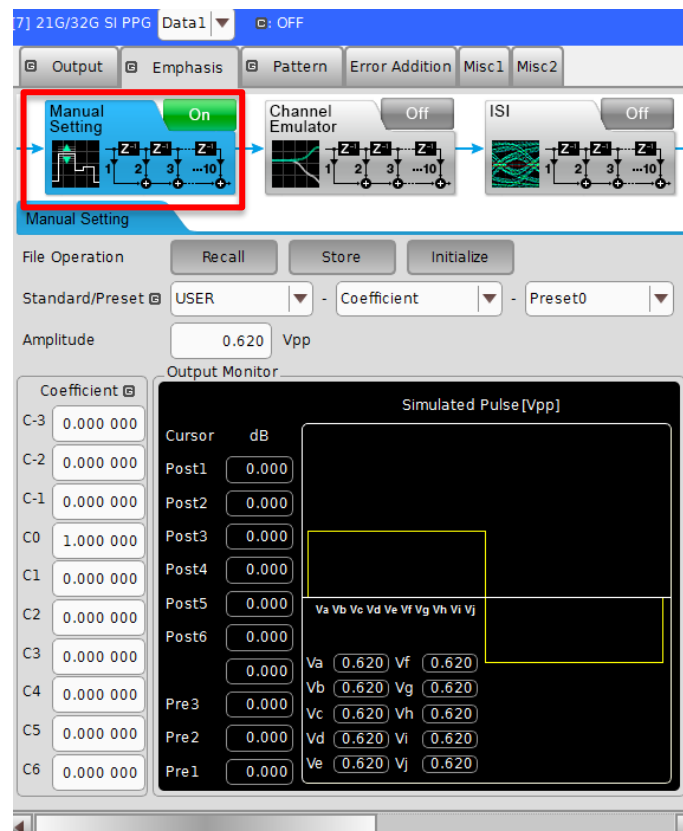


FIGURE 72. PPG EMPHASIS SETTING

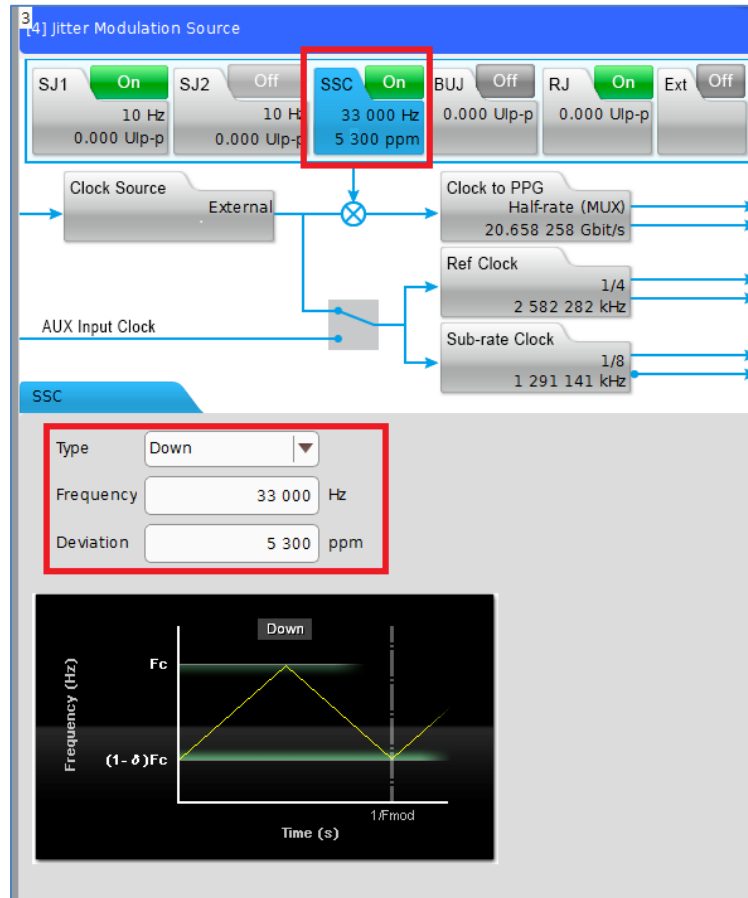


FIGURE 73. SSC SETUP



FIGURE 74. DATA+ AMPLITUDE SETTING

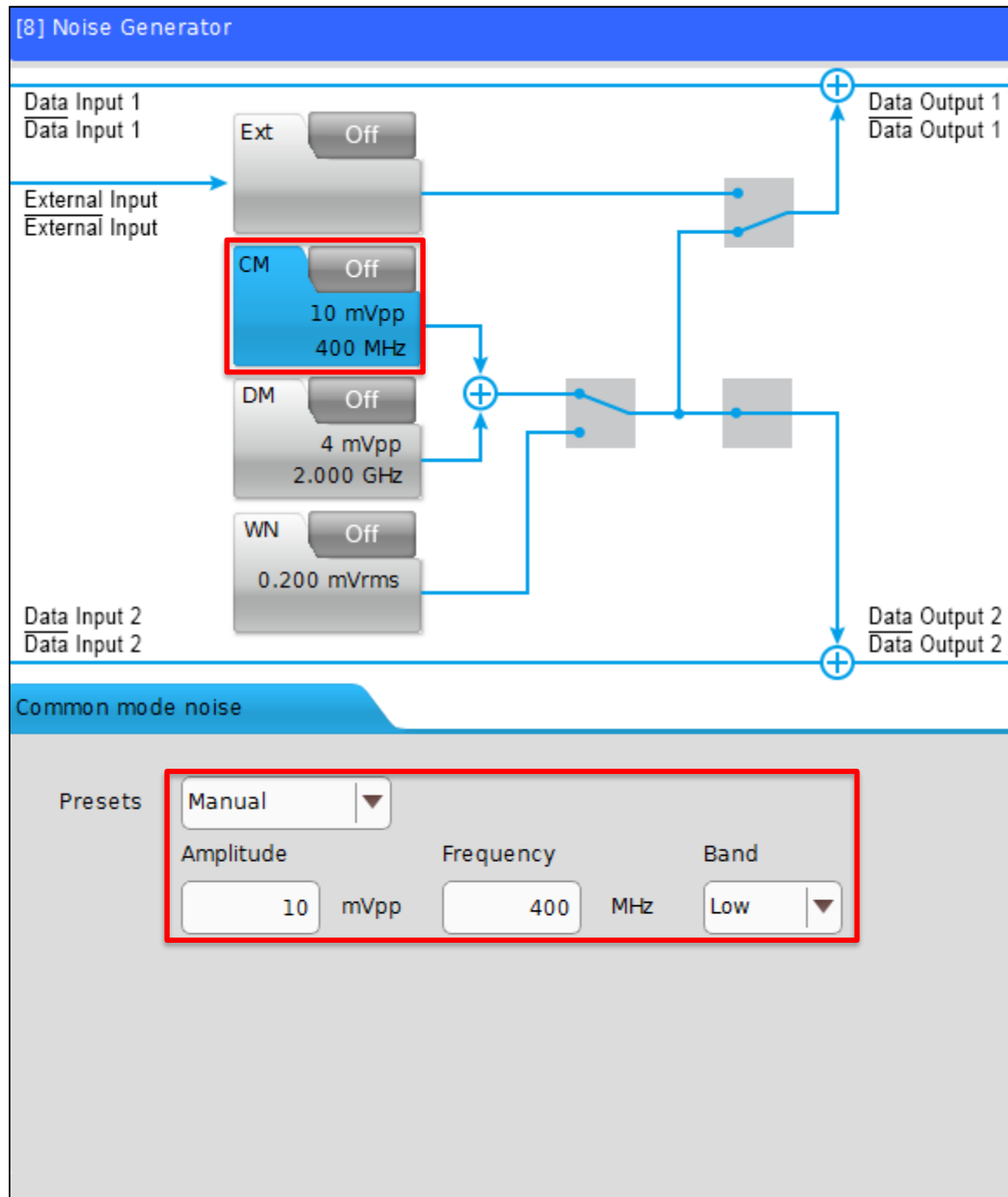


FIGURE 75. CM SETTING

8.2.1 Set Up Oscilloscope

8.2.1.1 Oscilloscope Vertical and Horizontal Setup

Set up the Scope as listed in Table 9.

TABLE 9. OSCILLOSCOPE VERTICAL AND HORIZONTAL SETUP

Setting	Setup
Vertical	Ch1-Ch3 (using the full range of the Scope's D/A)
Record Length	40M in a single acquisition
Sample Rate	80Gs/s
Averaging	OFF
Sample Mode	Real Time
Bandwidth	16GHz
Vertical Scale	Set to full screen without clipping
Sin x/x	OFF



FIGURE 76. OSCILLOSCOPE VERTICAL AND HORIZONTAL SETUP

8.2.1.2 Oscilloscope Clock Recovery Setup

Enter the Clock Recovery menu and set up the Scope as listed in Table 10.

TABLE 10. OSCILLOSCOPE CLOCK RECOVERY SETUP

Setting	Setup
Nominal Data Rate	10Gb/s
Clock Recovery Method	Second Order PLL
PLL Specification	OJTF Loop Bandwidth: 5.000MHz Damping factor: 0.94

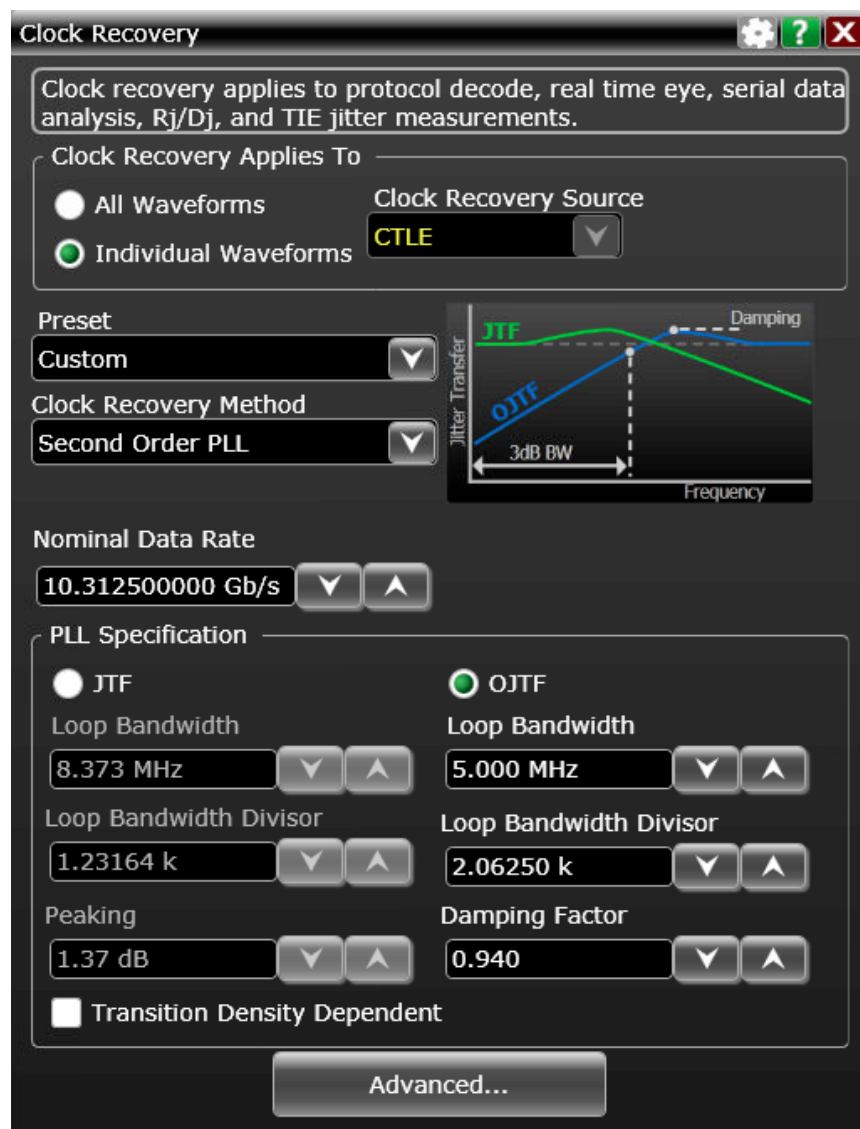


FIGURE 77. OSCILLOSCOPE CLOCK RECOVERY SETUP

8.2.1.3 Oscilloscope AC Common Mode (ACCM) Setup

Set up the Scope as listed in Table 11.

TABLE 11. OSCILLOSCOPE ACCM SETUP

Setting	Setup
Sample Rate	$\geq 80\text{Gs/s}$
Record Length	40Mpts per channel
Bandwidth	16GHz
Vertical Scale	20mV/div
CDR	OFF
Averaging	OFF
Sin x/x	OFF

8.2.1.4 Jitter Setup

Enter the Jitter menu and set up the Scope as listed in Table 12.

TABLE 12. OSCILLOSCOPE JITTER SETUP

Setting	Setup
Units	Unit Interval
Jitter Method	Spectral
Source for Jitter & Eye Diagram	Channel 1-3
BER Level	1E-9
Pattern	Periodic, Repeating Pattern ($2^{15}-1 = 32,767$ bits)

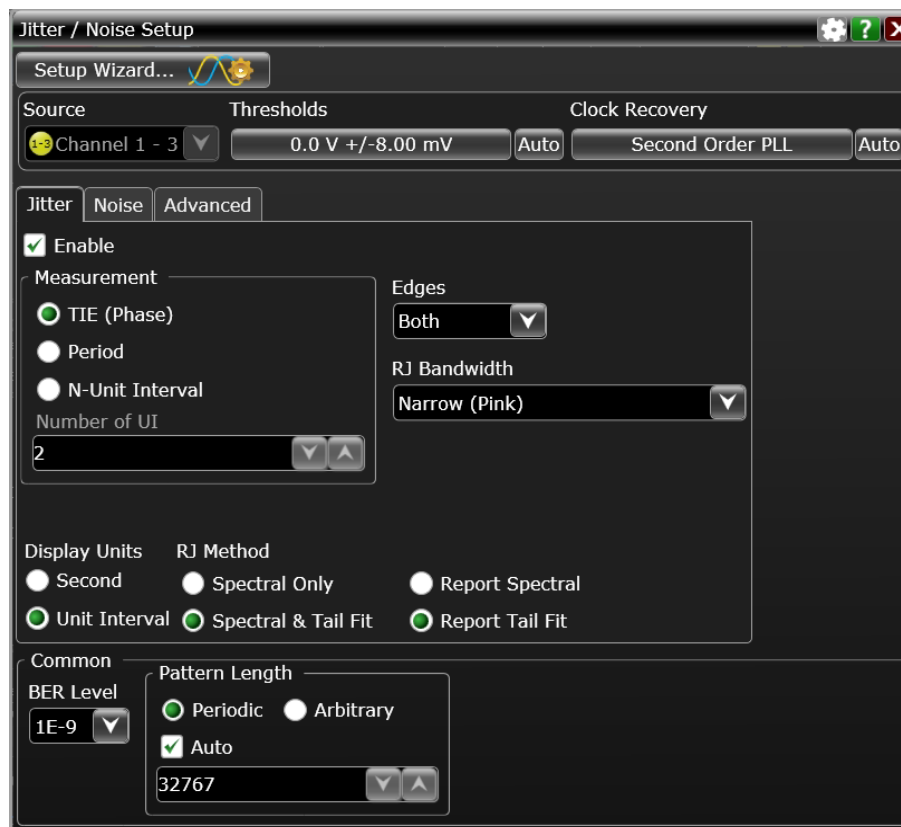
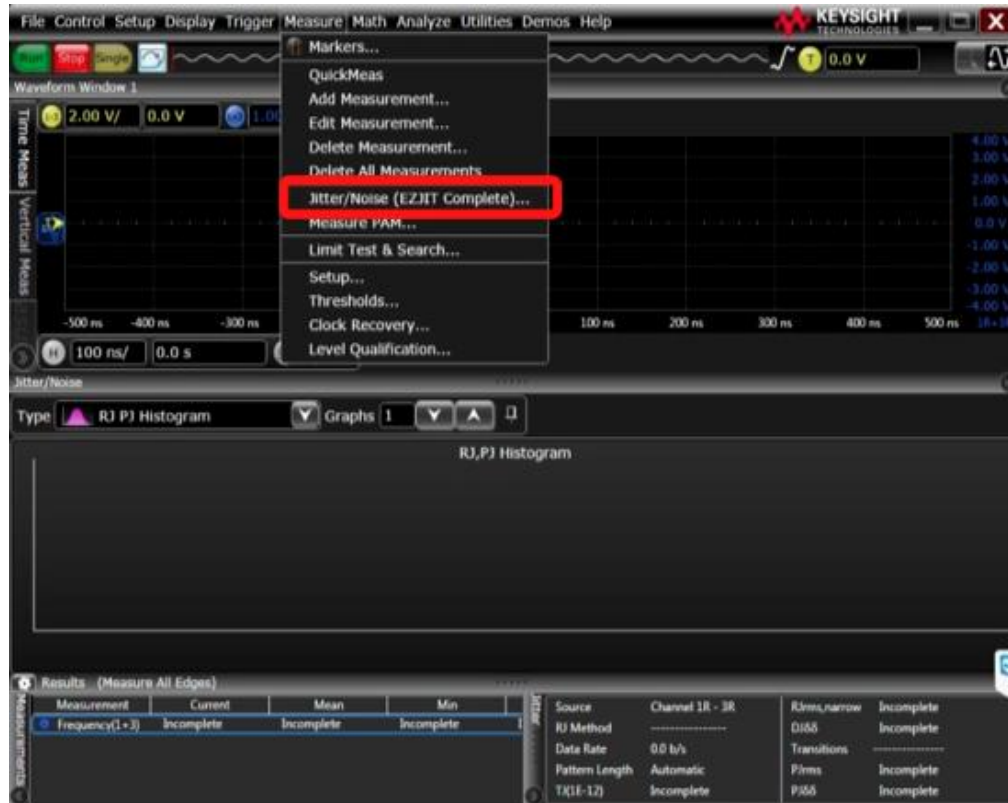


FIGURE 78. OSCILLOSCOPE JITTER SETUP

8.2.1.5 Eye Diagram Vertical Setup

Set up the Scope as listed in Table 13.

TABLE 13. OSCILLOSCOPE EYE DIAGRAM VERTICAL SETUP

Setting	Setup
Vertical Scale	200 mV/div
Horizontal Scale	2 UI's
Eye Mask Height	92 mV (for final Eye Height Calibration)
Eye Mask Width	513 mUI

8.2.2 Record ISI Measurements

- Step through Pre-set coefficients 0 to 14 and use a Preset which gives minimum DDJ Measurement. Although these are not calibrated values, record ISI measurement as part of the measurement table.

√Table 3-53: Preset FFE Coefficients ^{a b}

Preset #	Pre-shoot (dB)	De-emphasis (dB)	Informative Filter Coefficients		
			C-1	Co	C+~
0	0	0	0	1	0
1	0	-1.9	0	0.90	-0.10
2	0	-3.6	0	0.83	-0.17
3	0	-5.0	0	0.78	-0.22
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0
6	1.1	-1.9	-0.05	0.86	-0.09
7	1.4	-3.8	-0.05	0.79	-0.16
8	1.7	-5.8	-0.05	0.73	-0.22
9	2.1	-8.0	-0.05	0.68	-0.27
10	1.7	0	-0.09	0.91	0
11	2.2	-2.2	-0.09	0.82	-0.09
12	2.5	-3.6	-0.09	0.77	-0.14
13	3.4	-6.7	-0.09	0.69	-0.22
14	3.8 3.6	-3.8 0	-0.13 -0.17	0.74 0.83	-0.13 0
15	1.7	-1.7	-0.05	0.55	-0.05

FIGURE 79. ISI MEASUREMENT PRESET TABLE

- In 4Tap Emphasis Ch1 Menu, create 15 Presets with coefficients which match the Table in the DisplayPort 2.1 Specification. See Figure 80 below.

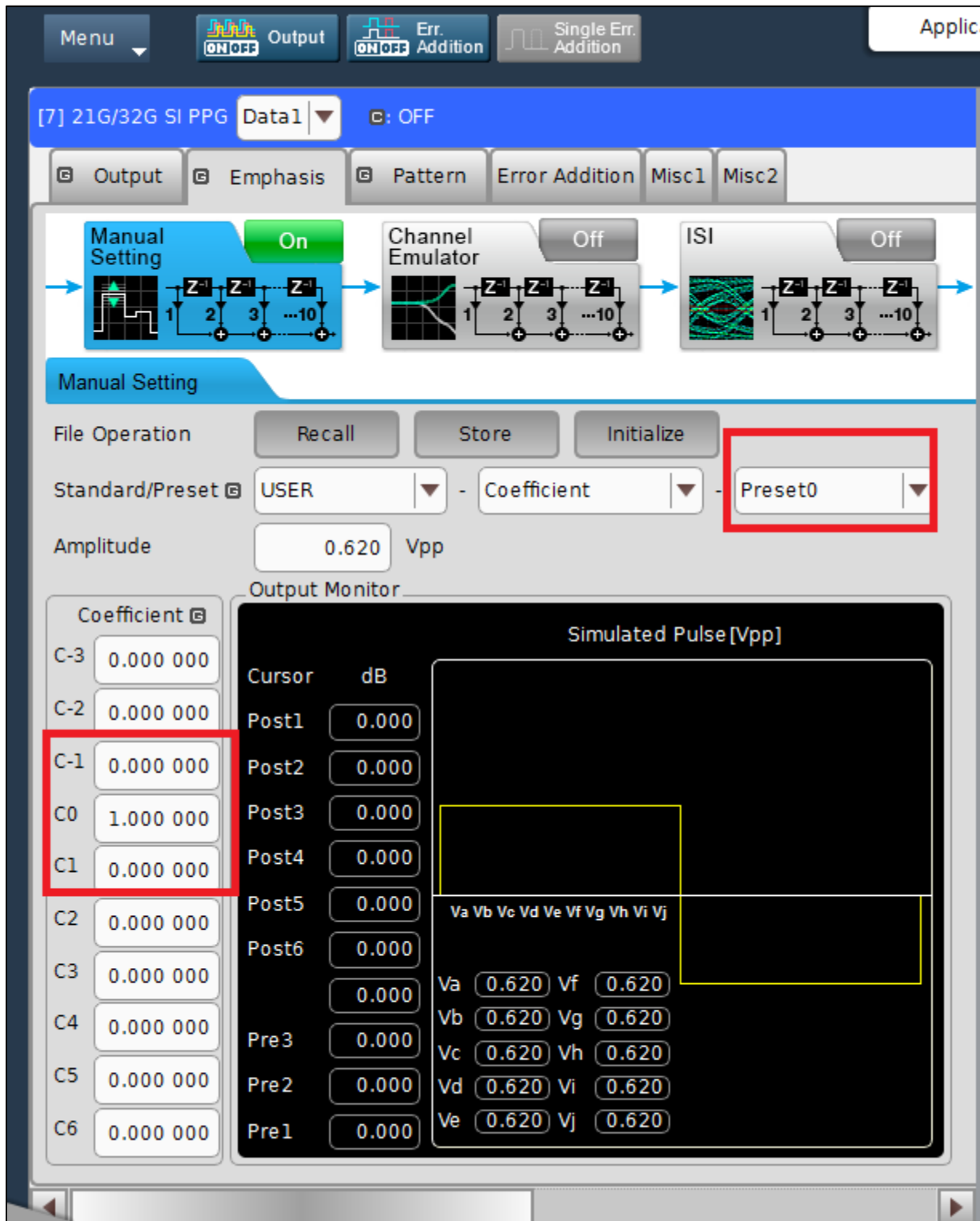


FIGURE 80. 4TAP EMPHASIS CH1 INTERFACE

- Step through all 15 Presets. The Preset with the minimum DDJpp measurement is the optimized preset.



FIGURE 81. OPTIMIZED PRESET (MINIMUM DDJPP) MEASUREMENT ON KEYSIGHT SCOPE

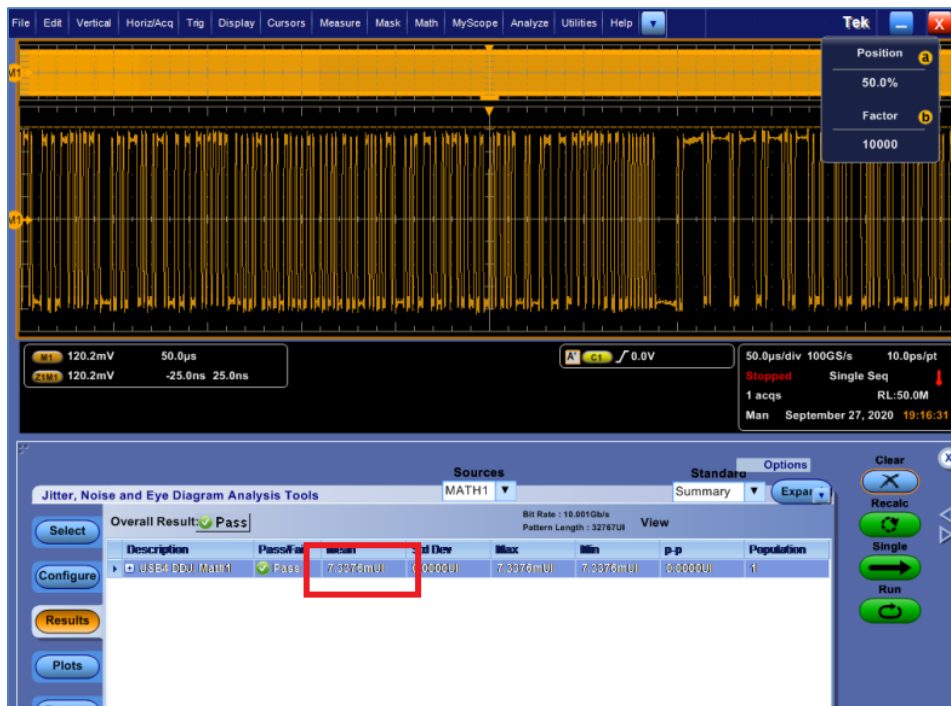


FIGURE 82. OPTIMIZED PRESET (MINIMUM DDJPP) MEASUREMENT ON TEKTRONIX SCOPE

- Set up the Scope so that Channel 1 and Channel 3 scale to 80% of screen.
- Turn on Function1 of Scope to perform subtraction of Channel 1 and Channel 3.
- Measure VPP on Function1.



FIGURE 83. CALIBRATION TO PHASE MATCH ON KEYSIGHT SCOPE



FIGURE 84. CALIBRATION TO PHASE MATCH ON TEKTRONIX SCOPE

7. Calibrate ACCM to be 100mVpp at 400MHz Clock, using ACCM Scope Setup. Then return CM Amplitude to zero.
 - a) Turn On SSC and turn Off all jitter components on the MP1900A Generator. Change the test pattern to PRBS31 and transmit the PRBS31 pattern from the MP1900A.
 - b) Set the frequency to 400MHz on the MP1900A CM Generator.

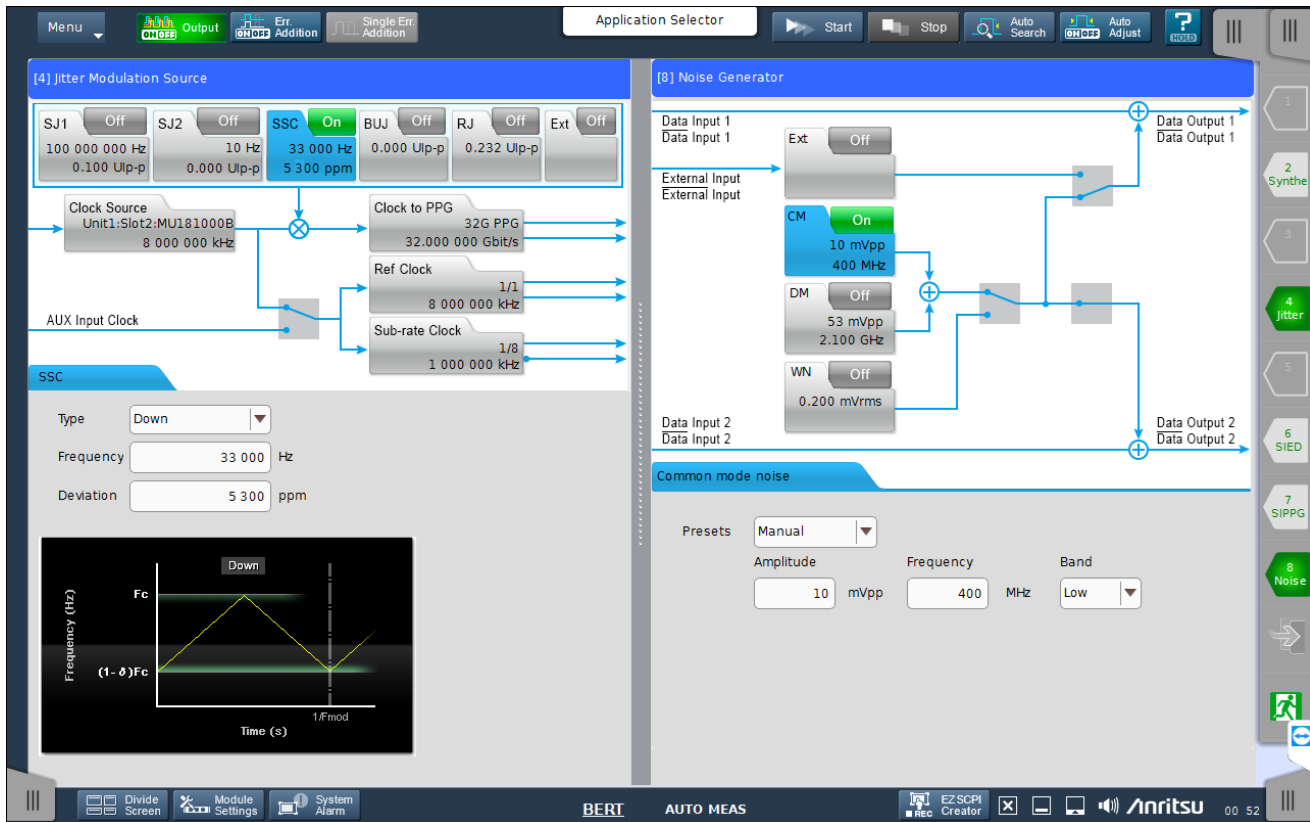


FIGURE 85. CALIBRATE ACCM

- c) Measure Ch1 and Ch3 Signals on the scope to have an amplitude of a Mean Peak-to-Peak measurement of 100mVpp.

$$V_{AC-CM} = (V_{TX-P} + V_{TX-N})/2$$

- d) Turn Off the CM output.

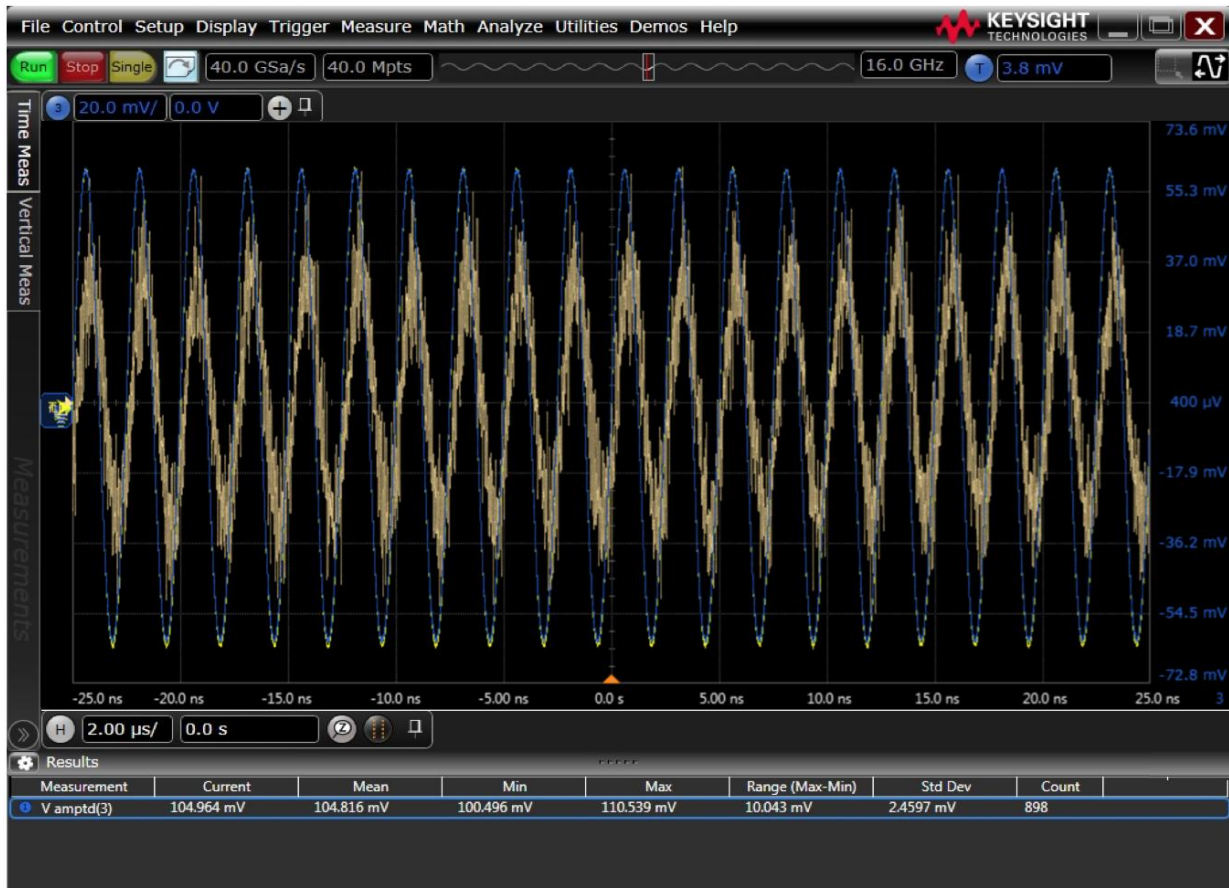


FIGURE 86. CALIBRATE ACCM PEAK-TO-PEAK AMPLITUDE

- Turn on all remaining Jitter terms (RJ-Filtered (User); HPF (10MHz); SJ@100MHz); and set all jitter amplitudes to zero.

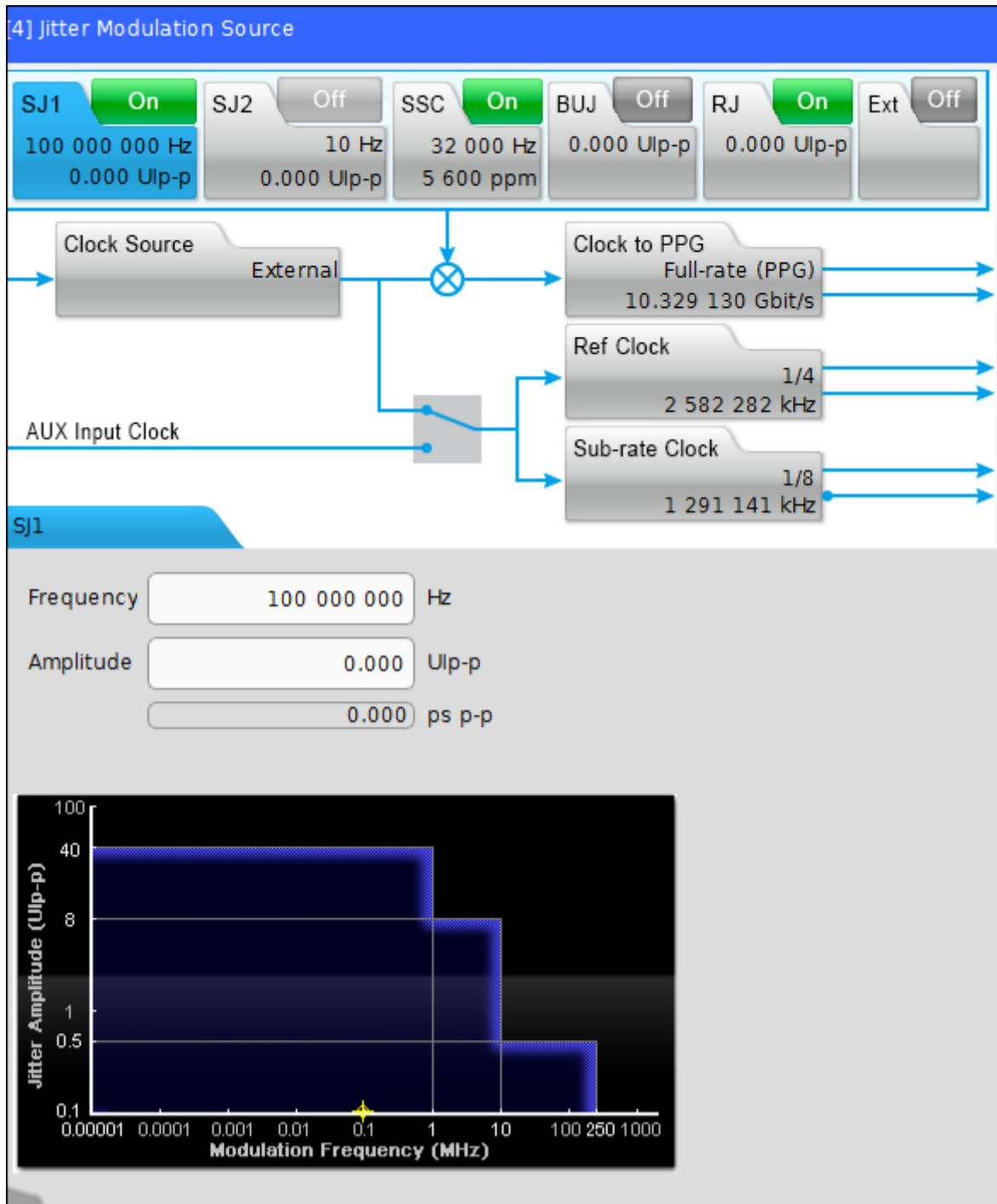


FIGURE 87. JITTER AMPLITUDES

9. Return the Scope setup to the jitter setup.
10. Set the PRBS15 pattern on the MP1900A.
11. Calibrate RJ amplitude to 115mUI peak-to-peak or 9.58mUI RMS.
12. Return amplitude to zero.
13. Capture a screen shot.

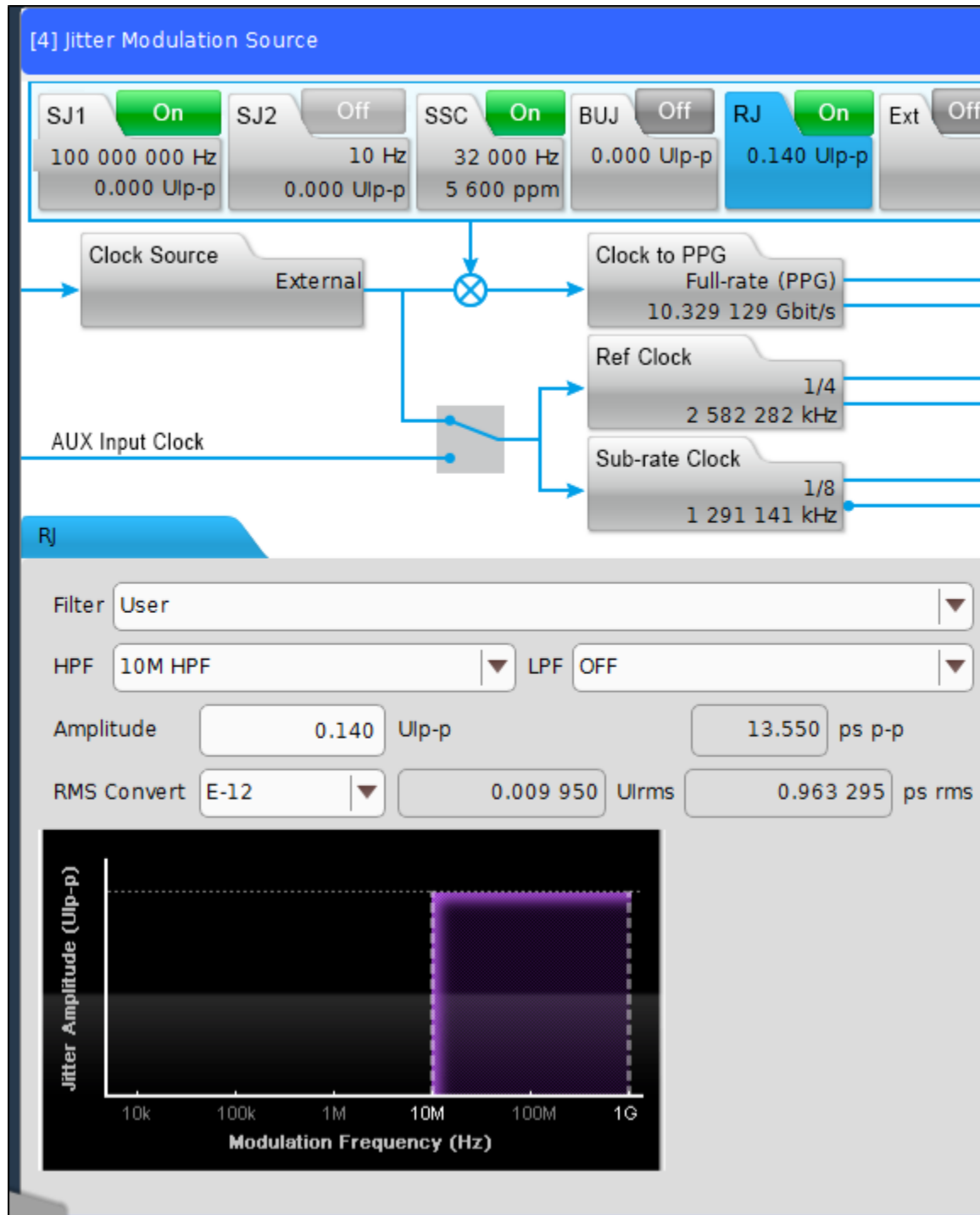


FIGURE 88. CALIBRATE RJ AMPLITUDE #1



FIGURE 89. CALIBRATE RJ AMPLITUDE #2 ON KEYSIGHT SCOPE

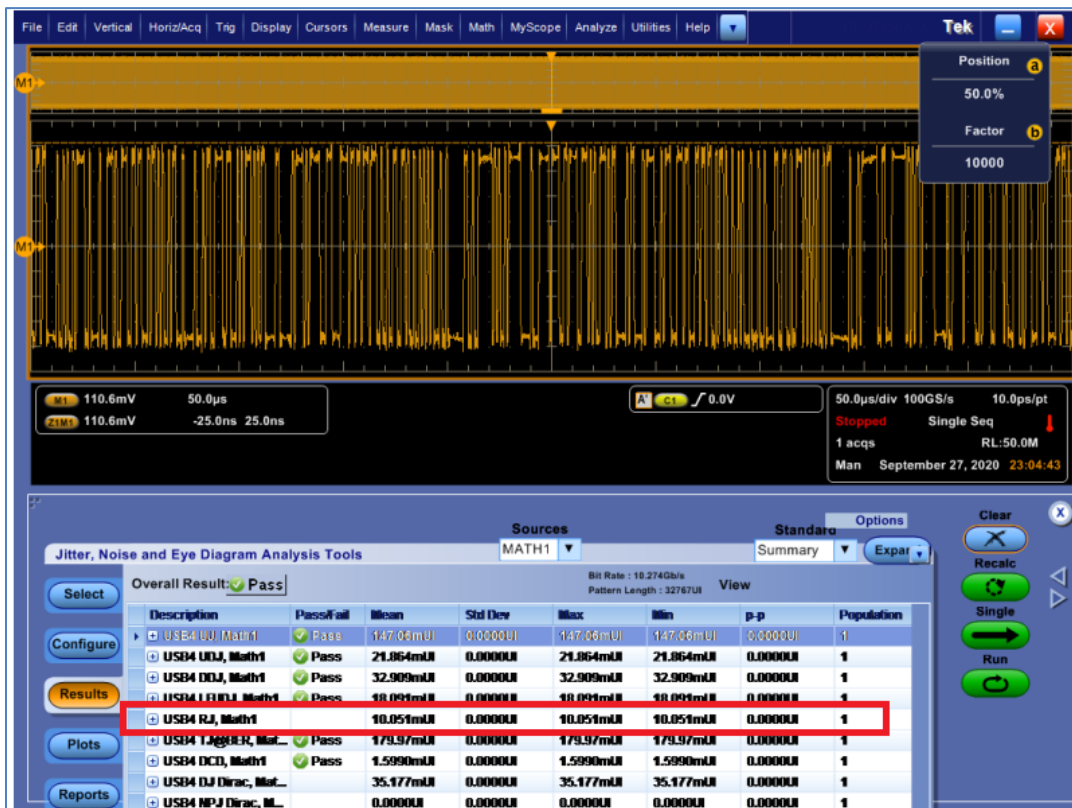


FIGURE 90. CALIBRATE RJ AMPLITUDE #2 ON TEKTRONIX SCOPE

14. Calibrate SJ amplitude to 170mUI peak-to-peak at 100MHz, where “peak-to-peak” is 170mUI.
15. Capture screen shot.

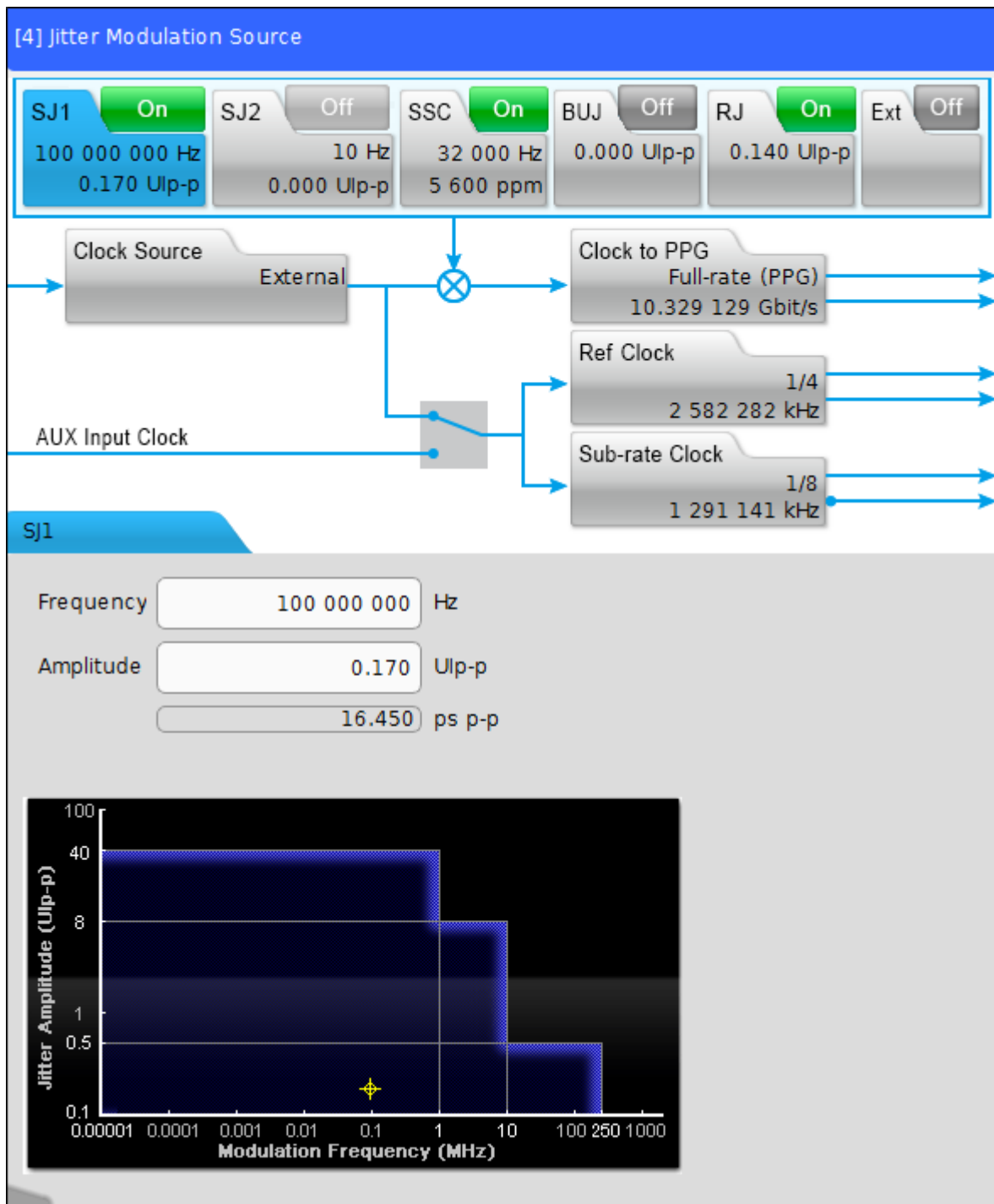


FIGURE 91. CALIBRATE SJ AMPLITUDE #1

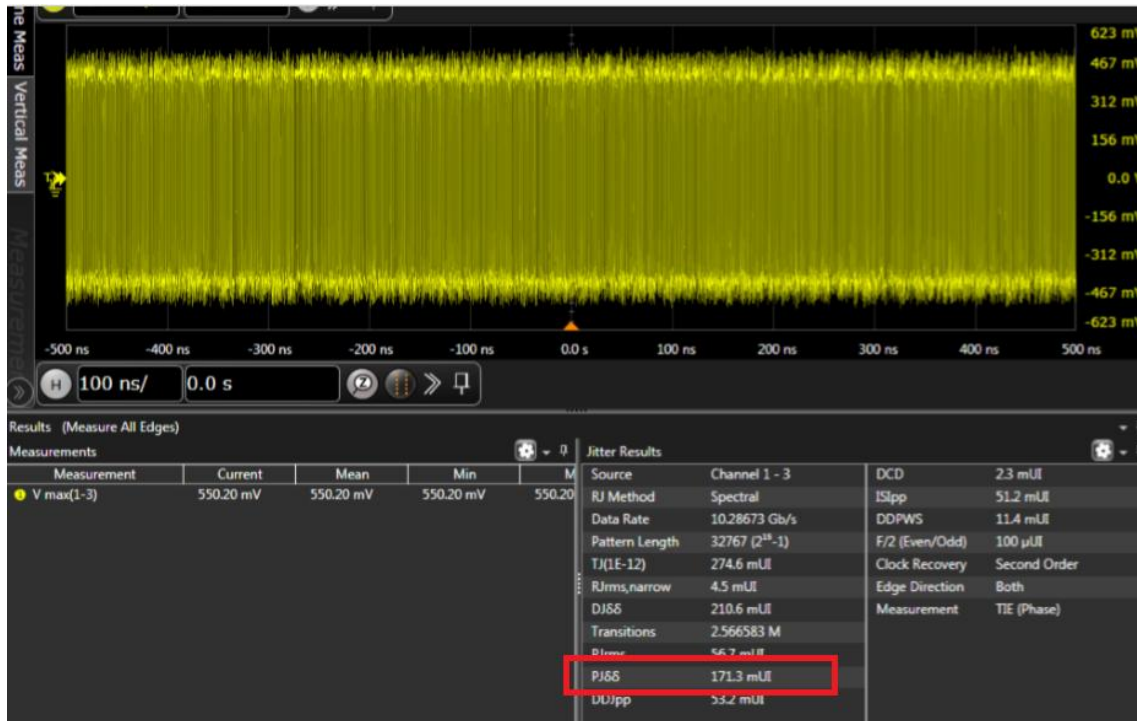


FIGURE 92. CALIBRATE SJ AMPLITUDE #2 ON KEYSIGHT SCOPE

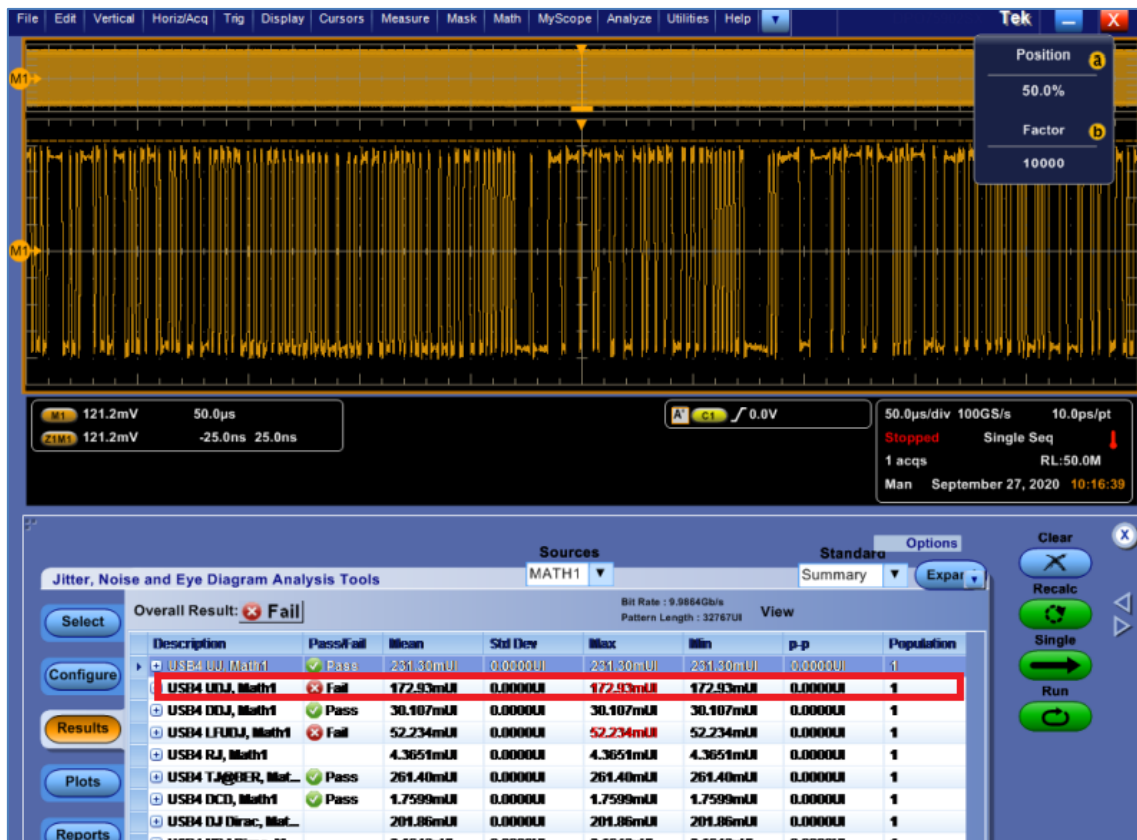


FIGURE 93. CALIBRATE SJ AMPLITUDE #2 ON TEKTRONIX SCOPE

16. Return all remaining impairment sources (CM, RJ, SJ) to their calibrated values.

17. Calibrate the TJ measurement to $330\text{mUI} \pm 12.5\text{mUI}$, using the SJ Amplitude control (for SJ frequency of 100MHz) and RJ Amplitude control (for SJ frequencies of less than 100MHz) as an adjustment on the BERT.
18. Capture screen shot.



FIGURE 94. TJ MEASUREMENT ON KEYSIGHT SCOPE

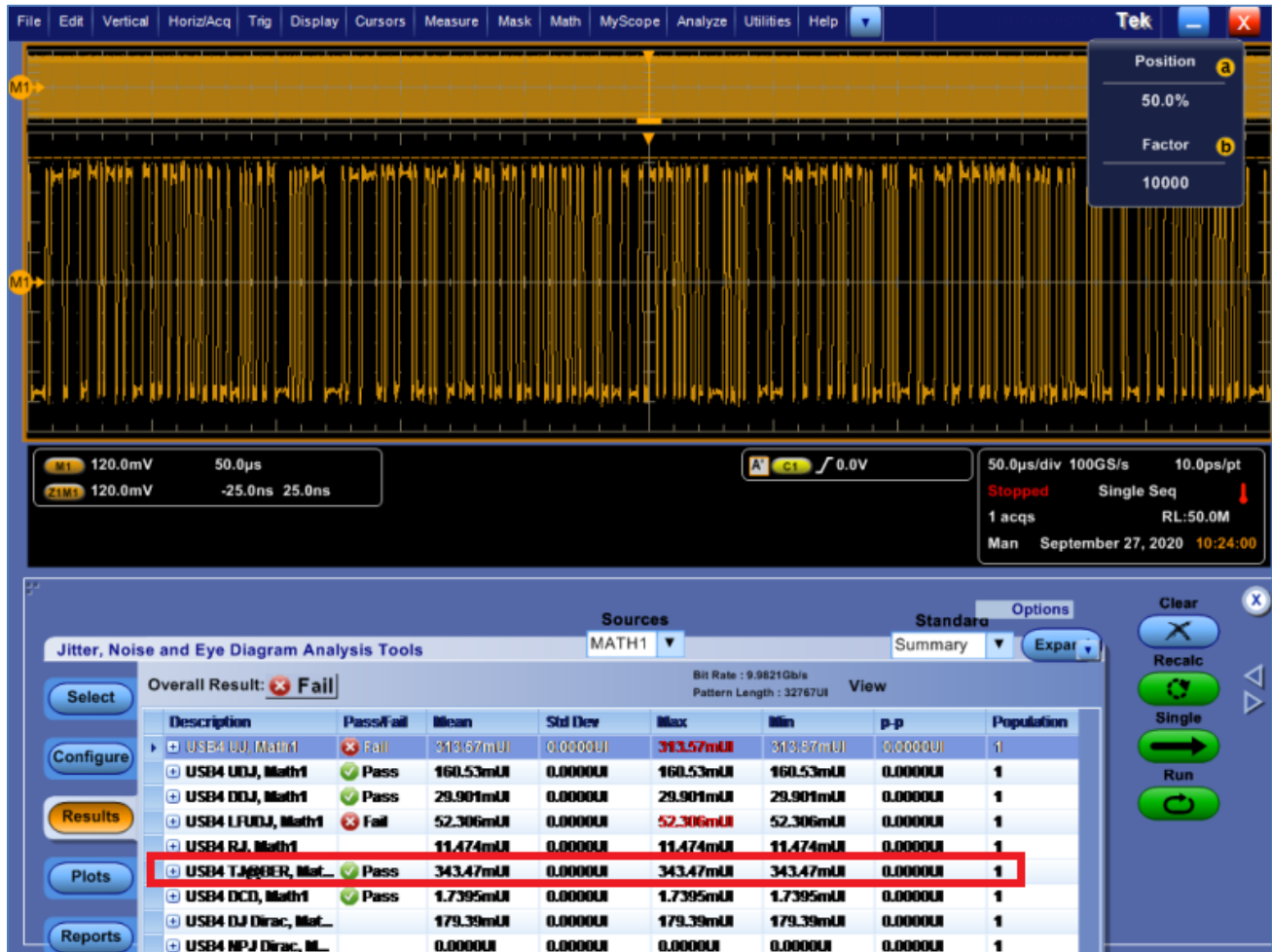


FIGURE 95. TJ MEASUREMENT ON TEKTRONIX SCOPE

19. Adjust the memory depth to capture 1,000,000 (1E6) bits.
20. Change the Pattern on the MP1900A BERT to PRBS31.
21. Calibrate Inner Eye Height to 700mV (top and bottom of the triangle eye mask are V:700mV, H:650mUI).
22. Capture screen shot.

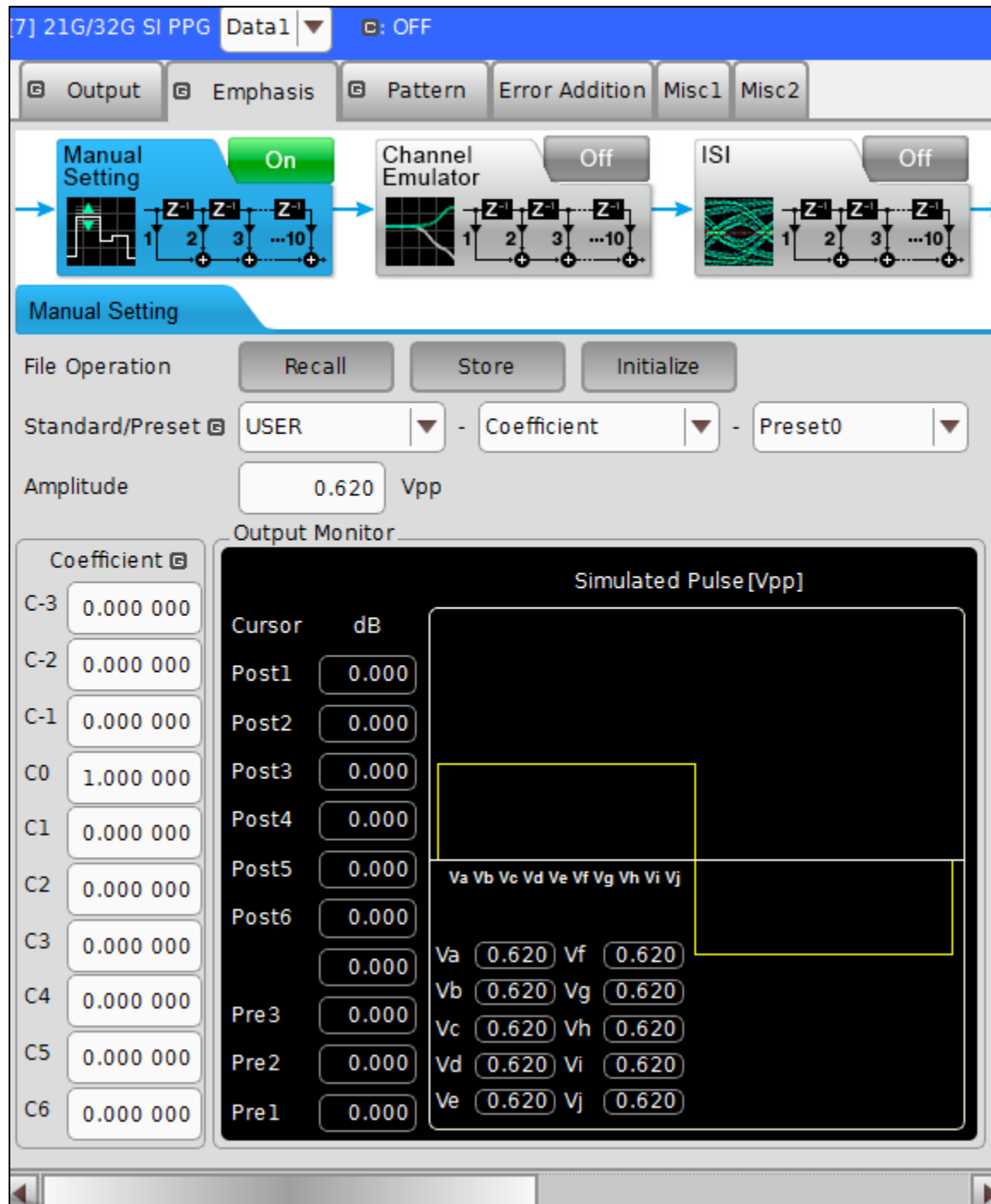


FIGURE 96. EYE AMPLITUDE

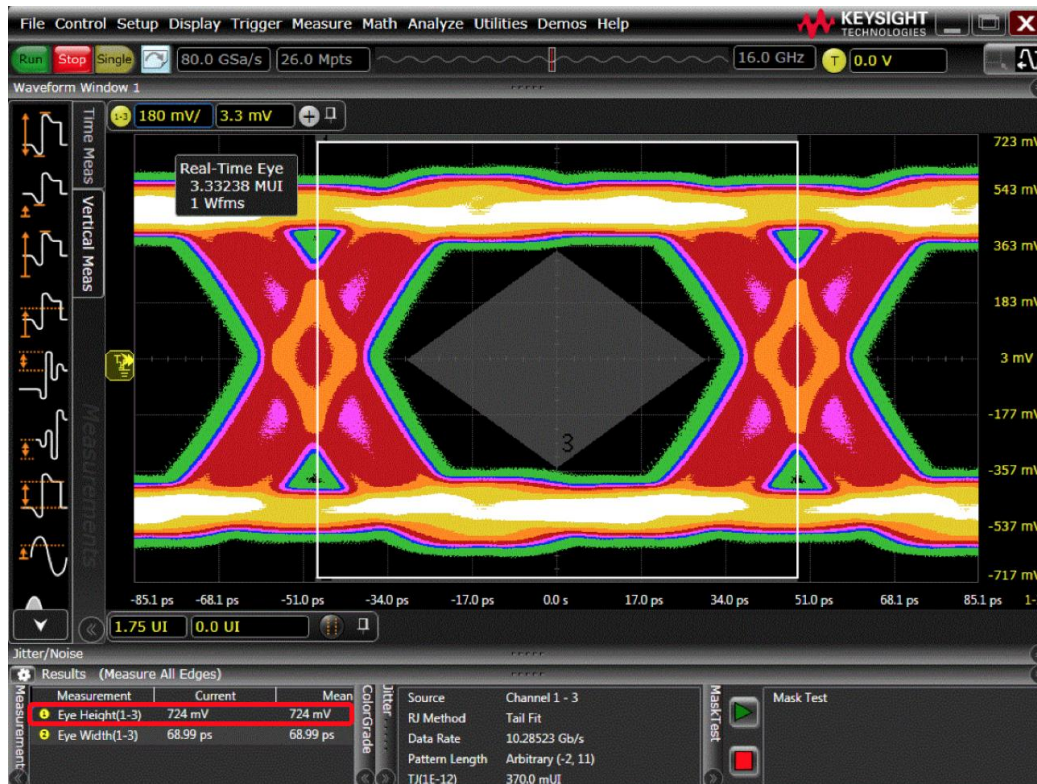


FIGURE 97. EYE MASK ON KEYSIGHT SCOPE

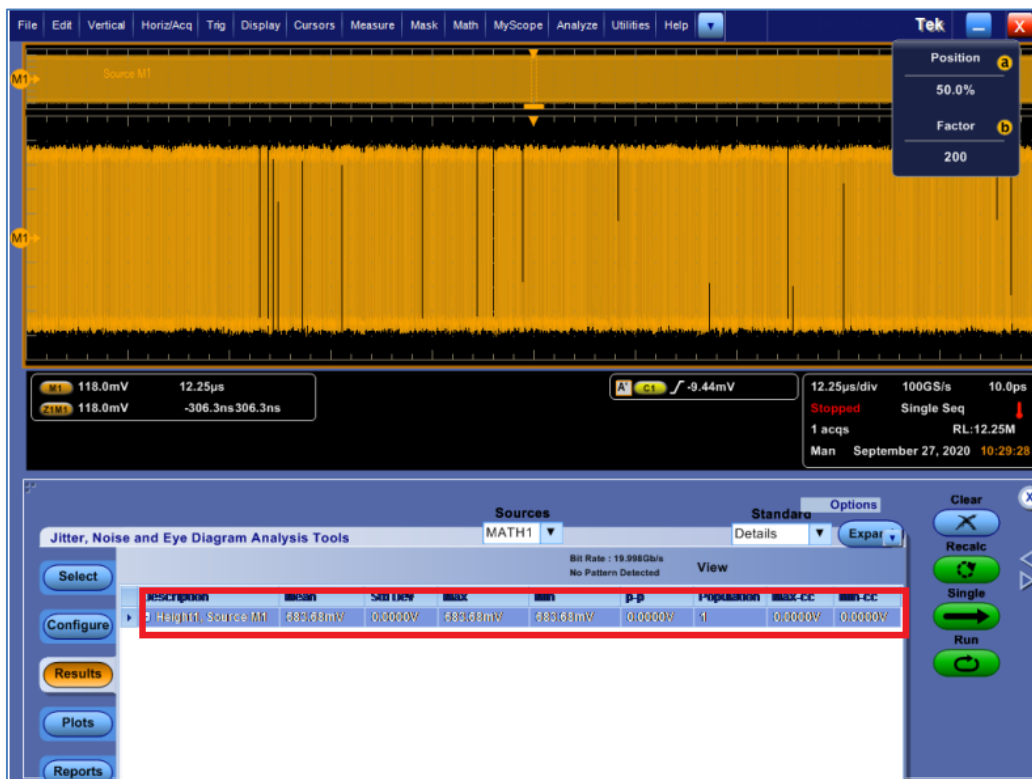


FIGURE 98. EYE MASK ON TEKTRONIX SCOPE

23. Save the BERT setup to “10G_TC1_100MHz”.

24. Return CM, RJ and PJ sources to zero amplitude.
25. Repeat step 8-21 for 1MHz, 2MHz, 10MHz and 50MHz PJ frequencies, saving the setups after each frequency as “10G_TC1_1MHz”, “10G_TC1_2MHz”, “10G_TC1_10MHz” and “10G_TC1_50MHz” respectively.

8.3 Calibrate and Save for UHBR10 (10.0 Gbit/s) Receiver at TP3_EQ

For this test case, the total ISI of a channel should be around -19dB @ 5GHz. The test fixture should have 1 to 1.5dB per mated pair.

1. Recall the BERT setup from 10G_TC1_100MHz.
2. Connect the physical setup with ISI Channel, as per Figure 35.
3. Search for the optimized DC Gain starting from DC Gain of 1 in Oscilloscope Equalization Setup, adjust the DC Gain to obtain the largest Eye Height with cable de-embedding.
 - a) Set up the Scope as follows for CTLE:
 - i) Number of Poles set to “2 Poles, AC Gain”
 - ii) DC Gain set to 1.00
 - iii) AC Gain set to 1.41
 - iv) Pole #1 Frequency set to 1.50 GHz
 - v) Pole #2 Frequency set to 5.00 GHz
 - b) Use the DC Gain Setting in Table 14 which yields the largest Eye Height.

TABLE 14. DC GAIN SETTINGS

Index	DC Gain Setting	Index	DC Gain Setting
0	1.000	-5	0.562
-1	0.891	-6	0.501
-2	0.794	-7	0.446
-3	0.708	-8	0.398
-4	0.630	-9	0.354

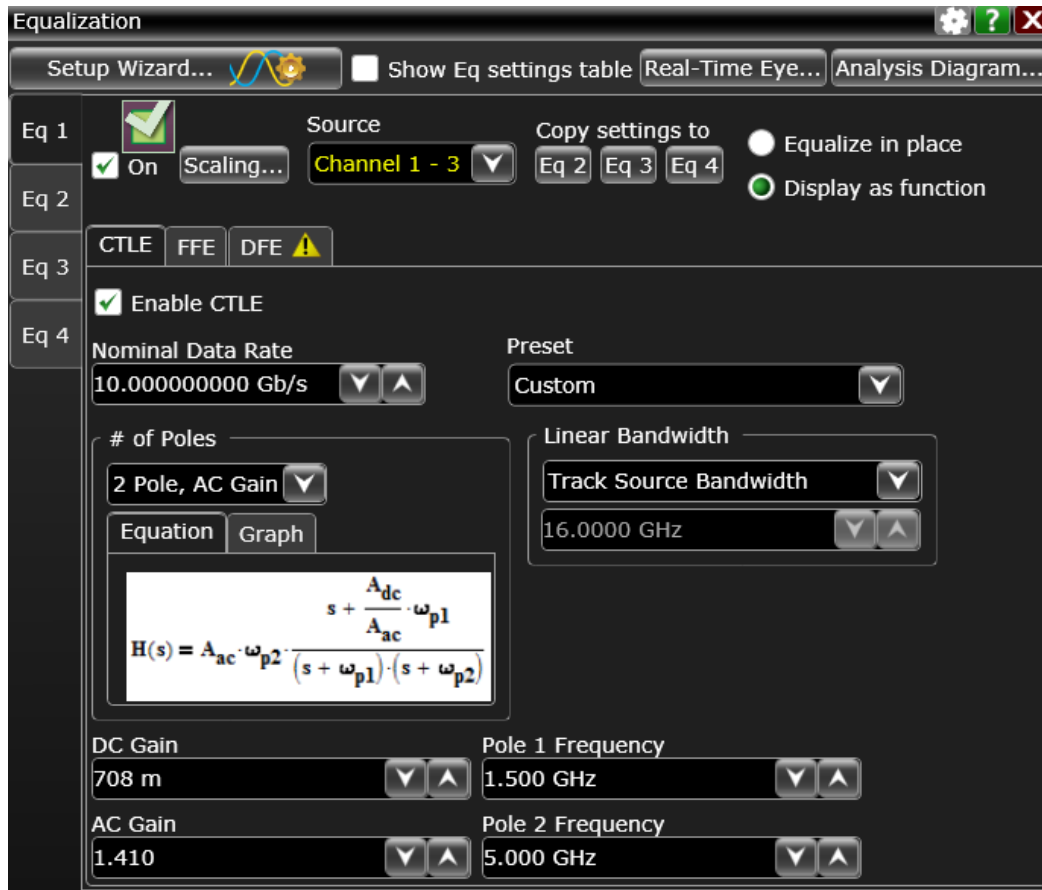


FIGURE 99. DC GAIN SETTING

c) Set up the DFE:

- i) Set Max Tap to 50mV.
- ii) Run Auto DFE.

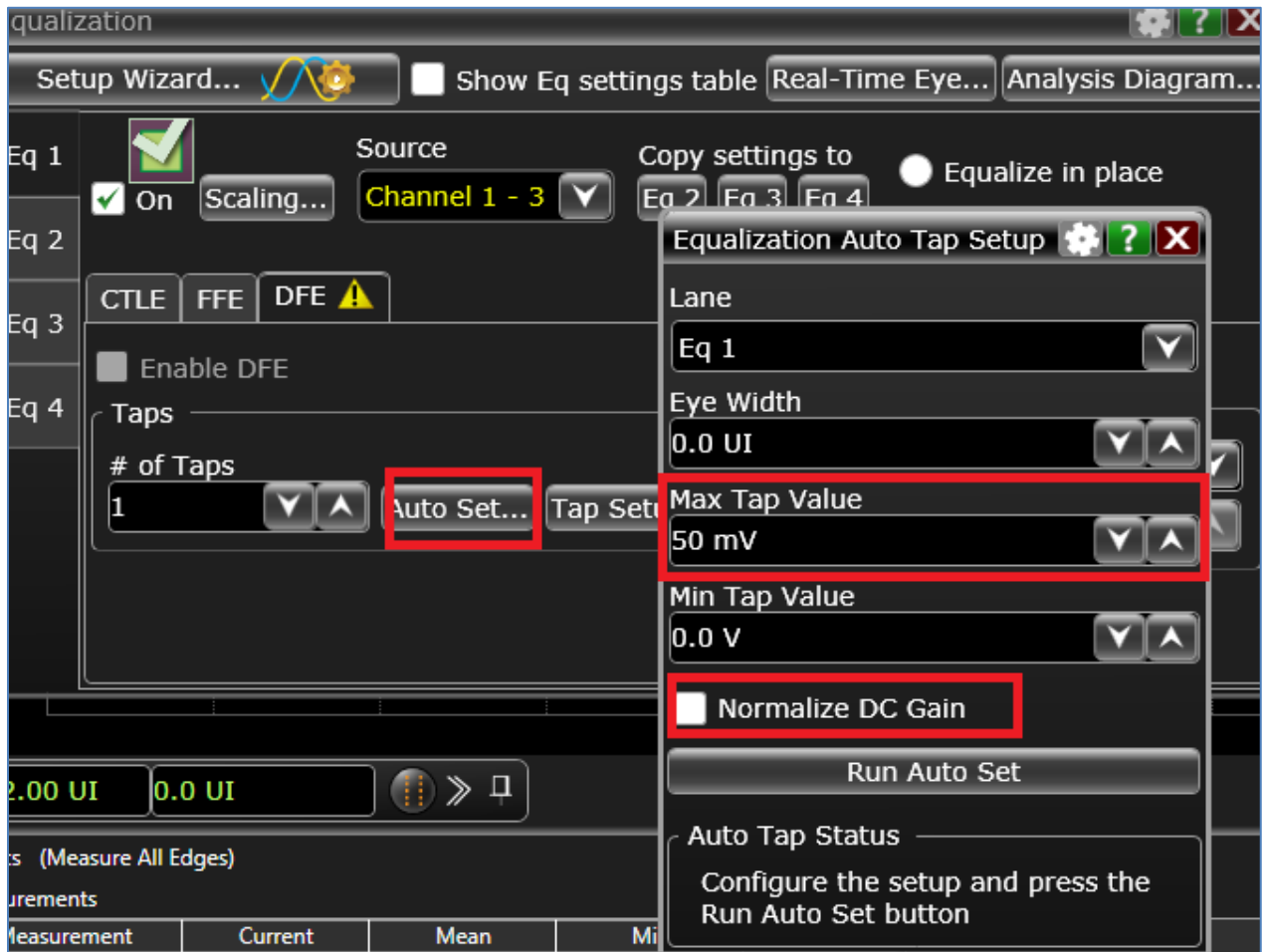


FIGURE 100. DFE SETTING

- d) Change the BERT Data pattern to PRBS31.
 - e) Adjust the memory depth to capture 1,000,000 (1E6) bits with 5 acquisitions (100,000 UIs per Acquisition).
 - f) For each acquisition, measure the Eye Width and Eye Height. Calculate the average of the five measurements and compute the Eye area via $Eye\ Width * Eye\ Height$.
 - g) Measure the Eye area by iterating through each CTLE gain. The CTLE gain with the biggest eye area is used for the following measurements.
11. By adjusting data amplitude, calibrate the Inner Eye Height to $92 \pm 10\text{mV}$ diff p-p (top and bottom of the triangle eye mask) using the PRBS31 pattern.

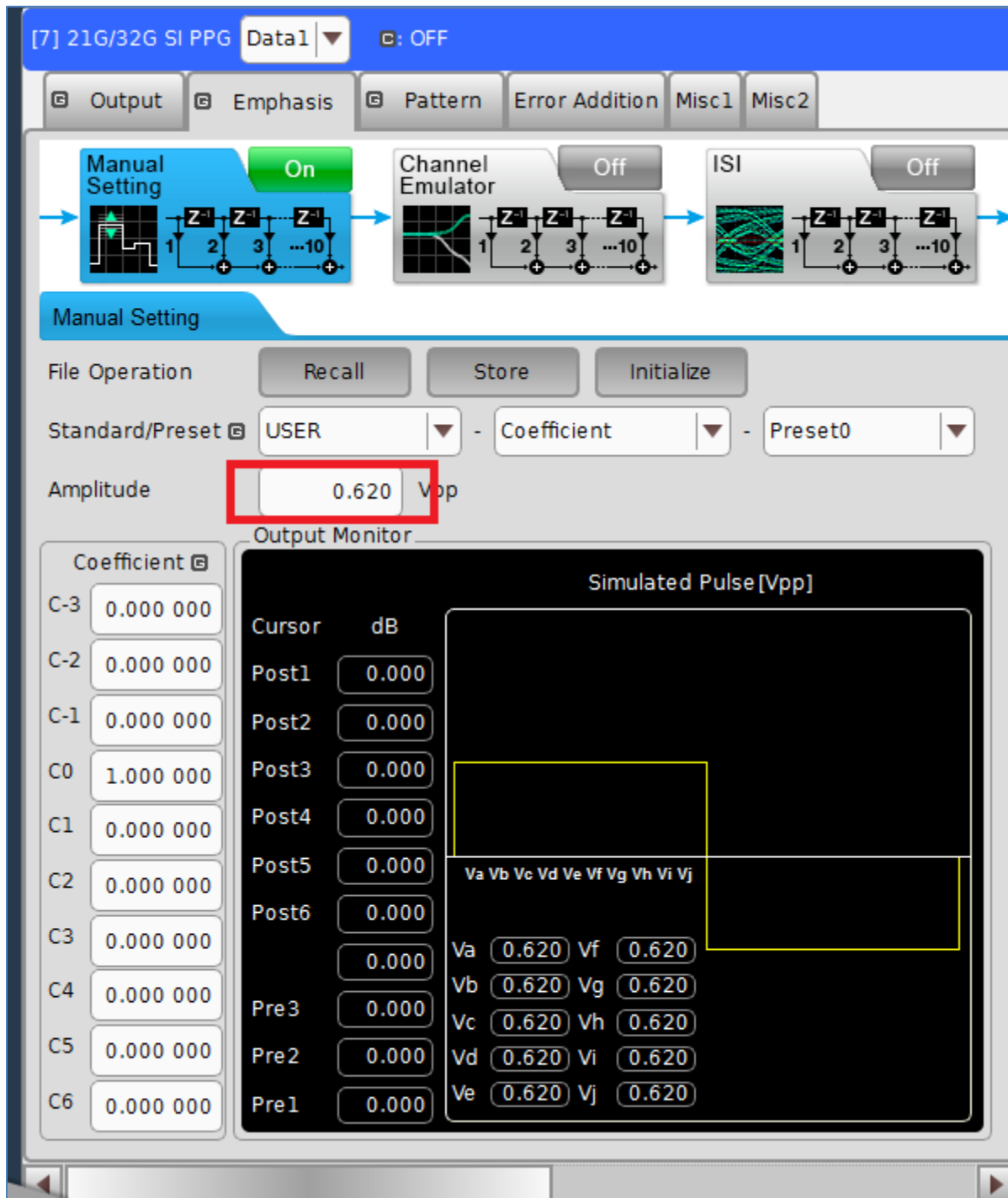
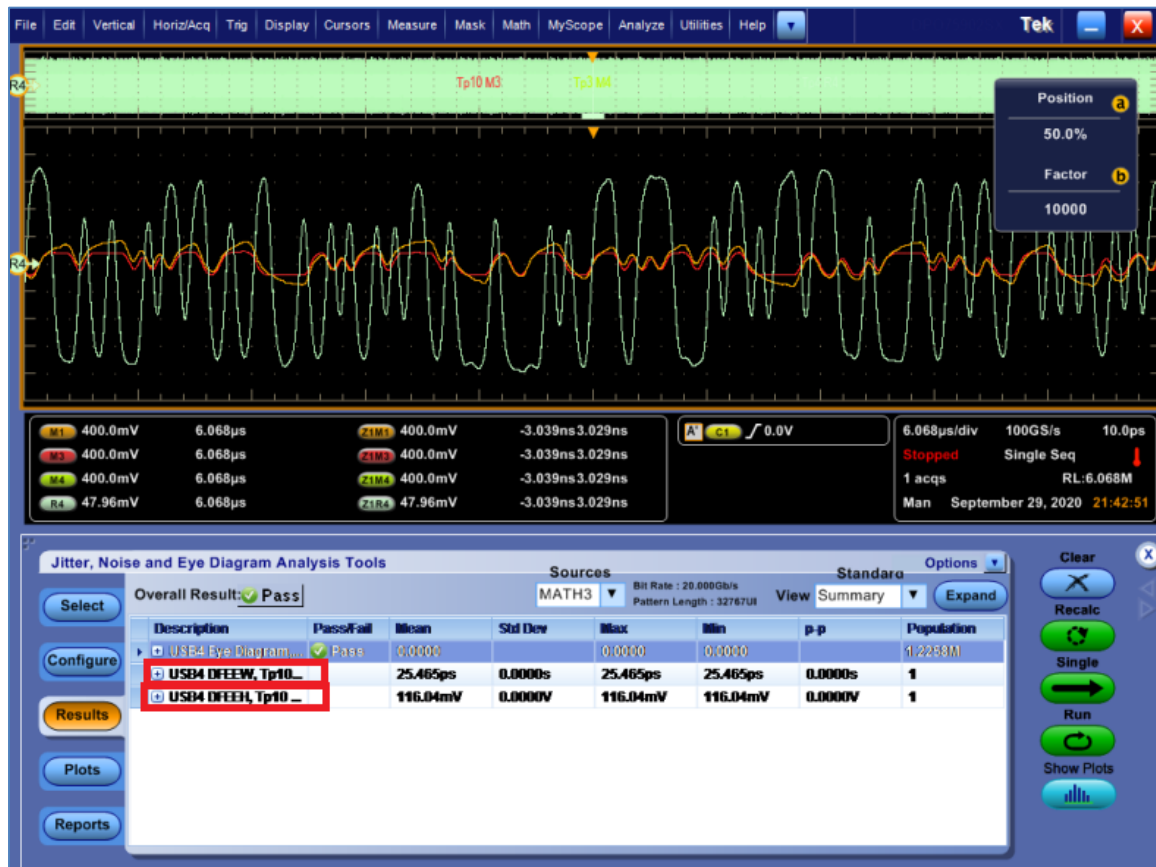
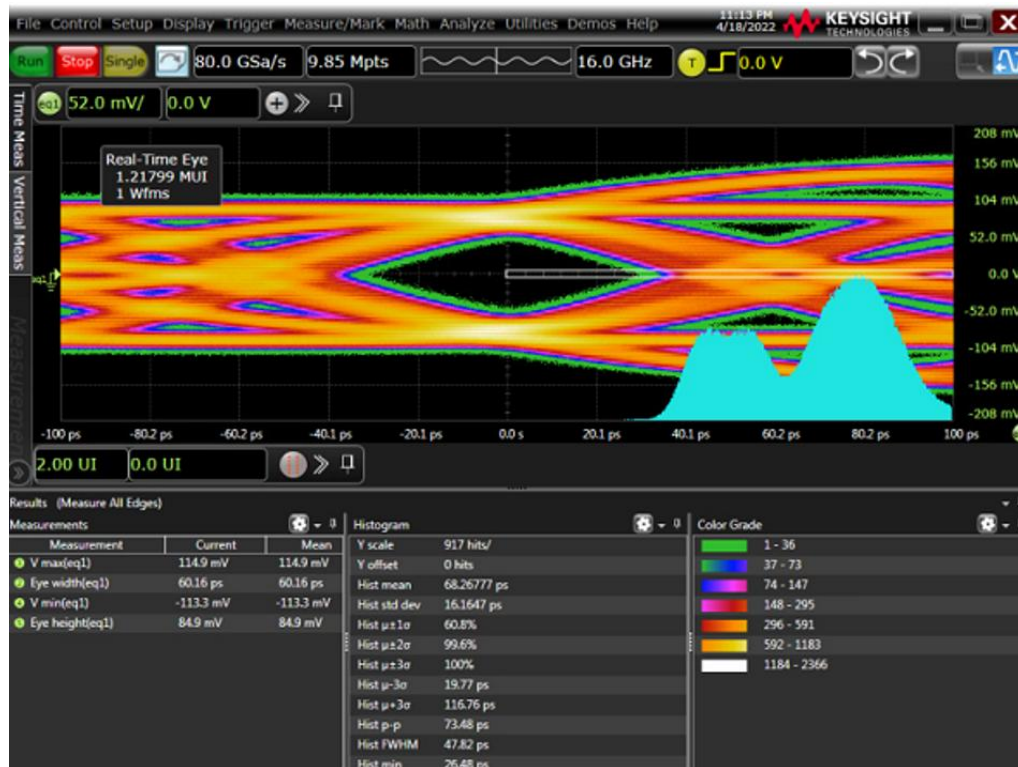


FIGURE 101. EYE AMPLITUDE



12. Measure the Eye Width at $\pm 2.5\text{mV}$ from 0mV . If the Eye width is not within the $513 \pm 25\text{mUI p-p}$ specification, tune RJ (if the SJ frequency is below 100MHz) or tune SJ (if the SJ frequency is 100MHz) so that the eye width is within specification.
13. Save the BERT Setup to “10G_TC2_100MHz”.
14. Repeat steps #1 to #10 for 1MHz , 2MHz , 10MHz and 50MHz PJ frequencies, saving each setup as 10G_TC2_1MHz, 10G_TC2_2MHz, 10G_TC2_10MHz and 10G_TC2_50MHz respectively.

8.4 Calibrate and Save for UHBR13.5 (13.5 Gbit/s) Receiver at TP1

The initial setups for the BERT and Scope are the same as defined for the 10Gb/s section above, except for the settings highlighted in **bold** below:

1. Set up the physical equipment connections without the ISI channel, as per Figure 34.
2. Set up the BERT as follows:
 - a) Set the Data Rate to **13.5Gb/s**.
 - b) Set the Pattern to PRBS15.
 - c) Turn on “SSC”, with settings of 33kHz (for 13.5G) with 5300ppm (for 13.5G) triangle down spread. (SSC will remain ON for all of the following steps.)
 - d) Set DATA+/DATA- Launch Amplitude to 750mV . This should set the differential amplitude just above the 700mV Eye Height target value as an initial value.
 - e) Set the initial CM interference amplitude to 0mV .

8.4.1 Set Up Oscilloscope

8.4.1.1 Oscilloscope Vertical and Horizontal Setup

Set up the Scope as listed in Table 21.

TABLE 15. OSCILLOSCOPE VERTICAL AND HORIZONTAL SETUP

Setting	Setup
Vertical	Ch1-Ch3 (using the full range of the Scope’s D/A)
Horizontal	20Gb/s
Record Length	40M
Sample Rate	80Gs/s
Averaging	OFF
Sample Mode	Real Time
Bandwidth	21GHz (The Calibration Bandwidth is limited to the Bit Rate of the signal, which is $2 * 1^{\text{st}}$ harmonic. This is done intentionally to be on the order of a Thunderbolt Receiver’s Bandwidth. This is essentially acting as an “Electrical Reference Receiver”, used for calibration. It reduces the noise measured by the Scope which a real Receiver will never perceive.)
Vertical Scale	Set to full screen without clipping

Sin x/x	OFF
---------	-----

8.4.1.2 Oscilloscope Clock Recovery Setup

Enter the Clock Recovery menu and set up the Scope as listed in Table 22.

TABLE 16. OSCILLOSCOPE CLOCK RECOVERY SETUP

Setting	Setup
Nominal Data Rate	13.5Gb/s
Clock Recovery Method	Second Order PLL
PLL Specification	OJTF Loop Bandwidth: 5.000 MHz Damping factor: 0.94

8.4.1.3 Oscilloscope AC Common Mode (ACCM) Setup

Set up the Scope as listed in Table 23.

TABLE 17. OSCILLOSCOPE ACCM SETUP

Setting	Setup
Sample Rate	$\geq 80\text{Gs/s}$
Record Length	27Mpts per channel
Bandwidth	21GHz
Vertical Scale	20mV/div
CDR	OFF
Averaging	OFF
Sin x/x	OFF

8.4.1.4 Jitter Setup

Enter the Jitter menu and set up the Scope as listed in Table 24.

TABLE 18. OSCILLOSCOPE JITTER SETUP

Setting	Setup
Units	Unit Interval
Jitter Method	Spectral
Source for Jitter & Eye Diagram	Channel 1-3
BER Level	1E-9
Pattern	Periodic, Repeating Pattern ($2^{15}-1 = 32,767$ bits)

8.4.1.5 Eye Diagram Vertical Setup

Set up the Scope as listed in Table 25.

TABLE 19. OSCILLOSCOPE EYE DIAGRAM VERTICAL SETUP

Setting	Setup
Vertical Scale	200 mV/div
Horizontal Scale	2 UI's
Eye Mask Height	112 mV (for final Eye Height Calibration)
Eye Mask Width	540 mUI

8.4.2 Record ISI Measurements

1. Step through the Preset Coefficients 0-15 and use the Preset which yields the minimum DDJ Measurement. Although this is not a Calibrated value, record this ISI Measurement as part of the measurements table.
2. Change the pattern on the BERT to PRBS31. Calibrate ACCM to be 100mVpp at 400MHz Clock, using the ACCM Scope Setup.
3. Return CM Amplitude to zero.
4. Turn on all remaining Jitter terms (RJ-Filtered [10MHz HPF] and SJ at 100MHz).
5. Set all jitter amplitudes to zero.
6. Return the Scope setup to the setup in Section 8.4.1.
7. Change the pattern on the BERT to PRBS15.
8. Calibrate RJ Amplitude to 115mUI peak-to-peak (9.58mUI RMS).
9. Return amplitude to zero.
10. Capture screen shot.
11. Calibrate SJ Amplitude to 170mUI peak-to-peak at 100MHz.
12. Capture screen shot.
13. Return all remaining impairment sources (CM, RJ, SJ) to their calibrated values.
14. Calibrate the TJ measurement to $360\text{mUI} \pm 17\text{mUI}$ using SJ Amplitude control (for SJ Frequency of 100MHz) and RJ Amplitude control (for SJ Frequencies of less than 100 MHz) as an adjustment on the BERT.
15. Capture screen shot.
16. Change the pattern on the BERT to PRBS31.
17. Calibrate Inner Eye Height to 700mV (top and bottom of triangle eye mask, with V:700mV; H:620mUI).
18. Capture screen shot.
19. Save BERT Setup to "135G_TC1_100MHz".

20. Repeat steps #1 to #18 for 1MHz, 2MHz, 10MHz and 50MHz PJ frequencies, saving each BERT Setup as 135G_TC1_1MHz, 135G_TC1_2MHz, 135G_TC1_10MHz and 135G_TC1_50MHz.

8.5 Calibrate and Save for UHBR13.5 (13.5Gbit/s) Receiver at TP3_EQ

For this test case, the total ISI of a channel should be around -16.5dB@10GHz. The test fixture should have 1 to 1.5dB per mated pair.

1. Recall the BERT setup from 135G_TC1_100MHz.
2. Connect the physical setup with ISI Channel, as per Figure 36.
3. Search for Optimized DC Gain starting from DC Gain of 1 in Oscilloscope Equalization Setup, adjust the DC Gain to obtain the largest Eye Height with cable de-embedding.
 - a) Set up the Scope as follows for CTLE:
 - i) Number of Poles set to “2 Poles, AC Gain”
 - ii) DC Gain set to 1.00
 - iii) AC Gain set to 1.41
 - iv) Pole #1 Frequency set to 3.375 GHz
 - v) Pole #2 Frequency set to 6.75 GHz
 - b) Use the DC Gain Setting in Table 26 which yields the largest Eye Height.

TABLE 20. DC GAIN SETTINGS

Index	DC Gain Setting	Index	DC Gain Setting
0	1.000	-5	0.562
-1	0.891	-6	0.501
-2	0.794	-7	0.446
-3	0.708	-8	0.398
-4	0.630	-9	0.354

- c) Set up the DFE:
 - i) Set Max Tap to 50mV.
 - ii) Run Auto DFE.

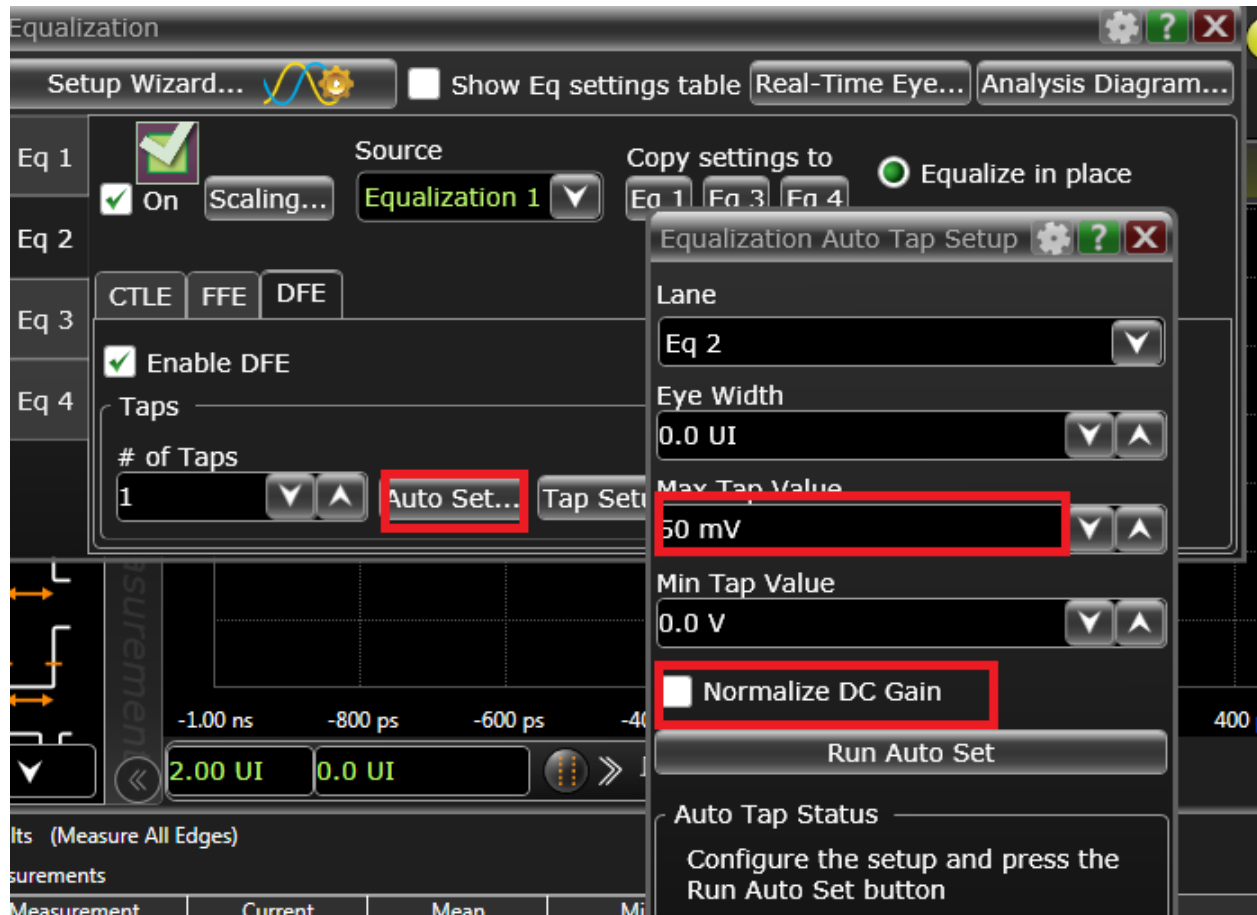




FIGURE 102. DFE SETTING

- d) Adjust the memory depth to capture 1,000,000 (1E6) bits with 5 acquisitions (100,000 UI's per Acquisition).
 - e) For each acquisition, measure the Eye Width and Eye Height. Calculate the average of the five measurements and compute the Eye area via *Eye Width * Eye Height*.
 - f) Measure the Eye area by iterating through each CTLE gain. The CTLE gain with the biggest Eye area is used for the following measurements.
15. Calibrate the Inner Eye Height to $112 \pm 10\text{mV}$ diff p-p (top and bottom of the triangle eye mask) using the PRBS31 pattern.

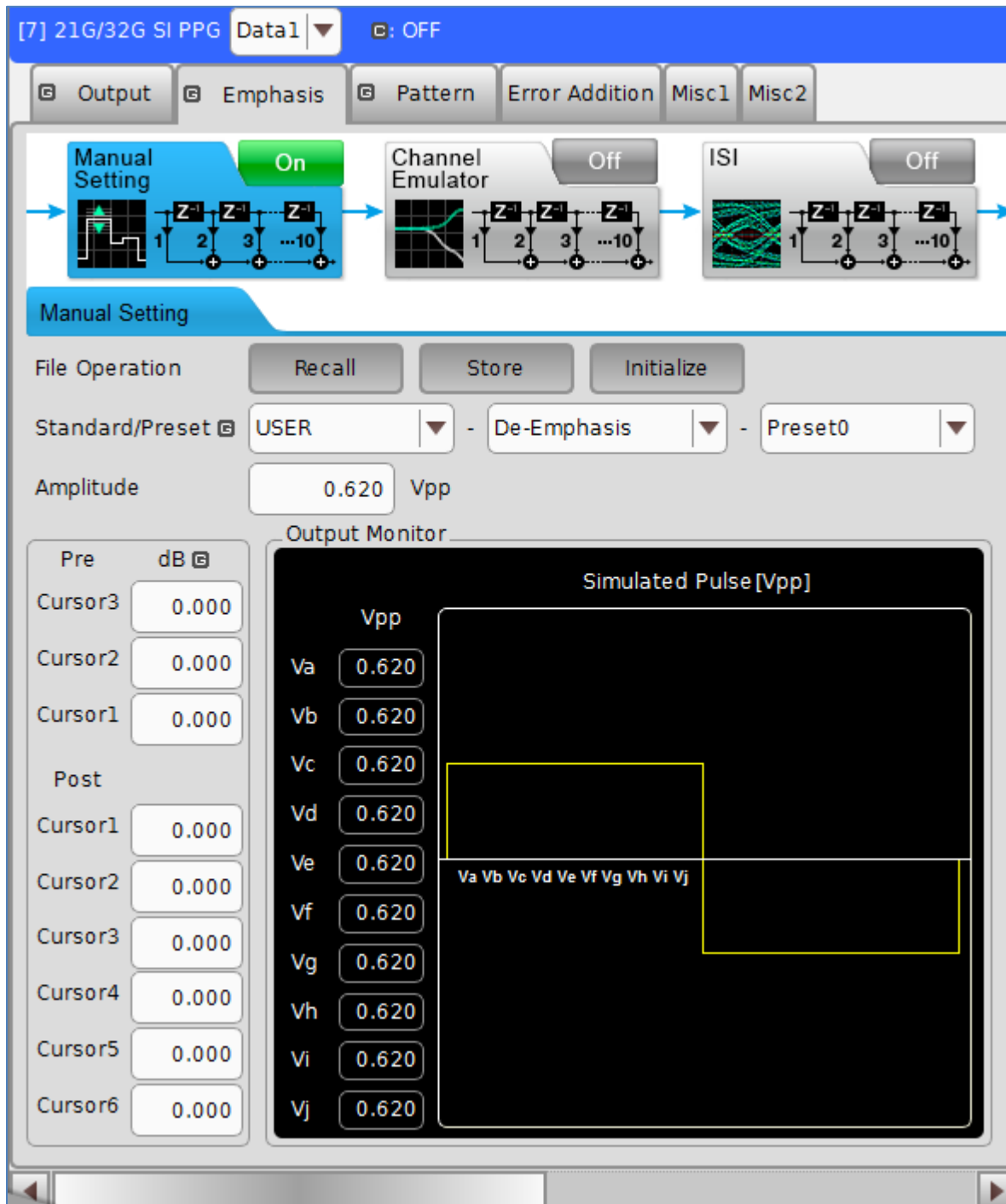


FIGURE 103. EYE AMPLITUDE



FIGURE 104. EYE AMPLITUDE MEASUREMENTS

16. Measure the Eye Width at $\pm 2.5\text{mV}$. If the Eye Width is not within the $540 \pm 50\text{mUI p-p}$ specification, tune RJ (if the SJ frequency is below 100MHz) or tune SJ (if the SJ frequency is 100MHz) so that the Eye Width is within specification.
17. Capture screen shot.
18. Save BERT Setup to "135G_TC2_100MHz".
19. Repeat steps #1 to #11 for 1MHz, 2MHz, 10MHz and 50MHz PJ frequencies, saving each setup as 135G_TC2_1MHz, 135G_TC2_2MHz, 135G_TC2_10MHz and 135G_TC2_50MHz respectively.

8.6 Calibrate and Save for UHBR20 (20.0 Gbit/s) Receiver at TP1

The initial setups for the BERT and Scope are the same as defined for the 10Gb/s section above, except for the settings highlighted in **bold** below.

1. Set up the physical equipment connections without the ISI channel, as per Figure 34.
2. Set up the BERT as follows:
 - a) Set the Data Rate to **20Gb/s**.
 - b) Set the Pattern to PRBS15.
 - c) Turn on "SSC", with settings of 32kHz (for 20G) with 5600ppm (for 20G) triangle down spread. (SSC will remain ON for all of the following steps.)
 - d) Set DATA+/DATA- Launch Amplitude to 750mV. This should set the differential amplitude just above the 700mV Eye Height target value as an initial value.
 - e) Set the initial CM interference amplitude to 0mV.

8.6.1 Set Up Oscilloscope

8.6.1.1 Oscilloscope Vertical and Horizontal Setup

Set up the Scope as listed in Table 21.

TABLE 21. OSCILLOSCOPE VERTICAL AND HORIZONTAL SETUP

Setting	Setup
Vertical	Ch1-Ch3 (using the full range of the Scope's D/A)
Horizontal	20Gb/s
Record Length	40M
Sample Rate	80Gs/s
Averaging	OFF
Sample Mode	Real Time
Bandwidth	21GHz (The Calibration Bandwidth is limited to the Bit Rate of the signal, which is $2 * 1^{\text{st}}$ harmonic. This is done intentionally to be on the order of a Thunderbolt Receiver's Bandwidth. This is essentially acting as an "Electrical Reference Receiver", used for calibration. It reduces the noise measured by the Scope which a real Receiver will never perceive.)

Vertical Scale	Set to full screen without clipping
Sin x/x	OFF

8.6.1.2 Oscilloscope Clock Recovery Setup

Enter the Clock Recovery menu and set up the Scope as listed in Table 22.

TABLE 22. OSCILLOSCOPE CLOCK RECOVERY SETUP

Setting	Setup
Nominal Data Rate	20Gb/s
Clock Recovery Method	Second Order PLL
PLL Specification	OJTF Loop Bandwidth: 5.000 MHz Damping factor: 0.94

8.6.1.3 Oscilloscope AC Common Mode (ACCM) Setup

Set up the Scope as listed in Table 23.

TABLE 23. OSCILLOSCOPE ACCM SETUP

Setting	Setup
Sample Rate	$\geq 80\text{Gs/s}$
Record Length	27Mpts per channel
Bandwidth	21GHz
Vertical Scale	20mV/div
CDR	OFF
Averaging	OFF
Sin x/x	OFF

8.6.1.4 Jitter Setup

Enter the Jitter menu and set up the Scope as listed in Table 24.

TABLE 24. OSCILLOSCOPE JITTER SETUP

Setting	Setup
Units	Unit Interval
Jitter Method	Spectral
Source for Jitter & Eye Diagram	Channel 1-3
BER Level	1E-12

Pattern	Periodic, Repeating Pattern ($2^{15}-1 = 32,767$ bits)
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8.6.1.5 Eye Diagram Vertical Setup

Set up the Scope as listed in Table 25.

TABLE 25. OSCILLOSCOPE EYE DIAGRAM VERTICAL SETUP

Setting	Setup
Vertical Scale	200 mV/div
Horizontal Scale	2 UI's
Eye Mask Height	96 mV (for final Eye Height Calibration)
Eye Mask Width	520 mUI

8.6.2 Record ISI Measurements

- Step through the Preset Coefficients 0-15 and use the Preset which yields the minimum DDJ Measurement. Although this is not a Calibrated value, record this ISI Measurement as part of the measurements table.
- Change the pattern on the BERT to PRBS31. Calibrate ACCM to be 100mVpp at 400MHz Clock, using the ACCM Scope Setup.
- Return CM Amplitude to zero.
- Turn on all remaining Jitter terms (RJ-Filtered [10MHz HPF] and SJ at 100MHz).
- Set all jitter amplitudes to zero.
- Return the Scope setup to the setup in Section 8.6.1.
- Change the pattern on the BERT to PRBS15.
- Calibrate RJ Amplitude to 115mUI peak-to-peak (9.58mUI RMS).
- Return amplitude to zero.
- Capture screen shot.
- Calibrate SJ Amplitude to 170mUI peak-to-peak at 100MHz.
- Capture screen shot.
- Return all remaining impairment sources (CM, RJ, SJ) to their calibrated values.
- Calibrate the TJ measurement to $360\text{mUI} \pm 25\text{mUI}$ using SJ Amplitude control (for SJ Frequency of 100MHz) and RJ Amplitude control (for SJ Frequencies of less than 100 MHz) as an adjustment on the BERT.
- Capture screen shot.
- Change the pattern on the BERT to PRBS31.
- Calibrate Inner Eye Height to 700mV (top and bottom of triangle eye mask, with V:700mV; H:620mUI).
- Capture screen shot.

19. Save BERT Setup to “20G_TC1_100MHz”.
20. Repeat steps #1 to #18 for 1MHz, 2MHz, 10MHz and 50MHz PJ frequencies, saving each BERT Setup as 20G_TC1_1MHz, 20G_TC1_2MHz, 20G_TC1_10MHz and 20G_TC1_50MHz.

8.7 Calibrate and Save for UHBR20 (20.0 Gbit/s) Receiver at TP3_EQ

For this test case, the total ISI of a channel should be around -16.5dB@10GHz. The test fixture should have 1 to 1.5dB per mated pair.

1. Recall the BERT setup from 20G_TC1_100MHz.
2. Connect the physical setup with ISI Channel, as per Figure 37.
3. Search for Optimized DC Gain starting from DC Gain of 1 in Oscilloscope Equalization Setup, adjust the DC Gain to obtain the largest Eye Height with cable de-embedding.
 - a) Set up the Scope as follows for CTLE:
 - i) Number of Poles set to “2 Poles, AC Gain”
 - ii) DC Gain set to 1.00
 - iii) AC Gain set to 1.41
 - iv) Pole #1 Frequency set to 5 GHz
 - v) Pole #2 Frequency set to 10 GHz
 - b) Use the DC Gain Setting in Table 26 which yields the largest Eye Height.

TABLE 26. DC GAIN SETTINGS

Index	DC Gain Setting	Index	DC Gain Setting
0	1.000	-5	0.562
-1	0.891	-6	0.501
-2	0.794	-7	0.446
-3	0.708	-8	0.398
-4	0.630	-9	0.354

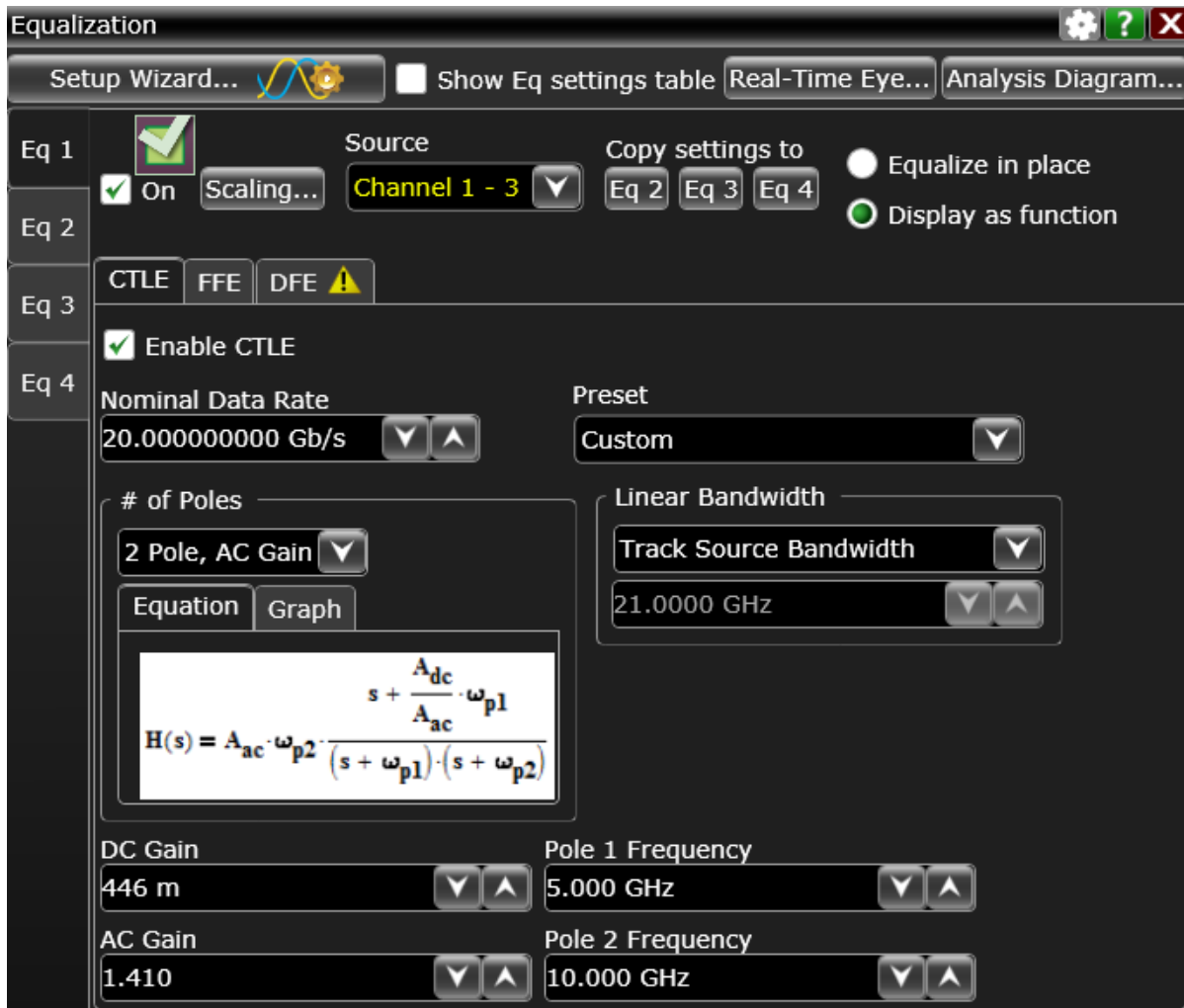


FIGURE 105. DC GAIN SETTING

- c) Set up the DFE:
- i) Set Max Tap to 50mV.
 - ii) Run Auto DFE.

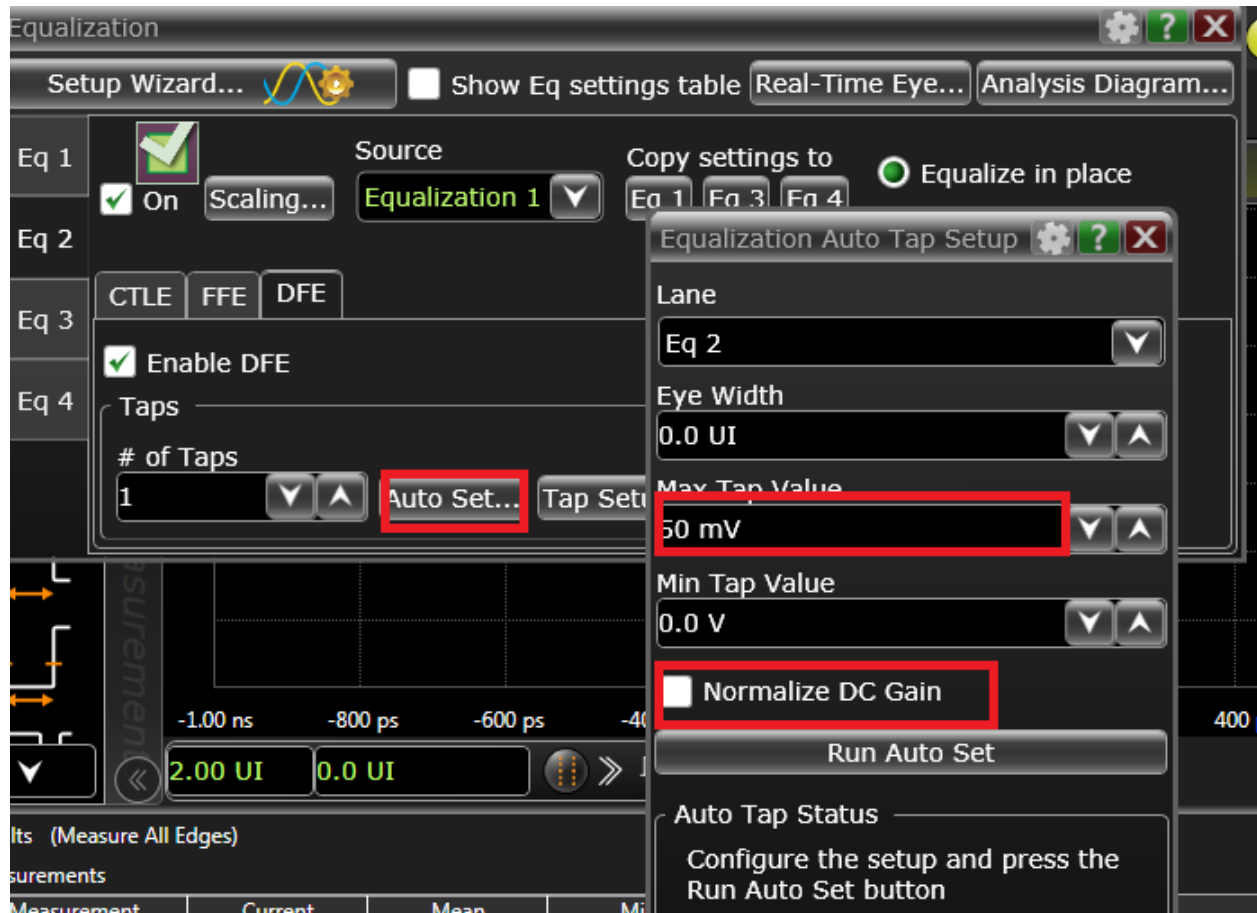


FIGURE 106. DFE SETTING

- d) Adjust the memory depth to capture 1,000,000 (1E6) bits with 5 acquisitions (100,000 UI's per Acquisition).
 - e) For each acquisition, measure the Eye Width and Eye Height. Calculate the average of the five measurements and compute the Eye area via *Eye Width * Eye Height*.
 - f) Measure the Eye area by iterating through each CTLE gain. The CTLE gain with the biggest Eye area is used for the following measurements.
20. Calibrate the Inner Eye Height to $96 \pm 10\text{mV}$ diff p-p (top and bottom of the triangle eye mask) using the PRBS31 pattern.

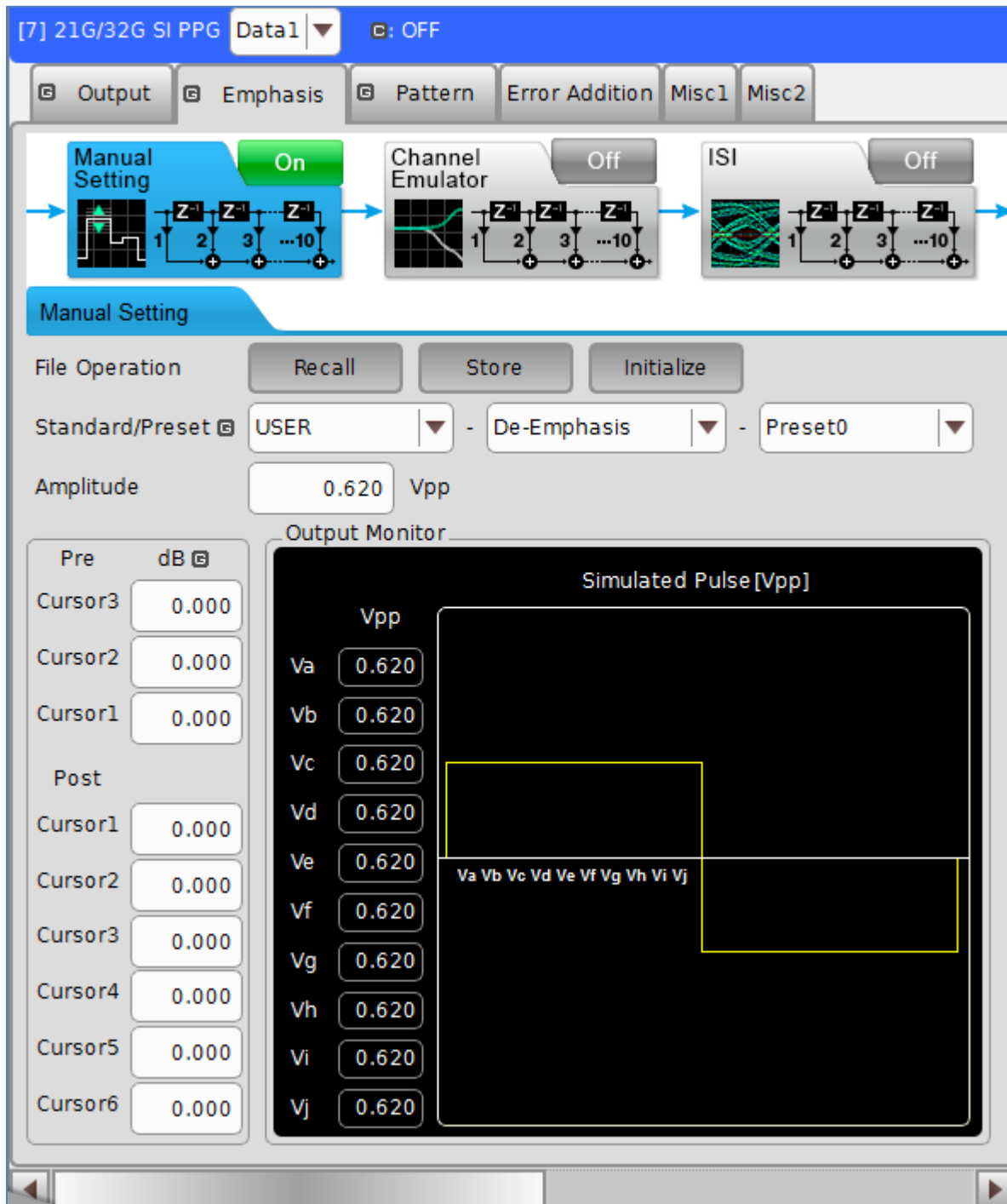


FIGURE 107. EYE AMPLITUDE



FIGURE 108. EYE AMPLITUDE MEASUREMENTS

21. Measure the Eye Width at $\pm 2.5\text{mV}$ from 0mV. If the Eye Width is not within the $520 \pm 50\text{mUI}$ p-p specification, tune RJ (if the SJ frequency is below 100MHz) or tune SJ (if the SJ frequency is 100MHz) so that the Eye Width is within specification.
22. Capture screen shot.
23. Save BERT Setup to "20G_TC2_100MHz".
24. Repeat steps #1 to #11 for 1MHz, 2MHz, 10MHz and 50MHz PJ frequencies, saving each setup as 20G_TC2_1MHz, 20G_TC2_2MHz, 20G_TC2_10MHz and 20G_TC2_50MHz respectively.

9 Appendix B: Connecting Keysight Oscilloscope to PC

If using a Keysight oscilloscope, refer to the following procedure on how to connect the Scope to be used with a control PC. The Keysight Scope can be connected to the control PC through GPIB, USB or LAN.

1. Download the latest version of the Keysight IO Libraries Suite software from the Keysight website and install on the control PC.
2. When installed successfully, the IO icon () will appear in the taskbar notification area of the control PC.
3. Select the IO icon to launch the **Keysight Connection Expert**.
4. Click Rescan.

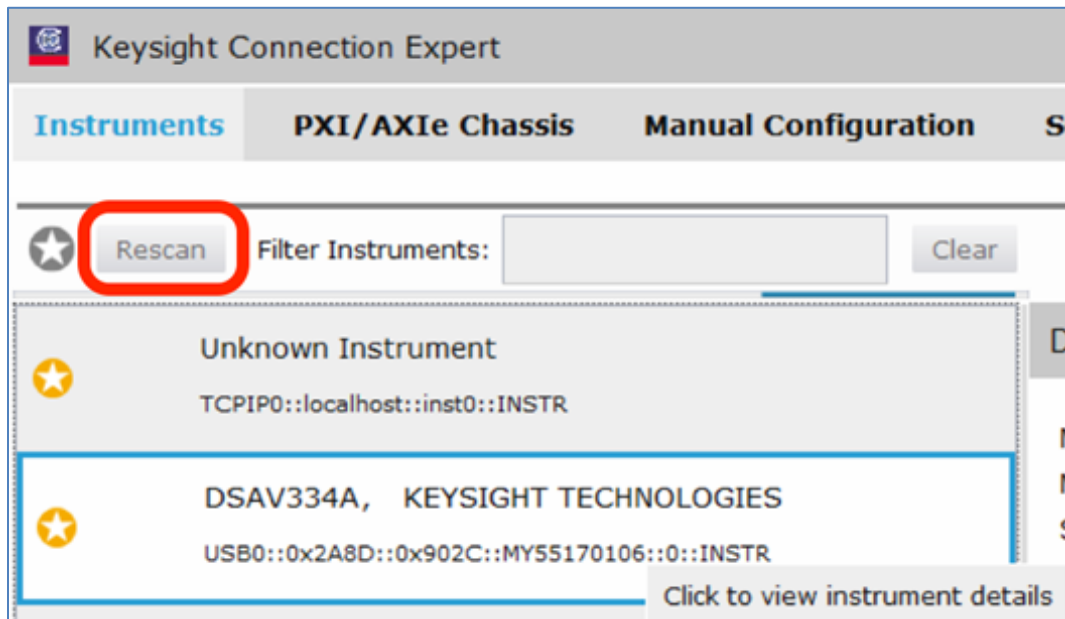


FIGURE 109. KEYSIGHT CONNECTION EXPERT

5. Refresh the system. The Keysight Scope is shown on the left pane and the VISA address is shown on the right pane.

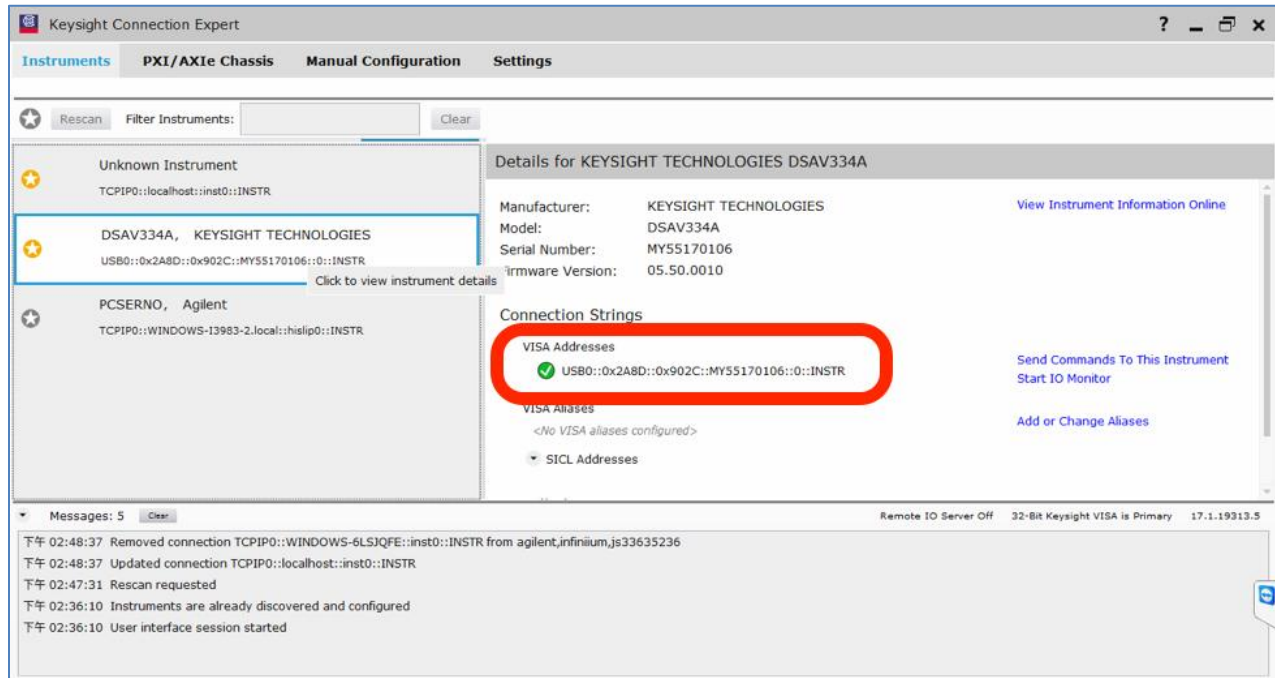


FIGURE 110. OSCILLOSCOPE'S VISA ADDRESS

6. When connecting the Keysight Scope to the PC through GPIB/USB, type in the VISA address into the 'Address' field on the Equipment Setup page of the GRL-Anritsu DisplayPort Sink 2.1 Test Application. If the GRL-Anritsu DisplayPort Sink 2.1 Test Application is installed on the Keysight Scope, type in the Scope IP address, for example "TCPIP0::127.0.0.1::inst0::INSTR". If the GRL Platform Solutions software is installed on the control PC to control the Scope via LAN, type in the Scope IP address, for example "TCPIP0::192.168.0.100::inst0::INSTR". Note to **omit** the Port number from the address.

If there is error in connection, type in the Scope IP address as "TCPIP0::192.168.0.100::5025::SOCKET".

10 Appendix C: Connecting Tektronix Oscilloscope to PC

If using a Tektronix DPOJET Series oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Tektronix Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Tektronix TekVISA software from the Tektronix website and install on the PC.
2. When installed successfully, open the OpenChoice Instrument Manager application.

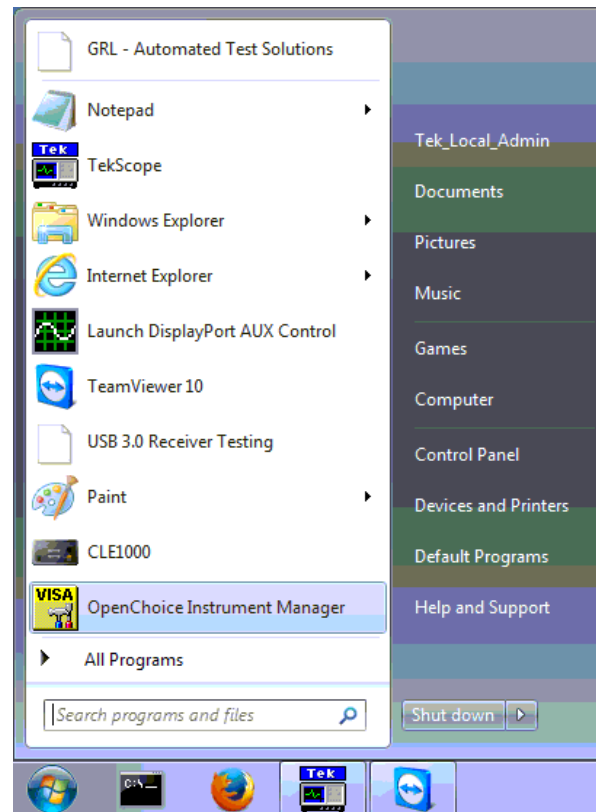


FIGURE 111. OPENCHOICE INSTRUMENT MANAGER IN START MENU

3. The left “Instruments” panel on the OpenChoice Instrument Manager will display all connected instruments. The functional buttons below the “Instruments” panel – “Instrument List Update”, “Search Criteria”, “Instrument Identify” and “Properties” can be used to detect the Scope in case it does not initially appear under “Instruments”.
 - a) “Instrument List Update”: Select to refresh the instrument list and locate new instruments connected to the PC.
 - b) “Search Criteria”: Select to configure the instrument search function.
 - c) “Instrument Identify”: Select to use a supported programming language to send a query to identify the selected instrument.
 - d) “Properties”: Select to display and view the selected instrument properties.

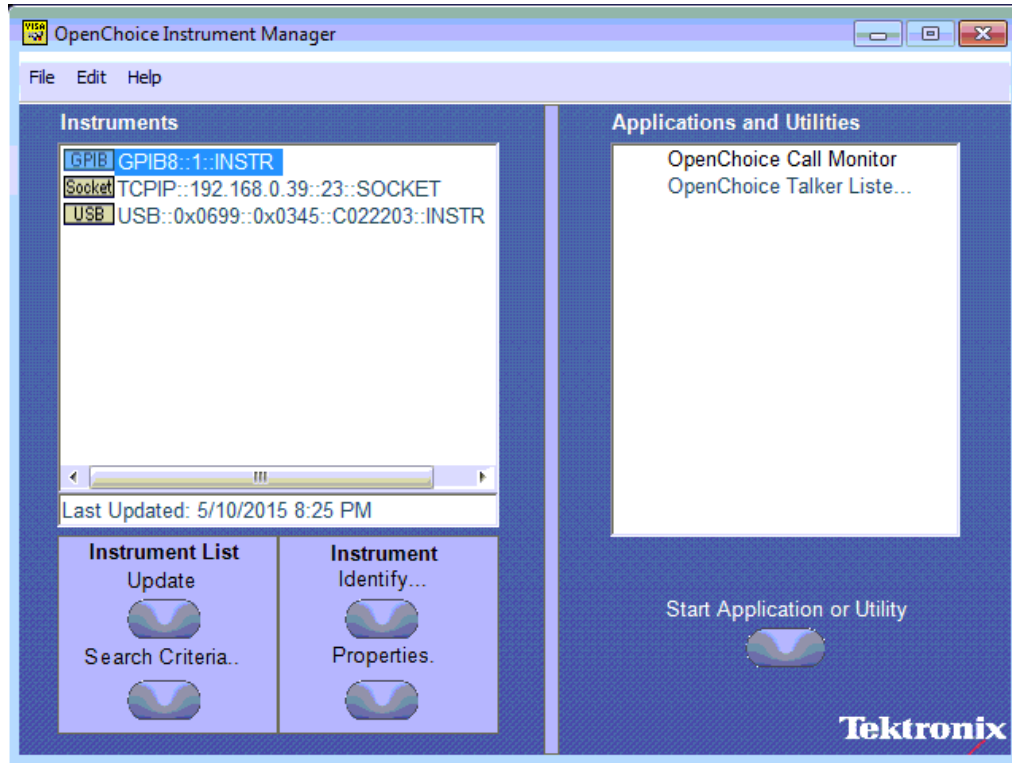


FIGURE 112. OPENCHOICE INSTRUMENT MANAGER MENU

4. If connecting the Tektronix Scope to the PC via USB, select the “Search Criteria” function to ensure that USB connection is enabled, and then select the “Instrument List Update” function. When the Scope appears on the “Instruments” panel, select it and then go to the “Instrument Identify” function. This will display the model and serial number of the Scope once detected. Select the “Properties” function to view the Scope address.
5. If connecting the Tektronix Scope to the PC via LAN, the Scope IP address must be pre-determined beforehand. Then select the “Search Criteria” function to ensure that LAN connection is enabled and type in the Scope IP address. When the Scope shows up in the list, select it followed by “Search”. The Scope should then appear on the “Instruments” panel. Select it and access the “Instrument Identify” function to view the Scope model and serial number as well as the “Properties” function to view the Scope address.
6. On the Equipment Setup page of the GRL Platform Solutions DisplayPort Sink 2.1 Test Application, type in the Scope address into the ‘Address’ field. If the DisplayPort Sink 2.1 Test Application is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example “GPIB8::1::INSTR”. If the GRL Platform Solutions software is installed on the PC to control the Scope, type in the Scope IP address, for example “TCPIP0::192.168.0.110::inst0::INSTR”. Note to **omit** the Port number from the address.

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