



GRL Platform Solutions

**GRL-PXE-TX PCI Express® 6.0 Transmitter Compliance
Test Automation Solution**

**Quick Start/User Guide/Method of Implementation (MOI)
for PCIe Gen6 Physical Layer Transmitter Test
Application**



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TABLE OF CONTENTS

1	INTRODUCTION	5
2	RESOURCE REQUIREMENTS	6
2.1	EQUIPMENT REQUIREMENTS	6
2.2	SOFTWARE REQUIREMENTS	7
3	SETTING UP GRL-PXE-TX AUTOMATION SOFTWARE	8
3.1	DOWNLOAD GRL-PXE-TX SOFTWARE.....	8
3.2	LAUNCH AND SET UP GRL-PXE-TX SOFTWARE	8
3.2.1	Set Up Remote File Server	11
3.3	PRE-CONFIGURE GRL-PXE-TX SOFTWARE BEFORE TESTING	13
3.3.1	Enter Test Session Information.....	13
3.3.2	Set Test Conditions	13
4	TESTING USING GRL-PXE-TX	15
4.1	GRL-PXE-TX ADVANTAGE	15
4.2	SET UP DUT TX TEST WITH AUTOMATION.....	15
4.2.1	Connect Equipment for System Board DUT Test.....	15
4.2.2	Connect Equipment for Add-In Card DUT Test.....	26
4.2.3	Connect Equipment for System Ref Clock Jitter Test.....	36
4.2.4	Connection Setup for Scope Intrinsic Noise Measurement (For PCIe Gen6).....	37
4.2.5	Set Up Test Requirements	37
4.2.6	Select Compliance Tests	40
4.2.7	Configure Test Parameters.....	43
4.3	RUN AUTOMATION TESTS	50
5	INTERPRETING GRL-PXE-TX TEST REPORT	51
5.1	UNDERSTAND TEST REPORT INFORMATION.....	51
5.1.1	Test Session Information.....	51
5.1.2	Test Summary Table.....	52
5.1.3	Test Results	52
5.2	DELETE TEST RESULTS.....	53
6	SAVING AND LOADING GRL-PXE-TX TEST SESSIONS	54
7	APPENDIX A: METHOD OF IMPLEMENTATION (MOI) FOR MANUAL PCIe 6.0 TRANSMITTER MEASUREMENTS	55
7.1	SYSTEM BOARD TX SIGNAL QUALITY TEST	55
7.2	ADD-IN CARD TX SIGNAL QUALITY TEST	57
7.3	SYSTEM BOARD TX PRESET TEST	58
7.4	ADD-IN CARD TX PRESET TEST.....	59
7.5	ADD-IN CARD TX BASE JITTER (UPW-TJ, UPW-DJDD, UTJ AND UDJDD) TEST	61

7.6	SYSTEM BOARD REF CLOCK (100 MHz) JITTER TEST.....	62
8	APPENDIX B: SIGTEST TOOL TAB	63
9	APPENDIX C: CONNECTING KEYSIGHT OSCILLOSCOPE TO PC	65
10	APPENDIX D: CONNECTING TEKTRONIX OSCILLOSCOPE TO PC	66

1 Introduction

This Quick Start/User Guide/MOI provides information using the GRL-PXE-TX test solution to set up and test an electrical transmitter (Tx) device for PCI Express (PCI-SIG SEG) certification.

The main body of this documentation describes how to configure the GRL-PXE-TX solution to capture and test waveforms in a PCIe 6.0 (or below) system (lane, data rate, preset), or individual waveforms, and perform SigTest signal quality and de-emphasis compliance tests. The GRL-PXE-TX solution also supports the Seasim software for PCIe Gen6 stressed eye validation. The test automation is carried out based on PCI-SIG-approved Methods of Implementation (MOI's) with high performance real-time oscilloscopes using existing PCI-SIG Compliance Base Boards (CBB's) and Compliance Load Boards (CLB's).

The GRL-PXE-TX solution consists of the GRL Platform Solutions PCIe "GRL-P1" hardware controller and automation software (GRL-PXE-TX). The GRL-PXE-TX software when run from the computer or oscilloscope enables automation control to test the device under test (DUT) for Tx electrical compliance. The GRL-P1 hardware controller is designed to work primarily with the GRL Platform Solutions software to provide compliance toggle to control the state of the DUT. Alternatively, an arbitrary function generator can also be used as a secondary option for compliance toggle control. The GRL Platform Solutions test solution also extends support for RF switch integration to automate switching or selection of the lane under test.

The GRL Platform Solutions automation control enabled PC or scope automates power and signal quality test sequencing and processing of captured waveforms for the DUT at the selected PCIe data rate. The Tx path is tested with worst case eye to ensure a Bit Error Ratio (BER) of less than $1E-12$ can be achieved. When combined with a satisfactory level of interoperability testing, these tests provide a reasonable level of confidence that the DUT's will function properly in most PCIe environments.

This documentation covers the following major components for PCIe Tx testing.

1. GRL-P1 hardware controller setup.
2. GRL-PXE-TX software configuration and test setup.

Note: For manual test methodology, please refer to PCI-SIG SEG for approved vendor specific Method of Implementation (MOI's) as technical reference.

2 Resource Requirements

Note: Equipment requirements may vary according to the lab setup and DUT board. Below are the recommended lists of equipment for the typical test setup.

2.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS – SYSTEMS

Equipment	Qty.	Description/Key Spec Requirement
High Performance Real-time Oscilloscope	1	• ≥ 25 GHz bandwidth (For PCIe Gen4 and below) • ≥ 33 GHz bandwidth (For PCIe Gen5 & 6), with sample rate of ≥ 128 Gb/s with 2x interpolation • Scope measurement software, e.g. Keysight InfiniiSim for Keysight scope or Tektronix DPOJET for Tektronix scope
“GRL-P1” PCIe Compliance Test Hardware Controller (Optional)	1	For PCIe compliance toggle control
Advanced Technology eXtended (ATX) Power Supply	1	For power supply to the DUT
GRL Platform Solutions Switch (Optional)	1	For multi-lane automated testing
PCI-SIG Compliance Base Board (CBB) or PCI-SIG Compliance Load Board (CLB)	1	For add-in cards For hosts
Computer/PC (laptop or desktop)	1	For automation control Minimum requirements: • Windows 10+ OS • Intel Core i5 processor • 120GB SSD storage • 16GB RAM • Gigabit Ethernet Recommended requirements: • Windows 10+ OS • Intel Core i7+ processor • 200GB SSD storage • 32GB RAM • Gigabit Ethernet

TABLE 2. EQUIPMENT REQUIREMENTS – CABLES

Cable	Qty.
Power Control Adapter Cable	1
USB Type-A to Type-A/B Micro Cable	1
Test Fixture Control Cable (2-conductor power control only cable or 6-conductor fixture control cable)	1
Clock Compliance Toggle Cables (matched SMA-to-SMP cables)	1 pair
SMA-to-SMP Cables	4 pairs ^[a]

^[a] Based on the standard test configuration. May require more or less cables depending on the DUT type.

2.2 Software Requirements

TABLE 3. SOFTWARE REQUIREMENTS

Software	Description/Source
GRL-PXE-TX	GRL Platform Solutions PCI Express® 6.0 Automated Transmitter Compliance Test Solution (hardware & software) – www.grlps.com Further automation license for Custom DUT, RF Switch, or other bench automation – www.grlps.com
VISA (Virtual Instrument Software Architecture) API Software	VISA Software is required to be installed on the control PC running GRL-PXE-TX software. GRL Platform Solutions' software framework has been tested to work with all three versions of VISA available on the Market: 1. NI-VISA: http://www.ni.com/download/ni-visa-17.0/6646/en/ 2. Keysight IO Libraries: www.keysight.com (Search on IO Libraries) 3. Tektronix TekVISA: www.tek.com (Downloads > Software > TekVisa)
SigTest	Standard Post Processing Analysis Software – www.intel.com/content/www/us/en/design/technology/high-speed-io/tools.html
Seasim	Seasim tool for post-processing analysis of the PCIe Gen6 captured waveform (Eye Opening simulation software) – www.pcisig.com

3 Setting Up GRL-PXE-TX Automation Software

This section provides the procedures to start up and pre-configure the GRL-PXE-TX automation software before running tests. It also helps users familiarize themselves with the basic operation of the software.

Note: The GRL-PXE-TX software installer will automatically create shortcuts in the Desktop and Start Menu when installing the software.

To start using the GRL-PXE-TX software, follow the procedures in the following sections.

3.1 Download GRL-PXE-TX Software

Download and install the GRL-PXE-TX software as follows:

1. If the GRL-PXE-TX software is to be installed on a PC (where is referred to as ‘control PC’), install VISA (Virtual Instrument Software Architecture) on to the PC where the GRL Platform Solutions software is to be used (see Section 2.2).
2. Download the software ZIP file package from the GRL Platform Solutions support site.
3. The ZIP file contains:
 - **PCIETxTestApplicationxxxxxxxxxxxxSetup.exe** – Run this on the PC or on the oscilloscope to install the GRL-PXE-TX application.
 - **PCIe_TxTestScopeSetupFilesInstallationxxxxxxxxSetup.exe** – Run this on the oscilloscope to install the scope setup files.

3.2 Launch and Set Up GRL-PXE-TX Software

1. Once the GRL-PXE-TX software is installed, open the GRL folder from the Windows Start menu. Click on **GRL – Automated Test Solutions** within the GRL folder to launch the GRL Platform Solutions software framework.

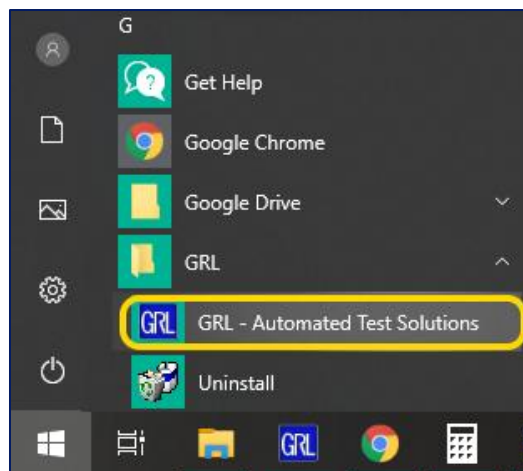


FIGURE 1. SELECT AND LAUNCH GRL PLATFORM SOLUTIONS FRAMEWORK

2. From the **Application → Framework Test Solution** drop-down menu, select **“PCIe Tx Test Application”** to start the PCIe Tx Test Application. If the selection is grayed out, it means that your license has expired.

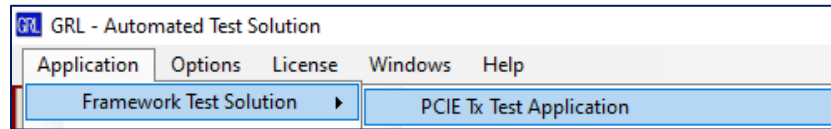


FIGURE 2. START PCIe TX TEST APPLICATION

3. To enable license, go to License → License Info.

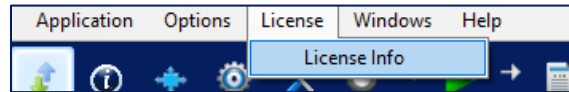


FIGURE 3. SEE LICENSE DETAILS

a) Check the license status for the installed application.

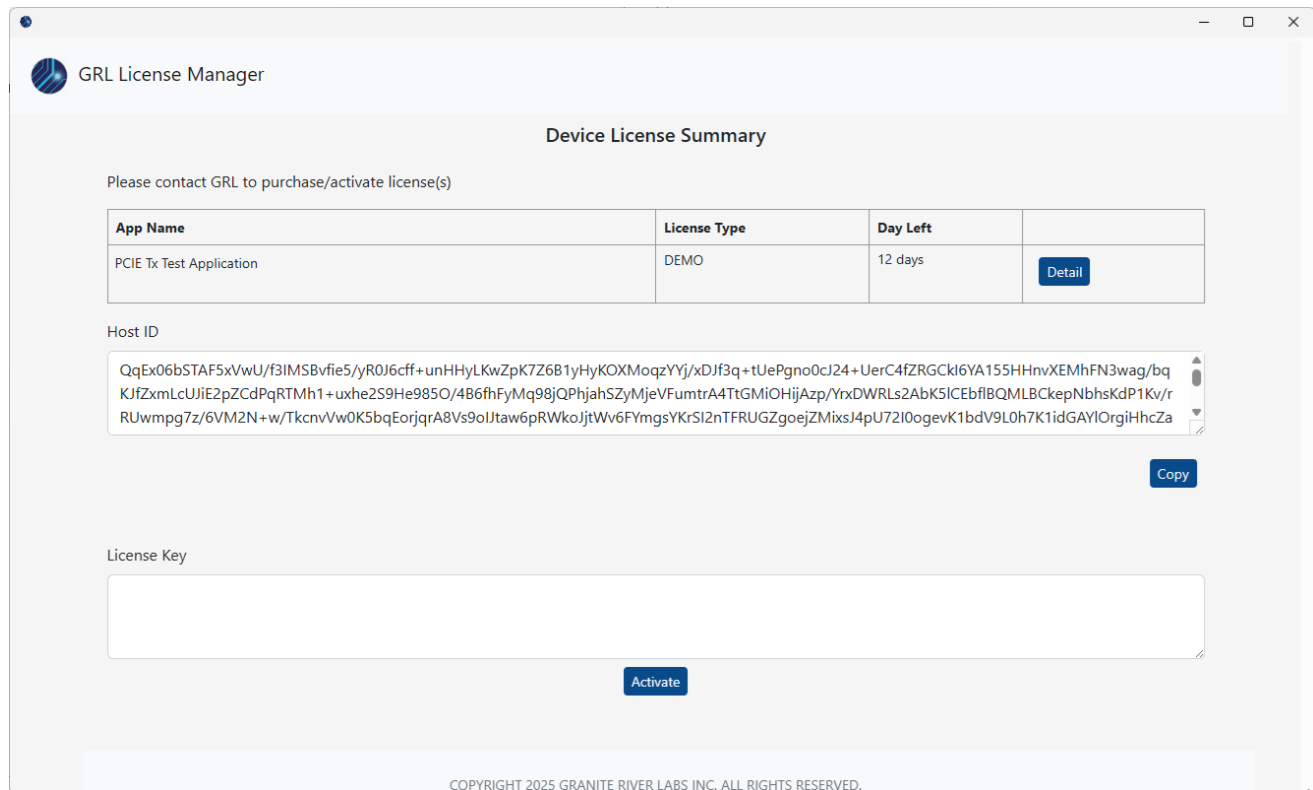


FIGURE 4. CHECK LICENSE FOR INSTALLED APPLICATIONS

b) Activate a License:

- If you have an Activation Key, enter it in the **License Key** field provided and select **Activate**. The installed application is ready for use upon successful activation.
- If you do not have an Activation Key, close the above window to use a demo version of the application over a free 12-day trial period.

Note: Once the 12-day trial period ends, you will need to request an Activation Key to continue using the application on the same computer by contacting support@grlps.com.

4. Select the Equipment Setup icon  on the PCIe Tx Test Application menu.

5. Connect the oscilloscope with the control PC through either GPIB, USB or LAN. (Note: Additional information for connecting the Keysight and Tektronix oscilloscopes to the control PC is provided in the Appendix of this document.)
6. If using an RF Switch, connect the switch via GPIB to the GRL Platform Solutions automation control enabled Scope or PC.
7. If using an Arbitrary Function Generator (AFG) as the compliance toggle control, connect the AFG via USB to the GRL Platform Solutions automation control enabled Scope or PC.
8. On the Scope or PC, obtain the network addresses for all the connected instruments from the device settings. These addresses will be used to connect the instruments to the GRL Platform Solutions automation software.
9. If using the GRL-P1 hardware controller, connect the controller via USB to the GRL Platform Solutions automation control enabled Scope or PC.
10. On the Scope or PC, obtain the network address for the connected GRL-P1 from the device settings. For example, if GRL-P1 is connected to the PC, open the Device Manager which should detect the controller as a Controller Serial (COM) Port, e.g. "GRL PCIe34 P1 (COM10)".
11. On the Equipment Setup page of the GRL-PXE-TX Test Application, type in the address of each connected instrument into the "Address" field.
12. (Note: If the GRL Platform Solutions software is installed on the **Tektronix Scope**, ensure the Scope is connected via GPIB and type in the GPIB network address, for example "GPIB8::1::INSTR".)

(Note: If the GRL Platform Solutions software is installed on the **Keysight Scope**, type in the Scope IP address, for example "TCPIP0::127.0.0.1::inst0::INSTR".)

If the GRL Platform Solutions software is installed on the PC to control the Scope, type in the Scope IP address, for example "TCPIP0::192.168.0.35::inst0::INSTR". Note to **omit** the Port number from the address.

(Note: If the GRL Platform Solutions software is installed on the **Keysight Scope**, and if there is error in connection, type in the Scope IP address as "TCPIP0::192.168.0.35::5025::SOCKET".)
13. If the GRL Platform Solutions software is installed on the PC to control the Scope, set up the Remote File Server as described in Section 3.2.1.
14. Then select the "lightning" button () for each connected instrument.

The "lightning" button should turn green () once the application has successfully established connection with each instrument.

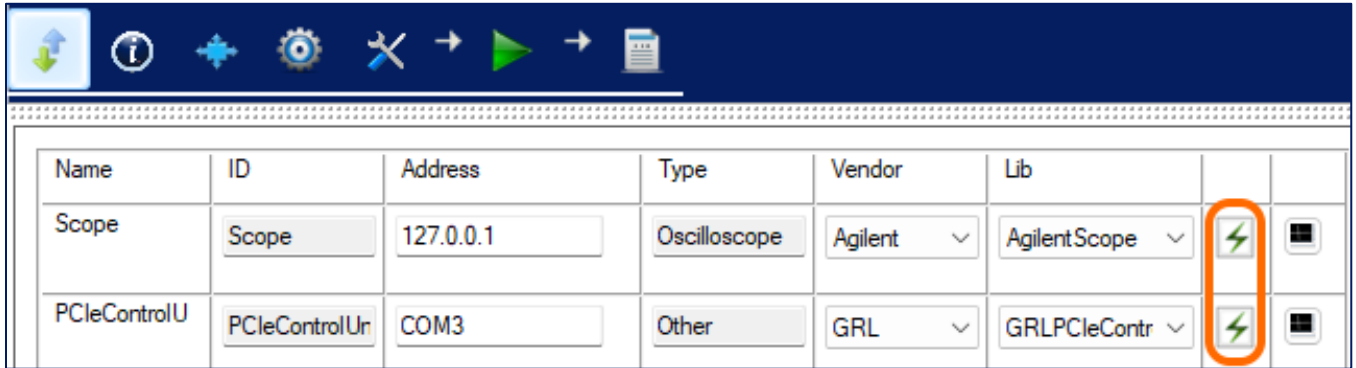


FIGURE 5. CONNECT INSTRUMENTS WITH GRL-PXE-TX SOFTWARE

3.2.1 Set Up Remote File Server

If the GRL-PXE-TX software is installed on the PC to control the Scope and SigTest is to be used, the GRL Platform Solutions Remote Proxy Server must be run on the Scope to move large waveform files (>17 Mpts acquisition points) back to the control PC. The GRL Platform Solutions software will then perform post-processing and analysis of these waveforms using SigTest.

Note: If the Remote Proxy Server is not run on the Scope, the acquisition process will fail.

The **GRLRemoteProxyServer.exe** will be installed along with the **PCle_TxTestScopeSetupFilesInstallationxxxxxxxxSetup.exe** on the Scope. The GRLRemoteProxyServer.exe is installed under the “C:\GRL\GRLRemoteProxyServer” directory.

Use the following procedure to set up the Remote Proxy Server.

1. Open the “C:\GRL\GRLRemoteProxyServer” folder on the Scope and run the **GRLRemoteProxyServer.exe** application.

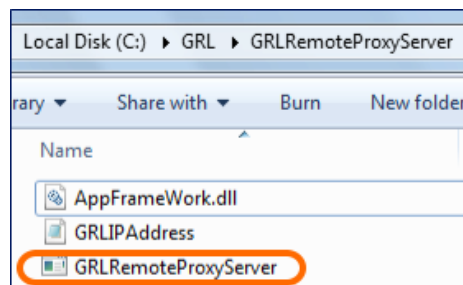


FIGURE 6. GRLREMOTEPROXYSERVER.EXE FILE DIRECTORY

2. When running the GRLRemoteProxyServer.exe, make sure that the control PC and Scope are connected to the same network, using IP addresses as in following example:
 - Control PC IP address: 192.168.100.8
 - Scope IP address: 192.168.100.35

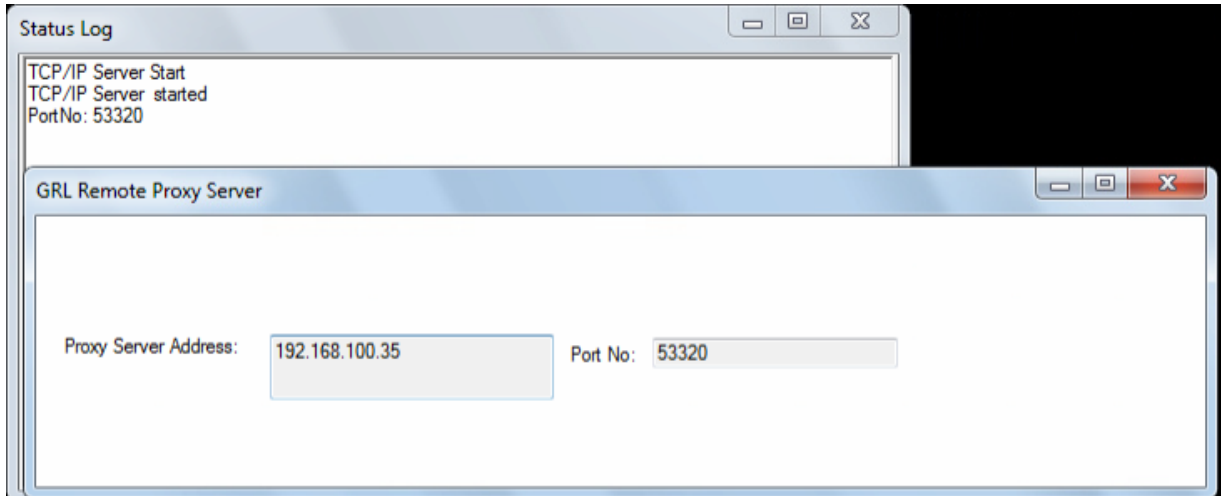


FIGURE 7. VERIFY PROXY SERVER CONNECTION FOR CONTROL PC AND SCOPE

3. On the GRL-PXE-TX software, configure the **Remote File Server IP Address** and **Remote File Server Port Number** parameters on the Configurations  page to match the network settings of the Remote Proxy Server as shown in the example below:

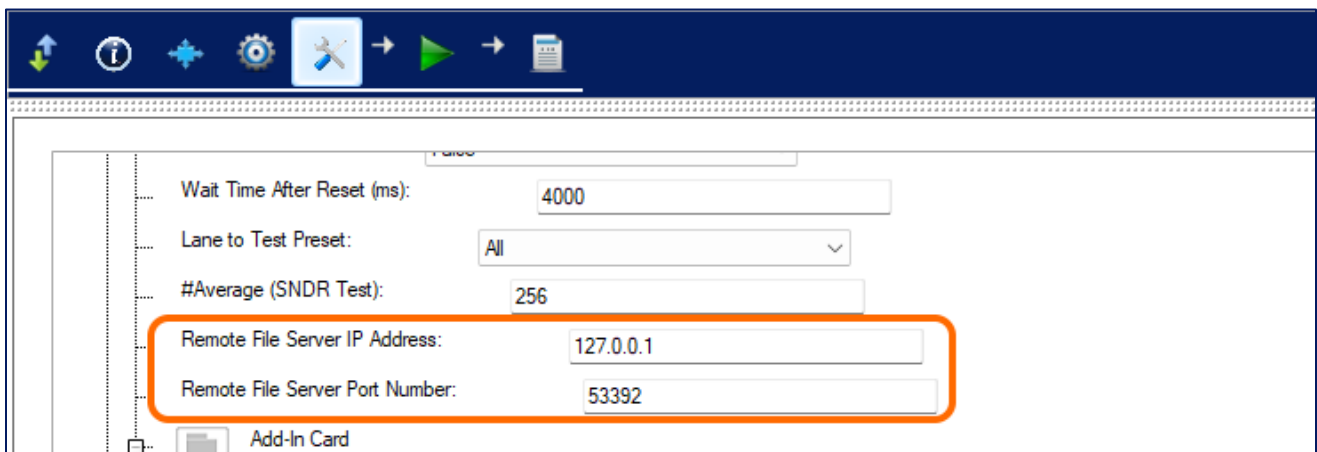


FIGURE 8. CONFIGURE REMOTE PROXY SERVER NETWORK SETTINGS ON GRL PLATFORM SOLUTIONS SOFTWARE

Refer Section 4.2.7 for more details on the parameters available in the Configurations page.

3.3 Pre-Configure GRL-PXE-TX Software Before Testing

Once all equipment is successfully connected from the previous section, proceed to set up the preliminary settings before going to the advanced test setup.

3.3.1 Enter Test Session Information

Select  from the menu to access the **Session Info** page. Enter the information as required for the test session that is currently being run. The information provided will be included in the test report generated by the software once tests are completed.

- The fields under **DUT Info** and **Test Info** are defined by the user.
- The **Software Info** field is automatically populated by the software.

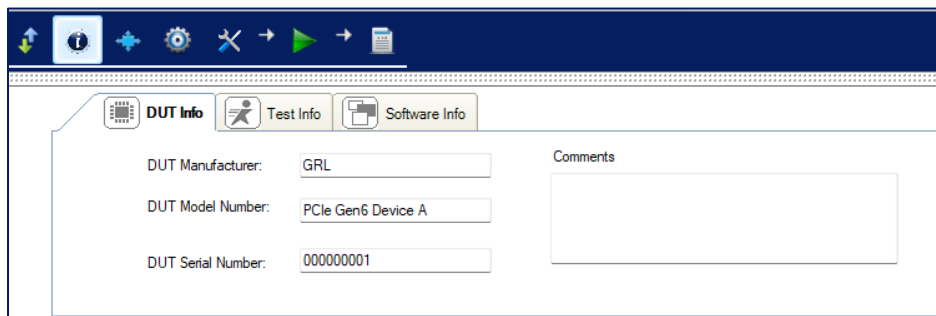


FIGURE 9. SESSION INFO PAGE

3.3.2 Set Test Conditions

Select  from the menu to access the **Conditions** page to set the conditions for testing. The software will run tests for the PCIe data lanes, data rates, and preset settings that are selected.

- Lane** tab: Select the desired data lanes to be tested.

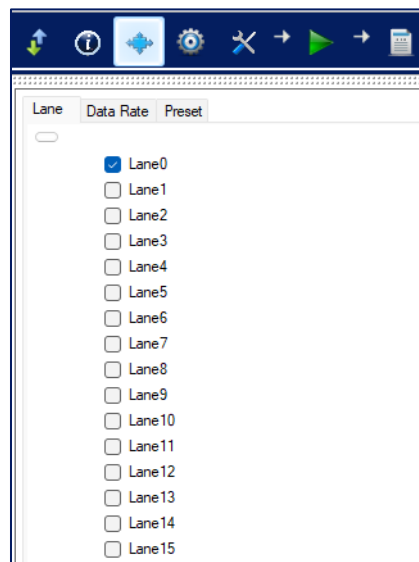


FIGURE 10. SELECT LANE UNDER TEST

b) **Data Rate** tab: Select the desired PCIe data rates for testing.

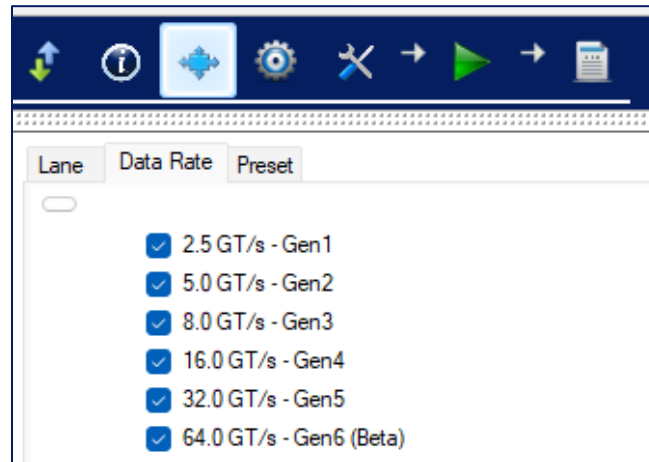


FIGURE 11. SELECT DATA RATES

c) **Preset** tab: Select the pre-defined Tx presets as required for Tx equalization.

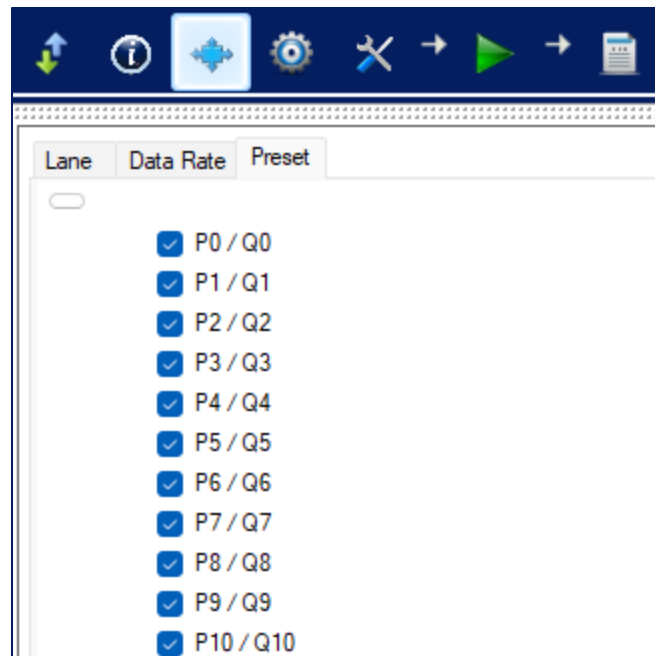


FIGURE 12. SELECT PRESETS

4 Testing Using GRL-PXE-TX

The GRL-PXE-TX test solution supports automated Tx compliance testing using the SigTest signal quality/de-emphasis and stress tolerance analysis application for PCIe system board and add-in card DUT's. Additionally, the Seasim software is also supported as a tool for PCIe Gen6 stressed eye validation.

In a typical test environment, the GRL-PXE-TX automation software is run from the PC/oscilloscope and communicates with the GRL-P1 hardware controller. This enables automation control for the DUT's power and signal quality test sequence, as well as waveform acquisition (for PCIe Gen1, Gen2, Gen3, Gen4, Gen5 and Gen6). Optionally an arbitrary function generator can also be used as an alternative compliance toggle controller.

The GRL-P1 controller can be connected to either a PCI-SIG compliance load board (CLB) test fixture for the system board DUT or compliance base board (CBB) test fixture for the add-in card DUT. The GRL Platform Solutions automation control enabled PC/Scope will send commands to the GRL-P1 which controls the power to the DUT and provides a compliance toggle signal to cause the DUT to enter the next compliance state.

The DUT will transmit the test signal to the oscilloscope that is used to validate the test pattern of the signal. The compliance signal will be captured and saved as a waveform file which is then measured for stress tolerance and preset test compliance. In between, an optional RF switch can be used and controlled by the GRL-PXE-TX software to automate selection of the lane under test. When testing is completed, the software will generate a test report detailing all results from all lanes tested.

4.1 GRL-PXE-TX Advantage

The GRL-PXE-TX test solution provides a more efficient way to perform PCIe Tx compliance testing rather than using traditional manually-driven methods that are generally both time-consuming and error prone, tying up valuable equipment and resources.

To increase test efficiency, the GRL-P1 controller will first quickly capture waveforms on the oscilloscope. Then using a separate computer, the GRL-PXE-TX software will run PCIe compliance tests for the waveforms, SigTest signal quality, and de-emphasis.

Through this offline processing of captured waveforms, the oscilloscope can be freed up for other work. The test time can also be further reduced with the software's multi-threading of SigTest. Another advantage is that GRL-P1 can be programmed to automatically capture only the waveforms for the test that the user wants to perform.

4.2 Set Up DUT Tx Test with Automation

Once pre-configuration has been completed from Section 3.3, continue with the test setup. The following procedures show how to set up the test environment to perform automated Tx compliance testing for both the System Board and Add-In Card DUT's.

4.2.1 Connect Equipment for System Board DUT Test

The connection diagrams below show the recommended equipment setups to perform waveform acquisition and analysis for the PCIe System Board DUT using a GRL Platform Solutions automation control enabled Scope and different test controller methods.

4.2.1.1 Setup Using GRL-P1 Hardware Controller with PCIe Test Fixtures

The following diagrams describe how to connect the equipment if using the GRL-P1 with the PCIe Gen4, Gen5 and Gen6 Compliance Load Boards (CLB's). *Note the use of GRL-P1 in the setup is optional.*

4.2.1.1.1 PCIe Gen4 System Board Connection Setup

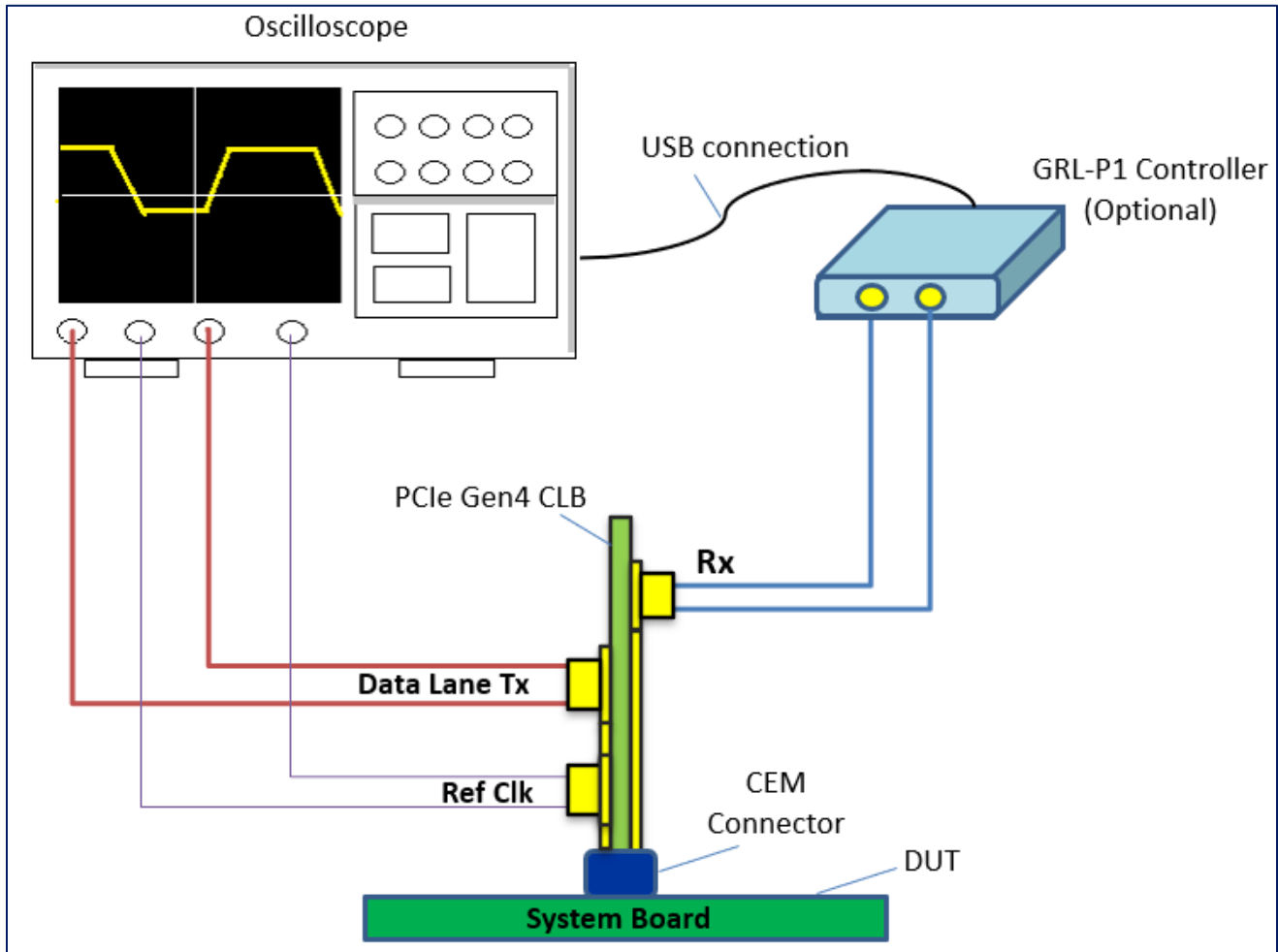


FIGURE 13. CONCEPTUAL PCIe GEN4 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITHOUT RF SWITCH)

1. Insert the CLB into the designated slot on the DUT.
2. Connect the Tx+ Data Lane from the CLB to Channel 1 of the Scope.
3. Connect the Tx- Data Lane from the CLB to Channel 3 of the Scope.
4. Connect Ref Clk+ from the CLB to Channel 2 of the Scope.
5. Connect Ref Clk- from the CLB to Channel 4 of the Scope.
6. Connect the CLB Rx+ Lane to the GRL-P1 Output 1.
7. Connect the CLB Rx- Lane to the GRL-P1 Output 2.
8. Connect the power control adapter cable from the ATX power supply to the DUT.
9. Connect the GRL-P1's power control only cable to the input of the power control adapter cable.

10. Connect GRL-P1 to the Scope using a USB cable.

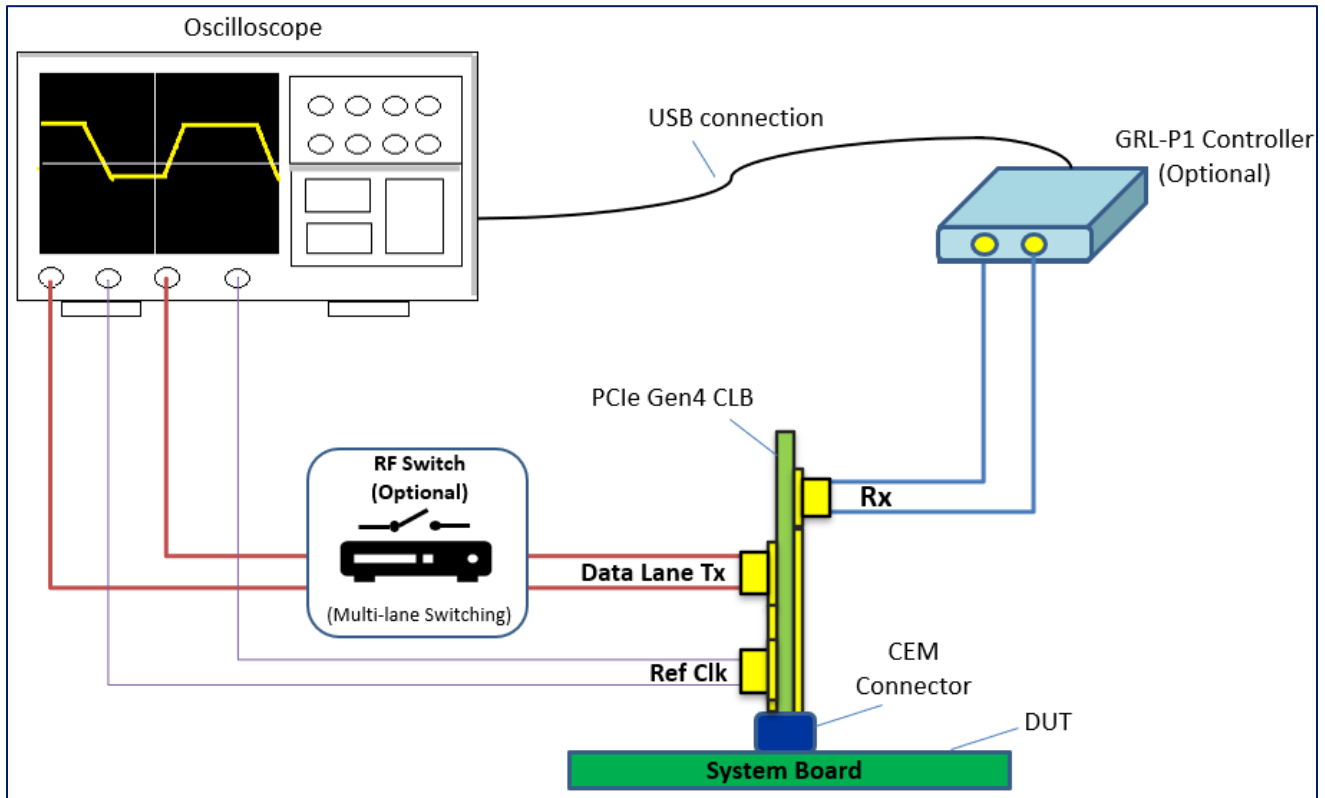


FIGURE 14. CONCEPTUAL PCIe GEN4 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH RF SWITCH)

Note the use of GRL-P1 and RF switch in the setup is optional.

1. Using the same connections from Figure 13, connect the Tx+ and Tx- Data Lanes from the CLB to the RF Switch Inputs.
2. Connect Output+ from the RF Switch to Channel 1 of the Scope.
3. Connect Output- from the RF Switch to Channel 3 of the Scope.
4. If using ISI, connect a 2 dB ISI in between the RF Switch outputs and Scope channels (Figure 15 below).

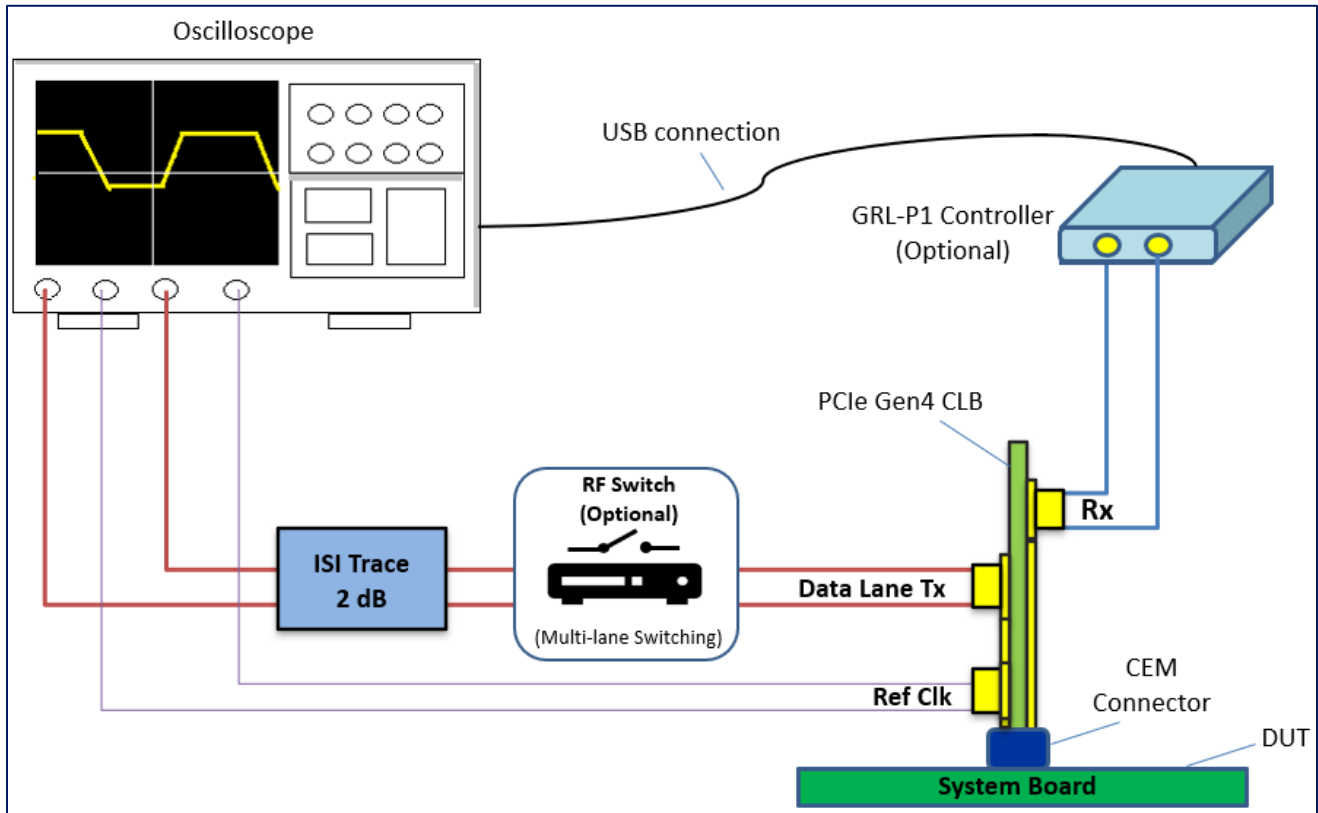


FIGURE 15. CONCEPTUAL PCIe GEN4 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH RF SWITCH AND ISI)

4.2.1.1.2 PCIe Gen5 System Board Connection Setup

Note the use of GRL-P1 in the setup is optional.

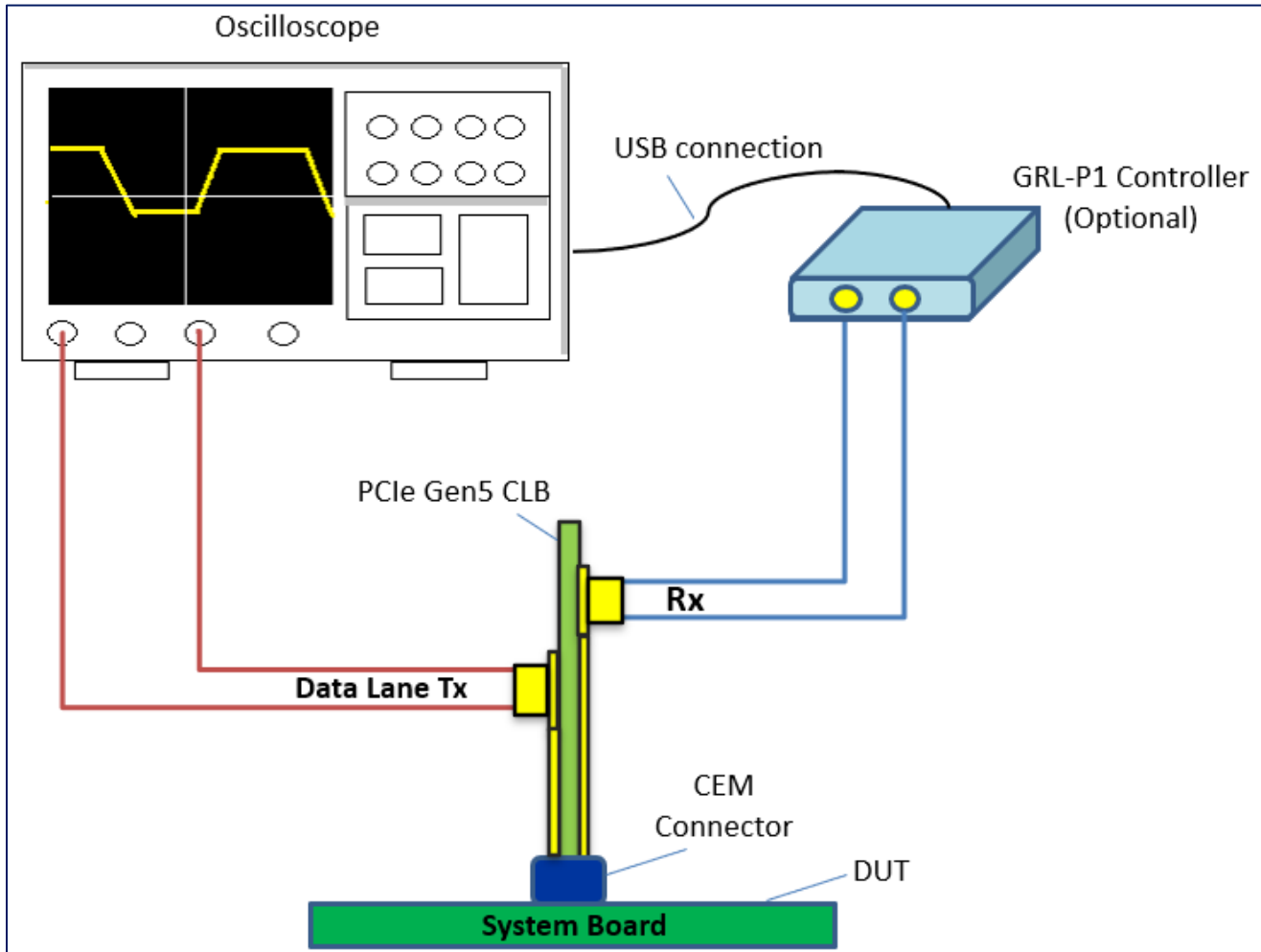


FIGURE 16. CONCEPTUAL PCIe GEN5 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITHOUT RF SWITCH)

1. Insert the CLB into the designated slot on the DUT.
2. Connect the Tx+ Data Lane from the CLB to Channel 1 of the Scope.
3. Connect the Tx- Data Lane from the CLB to Channel 3 of the Scope.
4. Connect the CLB Rx+ Lane to the GRL-P1 Output 1.
5. Connect the CLB Rx- Lane to the GRL-P1 Output 2.
6. Connect the power control adapter cable from the ATX power supply to the DUT.
7. Connect the GRL-P1's power control only cable to the input of the power control adapter cable.
8. Connect GRL-P1 to the Scope using a USB cable.

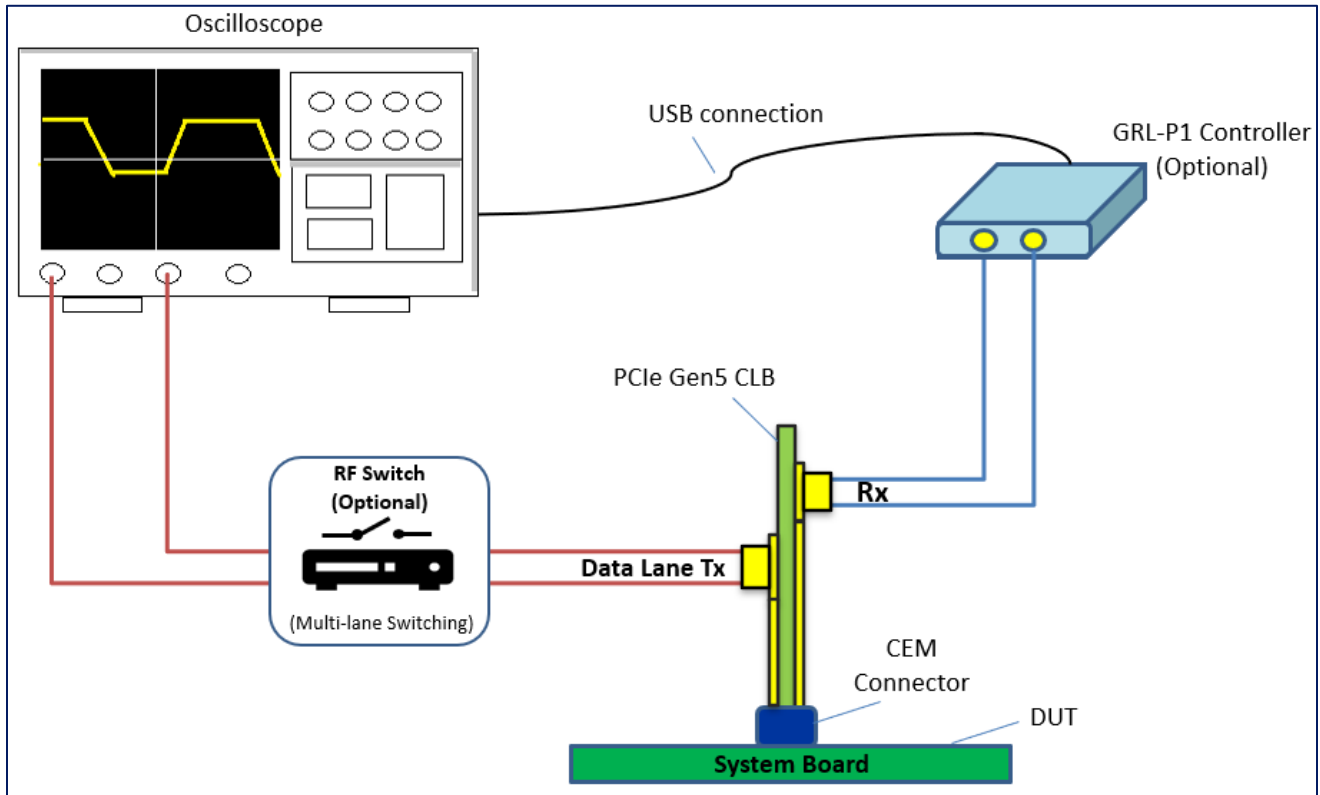


FIGURE 17. CONCEPTUAL PCIe GEN5 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH RF SWITCH)

Note the use of GRL-P1 and RF switch in the setup is optional.

1. Using the same connections from Figure 16, connect the Tx+ and Tx- Data Lanes from the CLB to the RF Switch Inputs.
2. Connect Output+ from the RF Switch to Channel 1 of the Scope.
3. Connect Output- from the RF Switch to Channel 3 of the Scope.
4. If using ISI, connect a 2.3 dB ISI in between the RF Switch outputs and Scope channels (Figure 18 below).

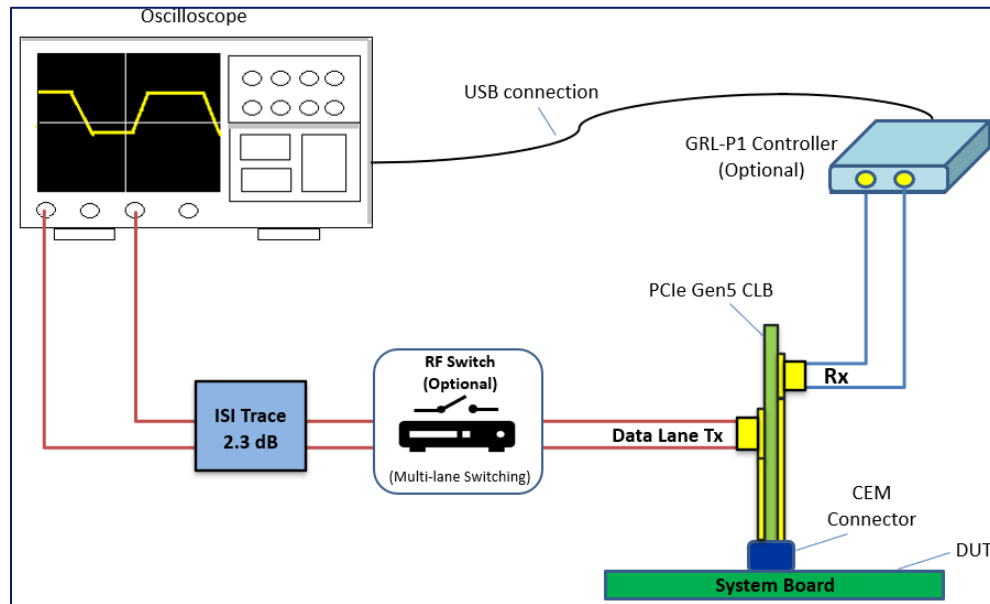


FIGURE 18. CONCEPTUAL PCIe GEN5 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH RF SWITCH AND ISI)

4.2.1.1.3 PCIe Gen6 System Board Connection Setup

Note the use of GRL-P1 in the setup is optional.

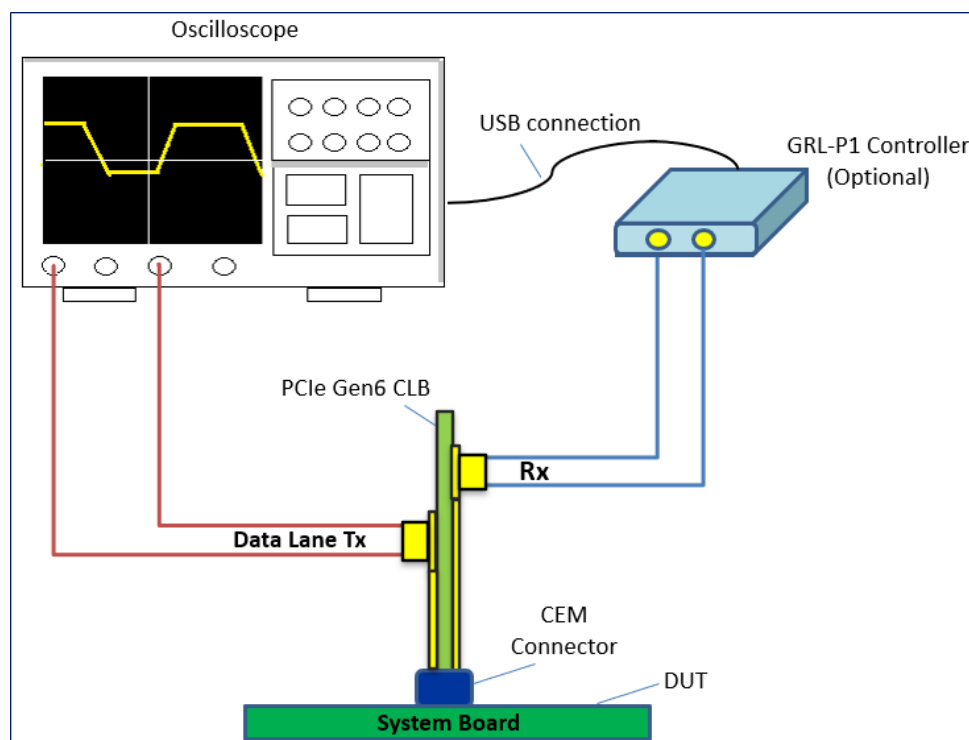


FIGURE 19. CONCEPTUAL PCIe GEN6 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITHOUT RF SWITCH)

1. Insert the CLB into the designated slot on the DUT.

2. Connect the Tx+ Data Lane from the CLB to Channel 1 of the Scope.
3. Connect the Tx- Data Lane from the CLB to Channel 3 of the Scope.
4. Connect the CLB Rx+ Lane to the GRL-P1 Output 1.
5. Connect the CLB Rx- Lane to the GRL-P1 Output 2.
6. Connect the power control adapter cable from the ATX power supply to the DUT.
7. Connect the GRL-P1's power control only cable to the input of the power control adapter cable.
8. Connect GRL-P1 to the Scope using a USB cable.

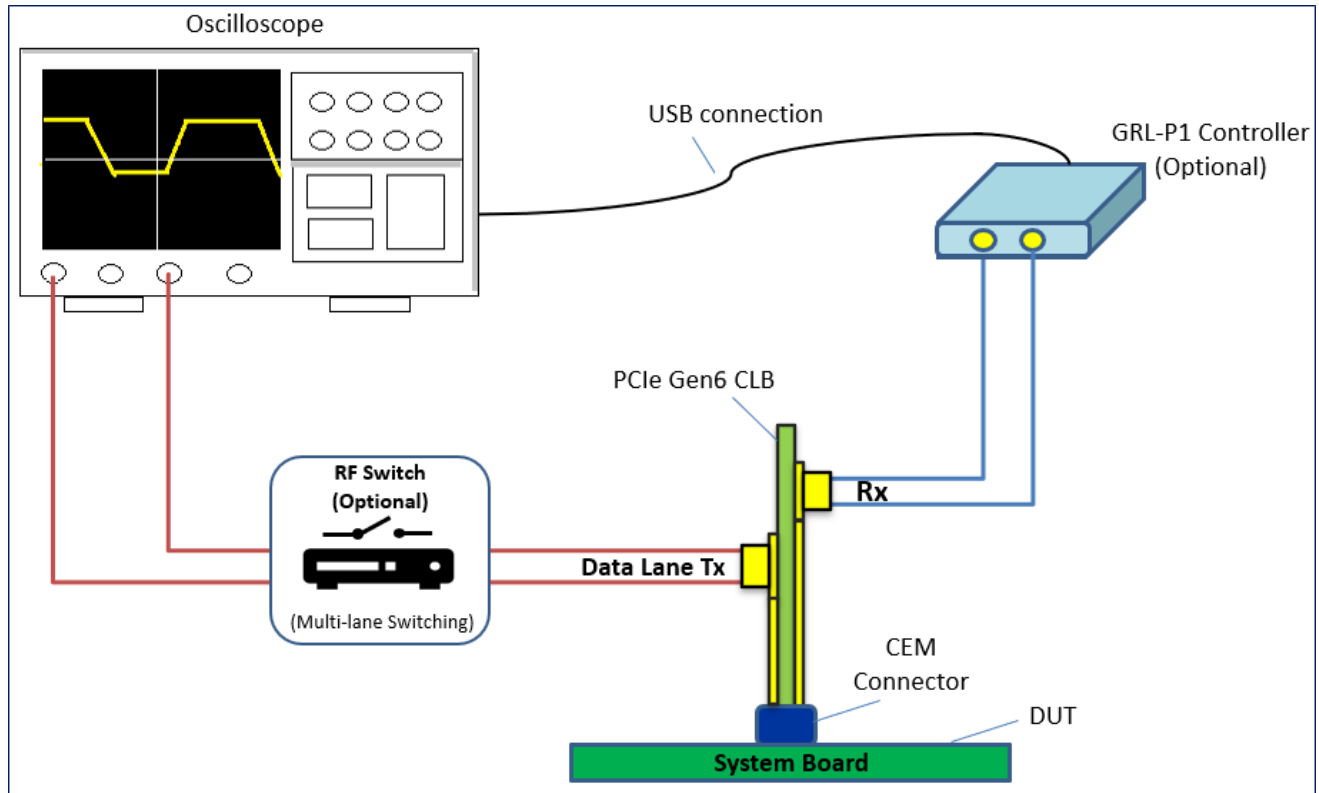


FIGURE 20. CONCEPTUAL PCIe GEN6 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH RF SWITCH)

Note the use of GRL-P1 and RF switch in the setup is optional.

1. Using the same connections from Figure 19, connect the Tx+ and Tx- Data Lanes from the CLB to the RF Switch Inputs.
2. Connect Output+ from the RF Switch to Channel 1 of the Scope.
3. Connect Output- from the RF Switch to Channel 3 of the Scope.
4. If using ISI, connect a 2.3 dB ISI in between the RF Switch outputs and Scope channels (Figure 21 below).

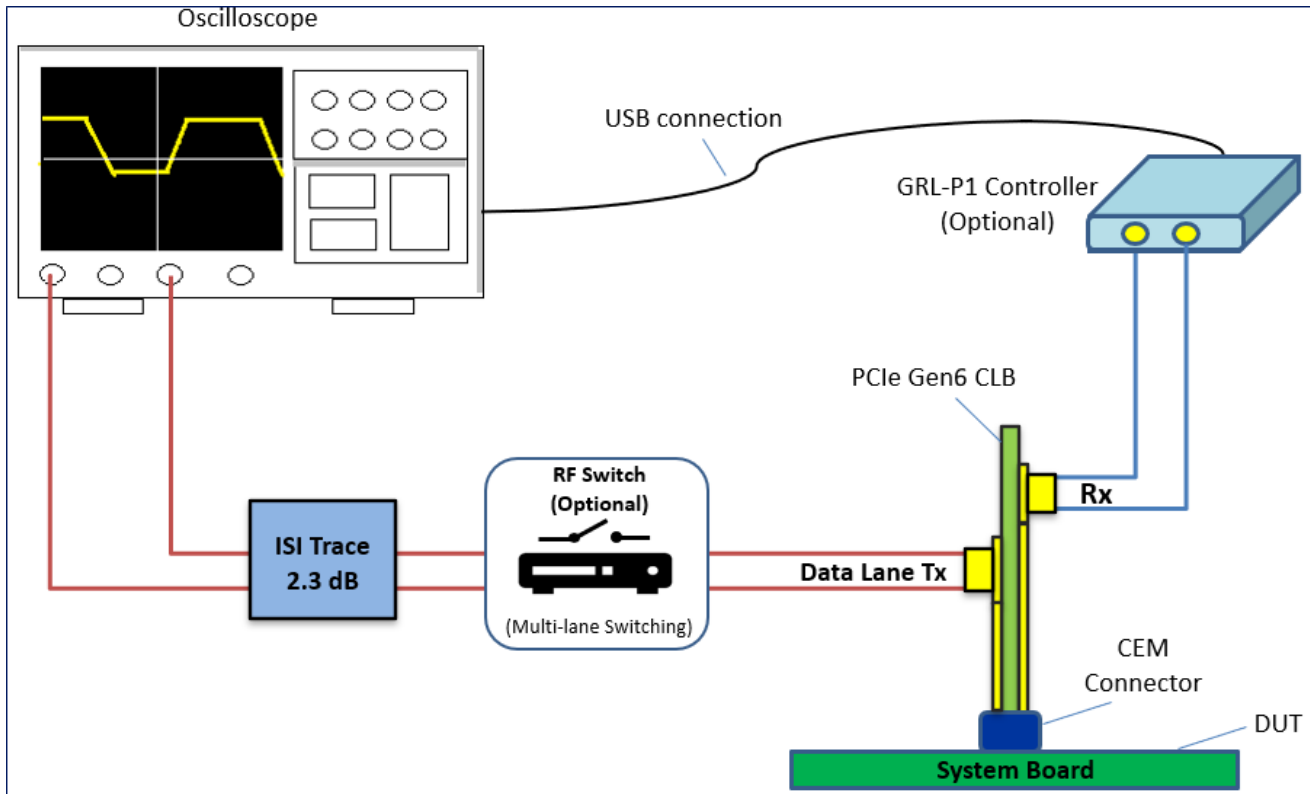


FIGURE 21. CONCEPTUAL PCIe GEN6 SYSTEM BOARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH RF SWITCH AND ISI)

4.2.1.2 Setup Using Manual Compliance Toggle

The following diagrams describe how to connect the equipment if not using any controller with a PCIe Compliance Load Board (CLB), a PCIe Gen3 U.2 (SFF-8639) CLB or a PCIe Gen3 M.2 CLB test fixture. *Note: With no controller connected, the compliance toggle must be initiated manually by pressing the compliance toggle button on the CLB.*

Note: For the PCIe Gen5 and Gen6 CLB, omit the Ref Clk connection in the setup.

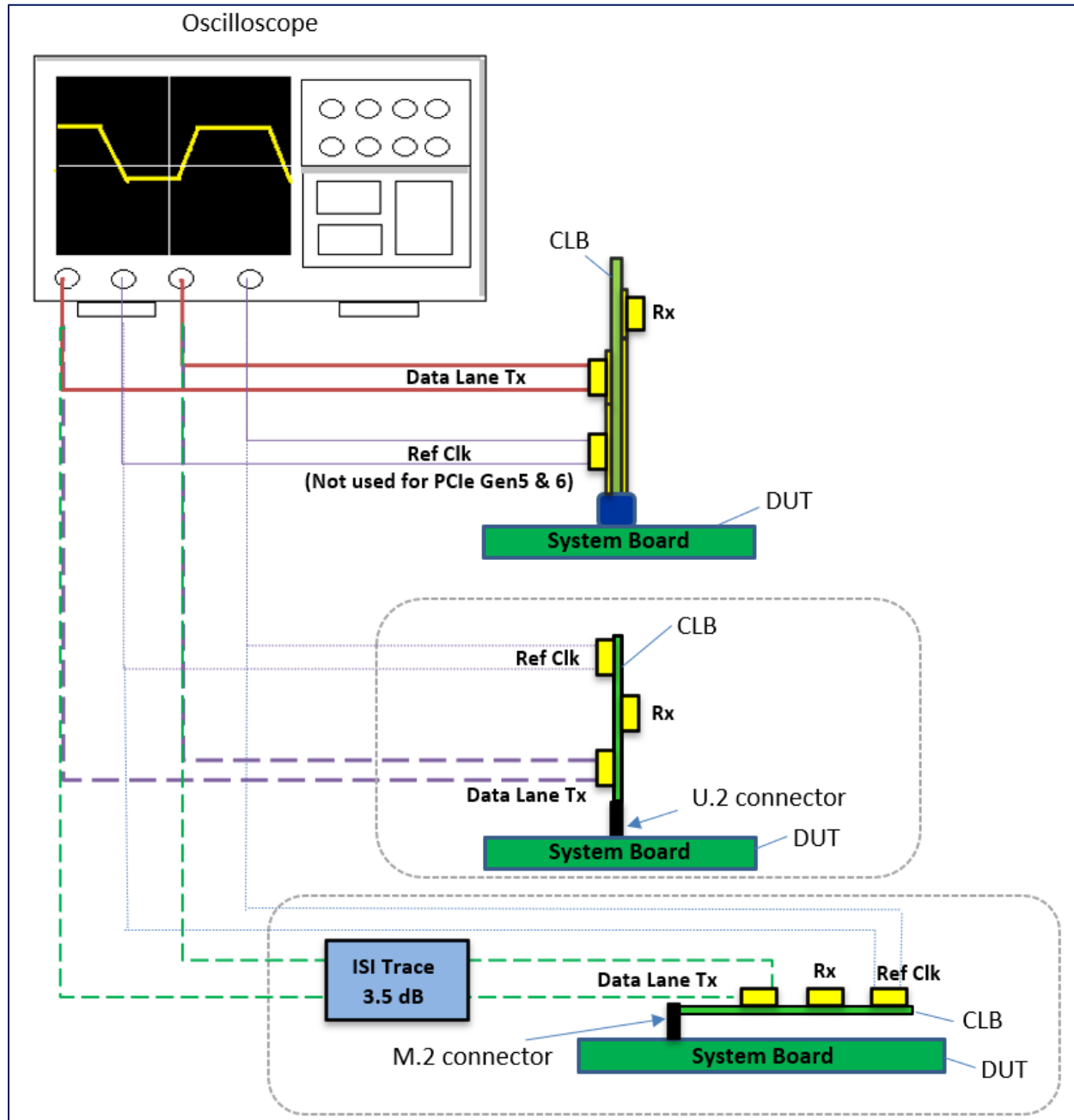


FIGURE 22. CONCEPTUAL PCIe SYSTEM BOARD TX TEST SETUP DIAGRAM USING MANUAL COMPLIANCE TOGGLE (WITHOUT RF SWITCH)

1. Insert the CLB into the designated slot on the DUT.
2. Connect the Tx+ Data Lane from the CLB to Channel 1 of the Scope.
3. Connect the Tx- Data Lane from the CLB to Channel 3 of the Scope.
4. If using the PCIe Gen3 M.2 CLB, connect a 3.5 dB ISI to the M.2 CLB Tx Data Lanes.
5. Connect Ref Clk+ from the CLB to Channel 2 of the Scope. *[Not applicable for PCIe Gen5 and Gen6]*
6. Connect Ref Clk- from the CLB to Channel 4 of the Scope. *[Not applicable for PCIe Gen5 and Gen6]*

7. Connect the power control adapter cable from the ATX power supply to the DUT.

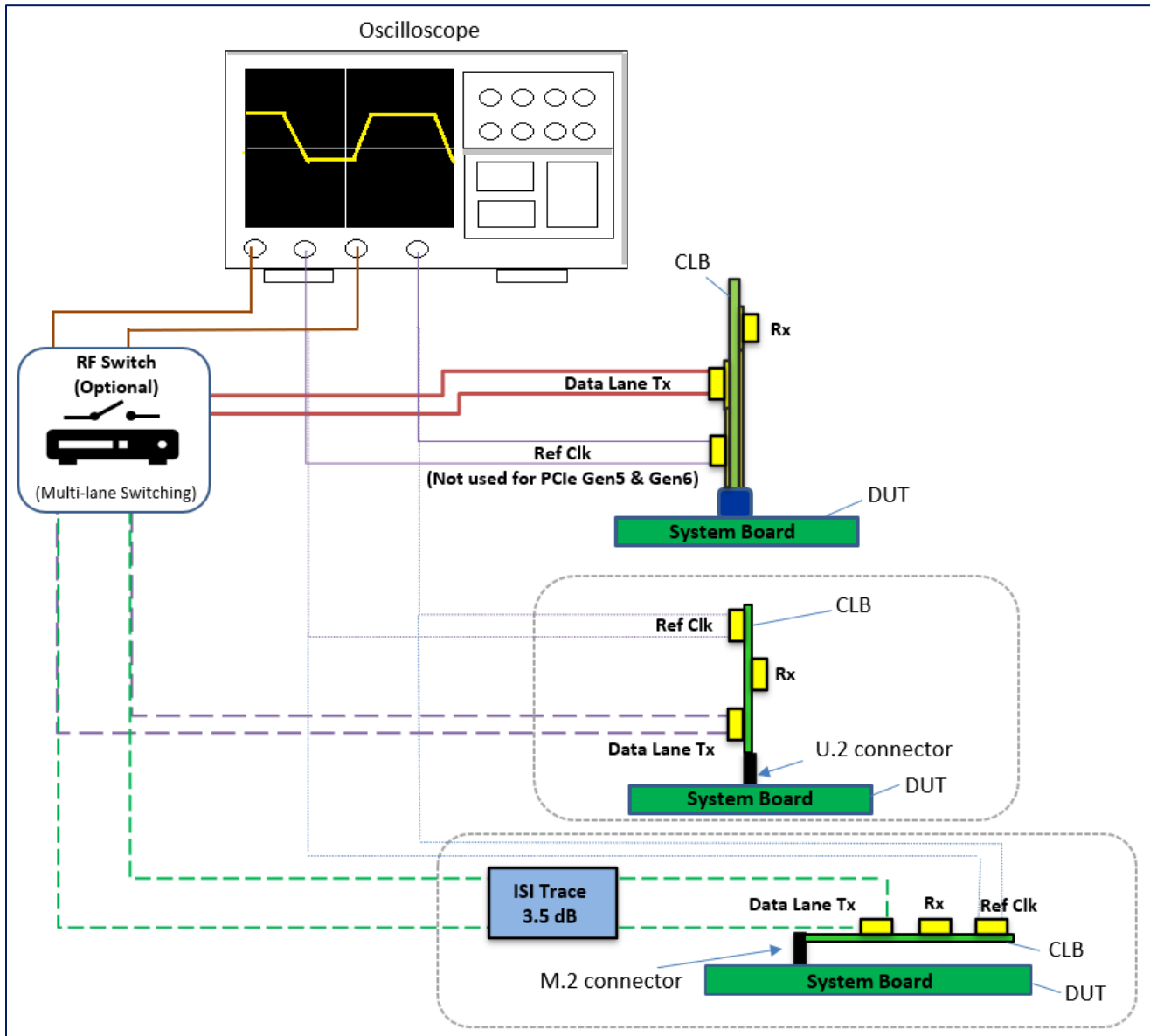


FIGURE 23. CONCEPTUAL PCIe SYSTEM BOARD TX TEST SETUP DIAGRAM USING MANUAL COMPLIANCE TOGGLE (WITH RF SWITCH)

Note the use of RF switch in the setup is optional.

1. Using the same connections from Figure 22, connect Tx+ and Tx- Data Lanes from the CLB to the RF Switch Inputs.
2. Connect Output+ from the RF Switch to Channel 1 of the Scope.
3. Connect Output- from the RF Switch to Channel 3 of the Scope.

4.2.2 Connect Equipment for Add-In Card DUT Test

The following connection diagrams show the recommended equipment setups to perform waveform acquisition and analysis for the PCIe Add-In Card DUT using a GRL Platform Solutions automation control enabled Scope and different test controller methods.

4.2.2.1 Setup Using GRL-P1 Hardware Controller with PCIe Test Fixtures

The following diagrams describe how to connect the equipment if using GRL-P1 with the PCIe Gen4, Gen5 and Gen6 Compliance Base Boards (CBB's). *Note the use of GRL-P1 in the setup is optional.*

4.2.2.1.1 PCIe Gen4 Add-In Card Connection Setup

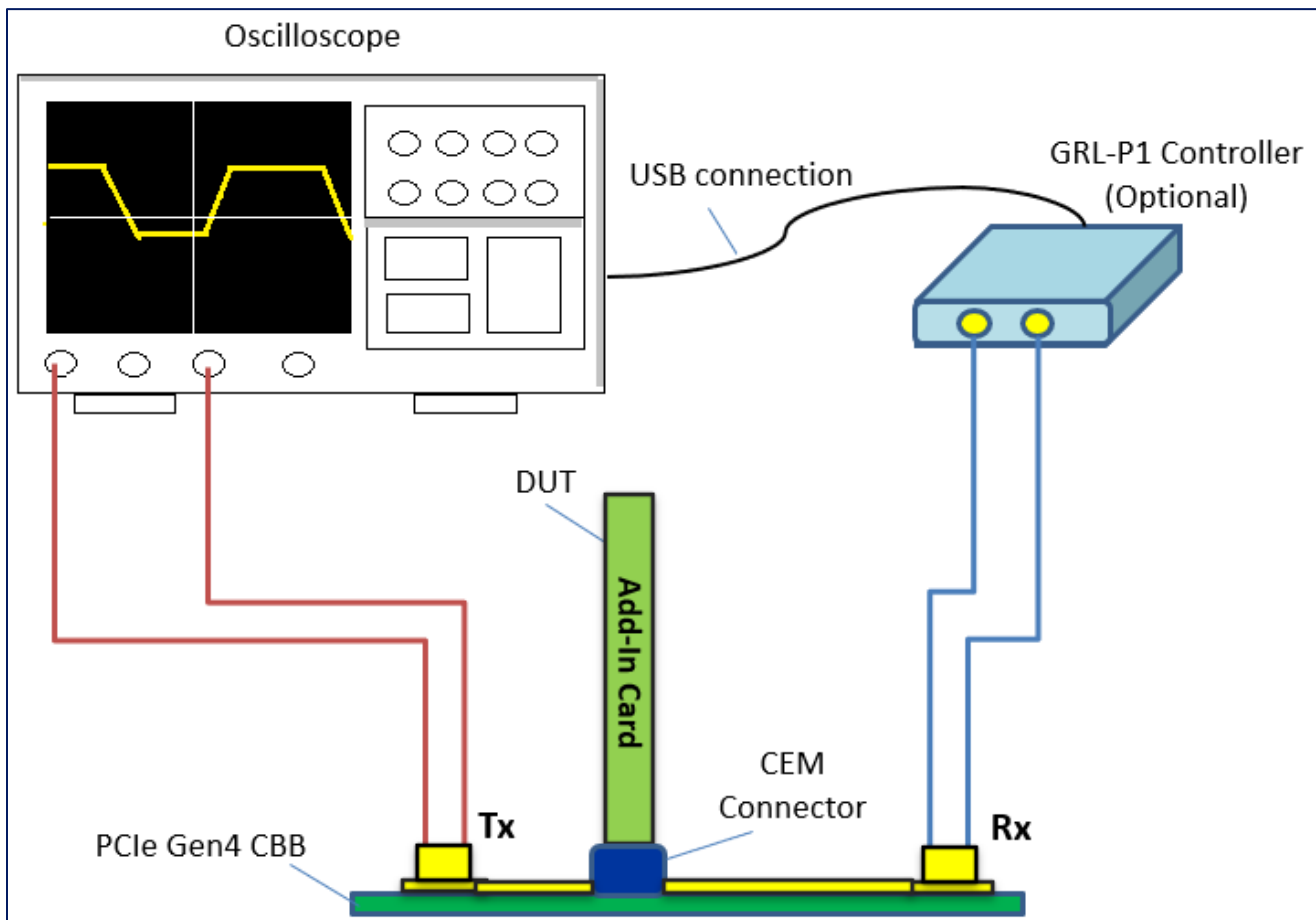


FIGURE 24. CONCEPTUAL PCIe GEN4 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITHOUT RF SWITCH)

1. Attach the DUT to the designated slot on the CBB.
2. Connect the Tx+ Data Lane from the CBB to Channel 1 of the Scope.
3. Connect the Tx- Data Lane from the CBB to Channel 3 of the Scope.
4. Connect the Rx+ Lane from the CBB to the GRL-P1 Output 1.
5. Connect the Rx- Lane from the CBB to the GRL-P1 Output 2.
6. Connect the power control adapter cable from the ATX power supply to the CBB.

7. Connect the GRL-P1's power control only cable to the input of the power control adapter cable.
8. Connect GRL-P1 to the Scope using a USB cable.

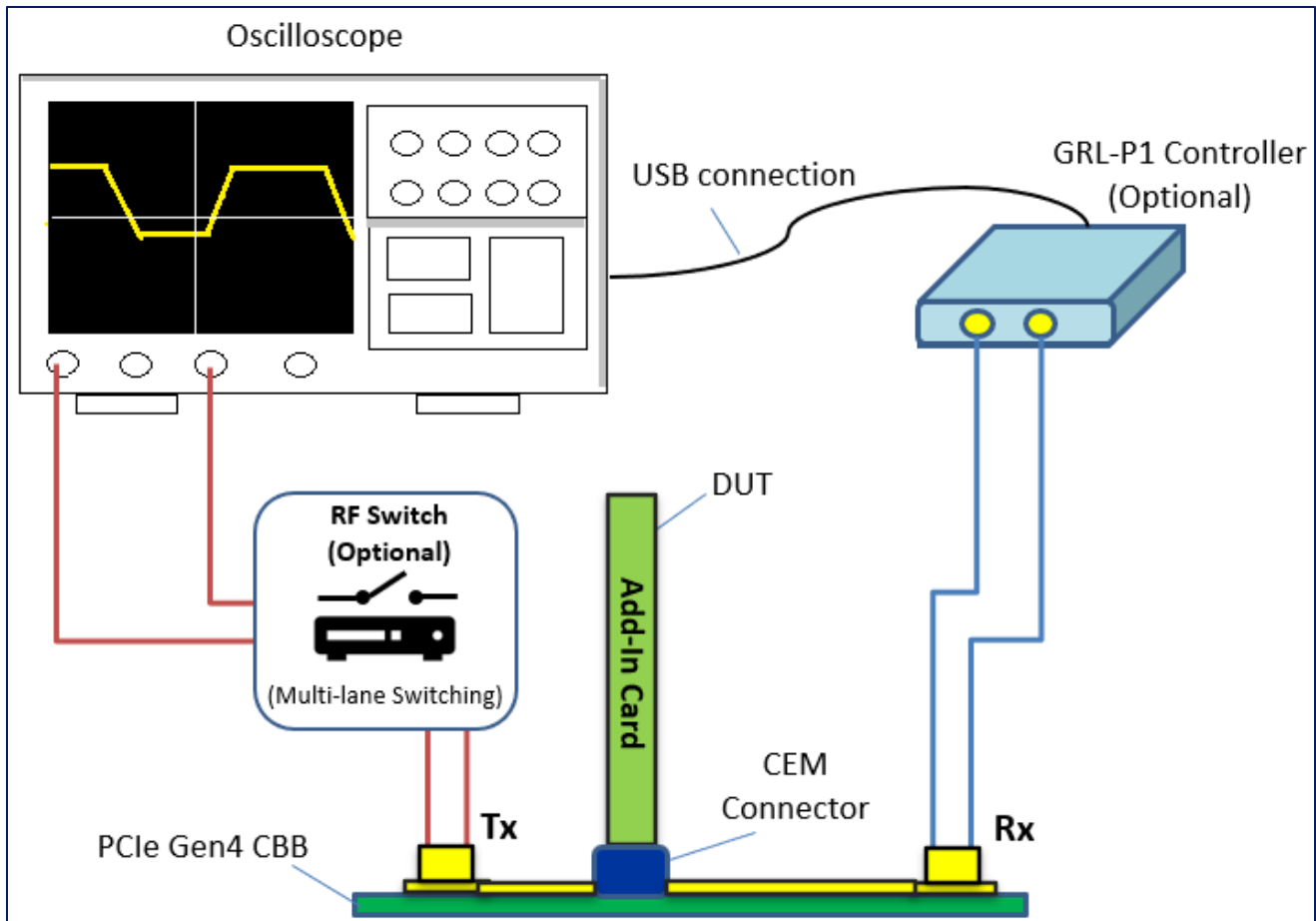


FIGURE 25. CONCEPTUAL PCIe GEN4 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH RF SWITCH)

Note: The use of GRL-P1 and RF switch in the setup is optional.

1. Using the same connections from Figure 24, connect the Tx+ and Tx- Data Lanes from the CBB to the RF Switch Inputs.
2. Connect Output+ from the RF Switch to Channel 1 of the Scope.
3. Connect Output- from the RF Switch to Channel 3 of the Scope.
4. If using ISI, connect a 10.3 dB ISI in between the RF Switch outputs and Scope channels (Figure 26 below).

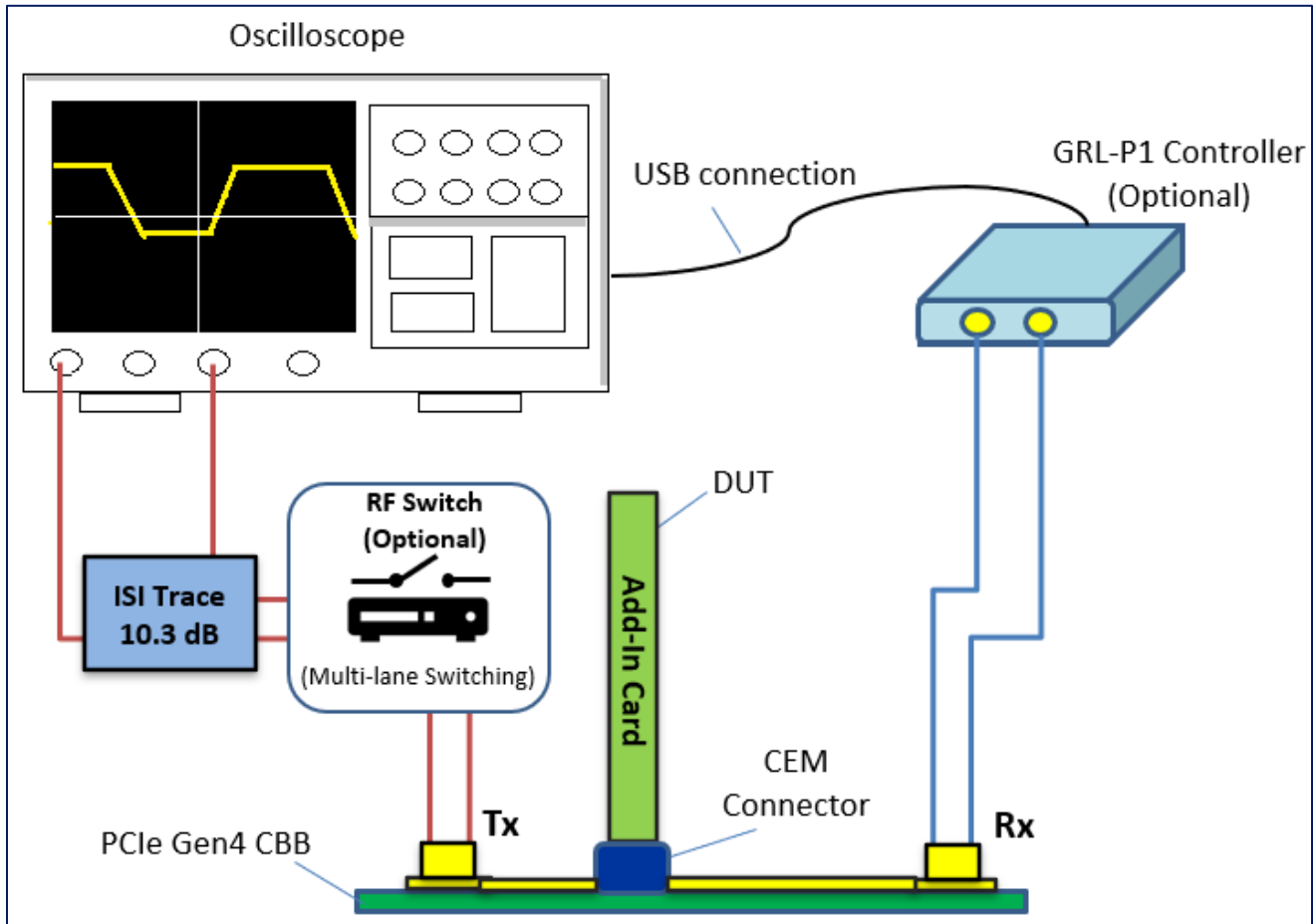


FIGURE 26. CONCEPTUAL PCIe GEN4 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH RF SWITCH AND ISI)

4.2.2.1.2 PCIe Gen5 Add-In Card Connection Setup

Note: The use of GRL-P1 in the setup is optional.

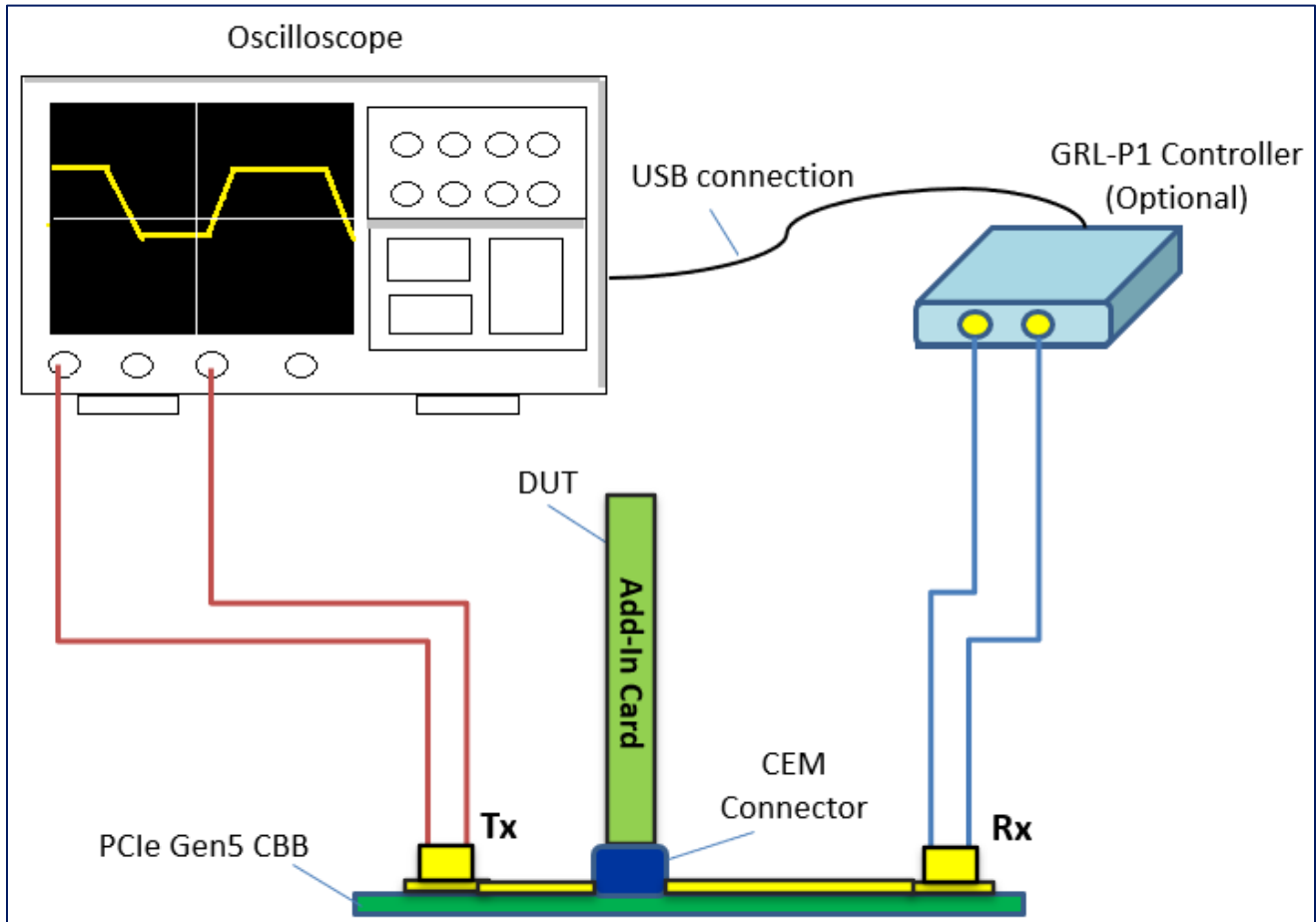


FIGURE 27. CONCEPTUAL PCIe GEN5 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITHOUT RF SWITCH)

1. Attach the DUT to the designated slot on the CBB.
2. Connect the Tx+ Data Lane from the CBB to Channel 1 of the Scope.
3. Connect the Tx- Data Lane from the CBB to Channel 3 of the Scope.
4. Connect the Rx+ Lane from the CBB to the GRL-P1 Output 1.
5. Connect the Rx- Lane from the CBB to the GRL-P1 Output 2.
6. Connect the power control adapter cable from the ATX power supply to the CBB.
7. Connect the GRL-P1's power control only cable to the input of the power control adapter cable.
8. Connect GRL-P1 to the Scope using a USB cable.

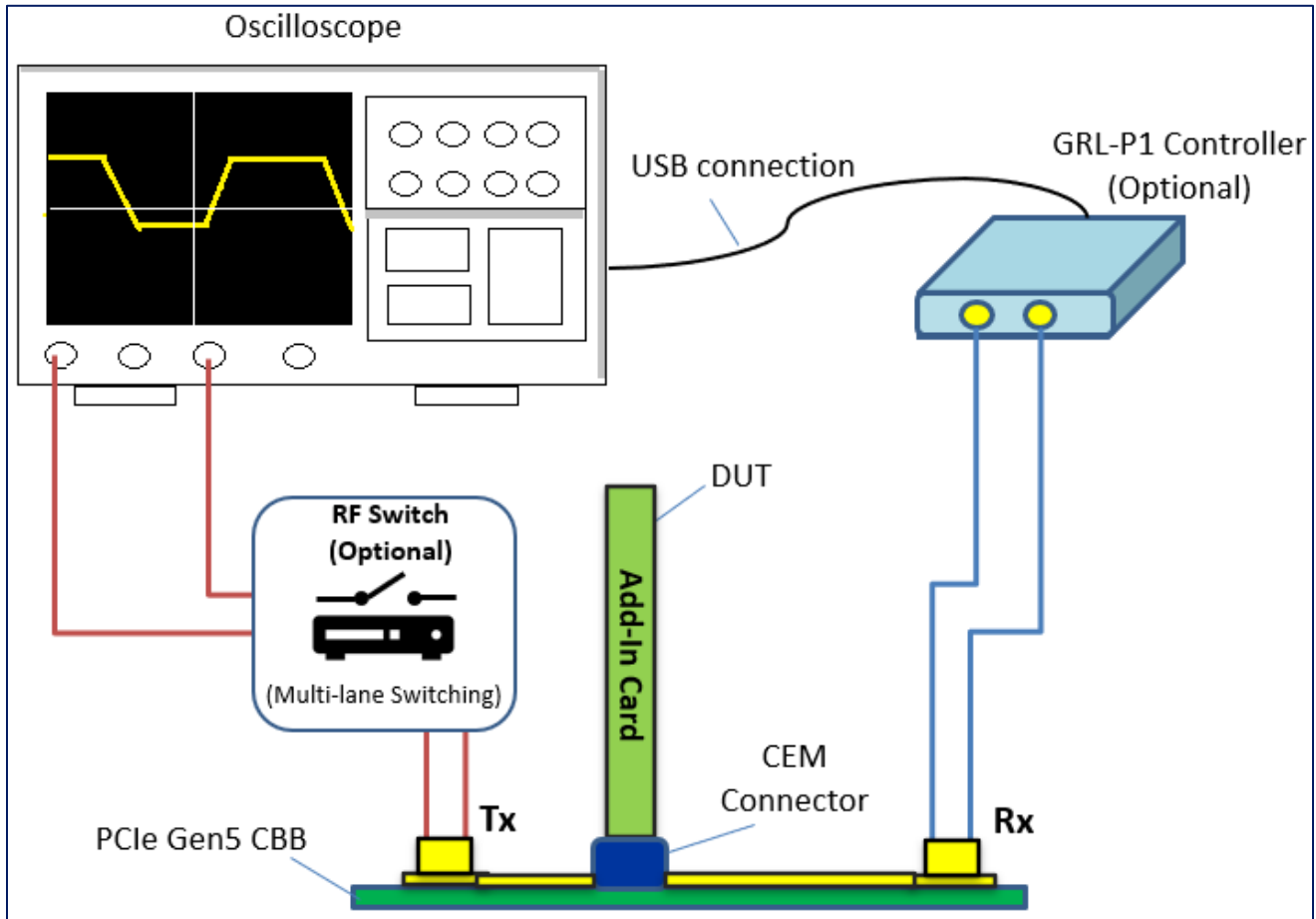


FIGURE 28. CONCEPTUAL PCIe GEN5 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH RF SWITCH)

Note: The use of GRL-P1 and RF switch in the setup is optional.

1. Using the same connections from Figure 27, connect the Tx+ and Tx- Data Lanes from the CBB to the RF Switch Inputs.
2. Connect Output+ from the RF Switch to Channel 1 of the Scope.
3. Connect Output- from the RF Switch to Channel 3 of the Scope.
4. If using ISI, connect a 12.5 dB ISI in between the RF Switch outputs and Scope channels (Figure 29 below).

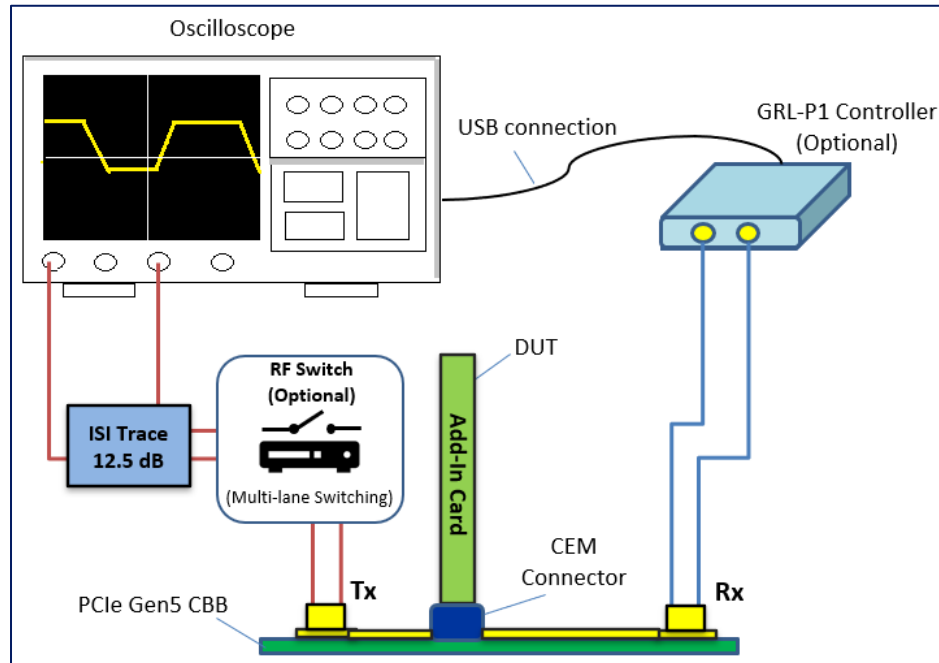


FIGURE 29. CONCEPTUAL PCIe GEN5 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH RF SWITCH AND ISI)

4.2.2.1.3 PCIe Gen6 Add-In Card Connection Setup

Note: The use of GRL-P1 in the setup is optional.

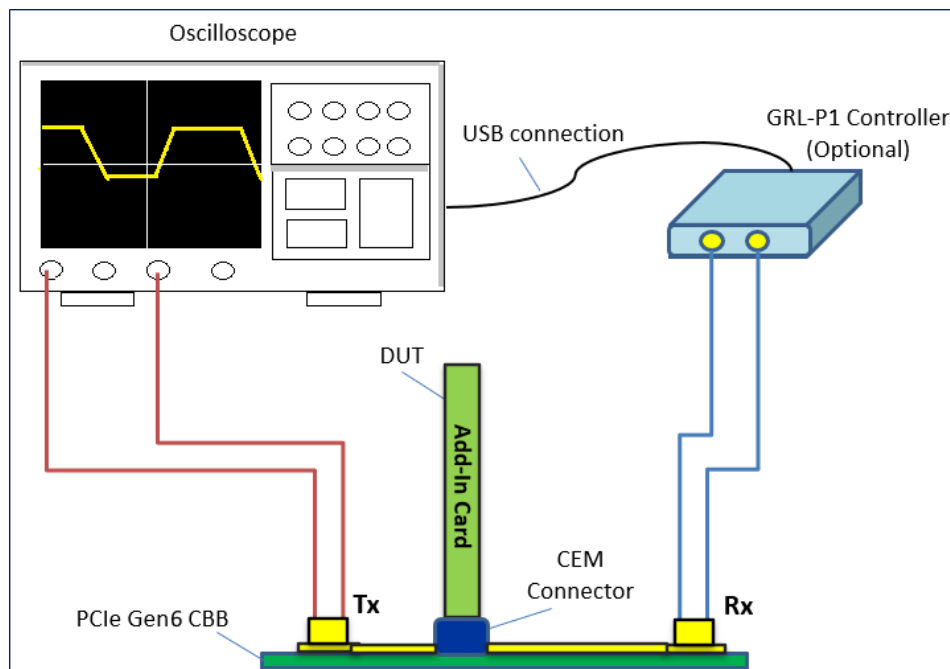


FIGURE 30. CONCEPTUAL PCIe GEN6 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITHOUT RF SWITCH)

1. Attach the DUT to the designated slot on the CBB.
2. Connect the Tx+ Data Lane from the CBB to Channel 1 of the Scope.

3. Connect the Tx- Data Lane from the CBB to Channel 3 of the Scope.
4. Connect the Rx+ Lane from the CBB to the GRL-P1 Output 1.
5. Connect the Rx- Lane from the CBB to the GRL-P1 Output 2.
6. Connect the power control adapter cable from the ATX power supply to the CBB.
7. Connect the GRL-P1's power control only cable to the input of the power control adapter cable.
8. Connect GRL-P1 to the Scope using a USB cable.

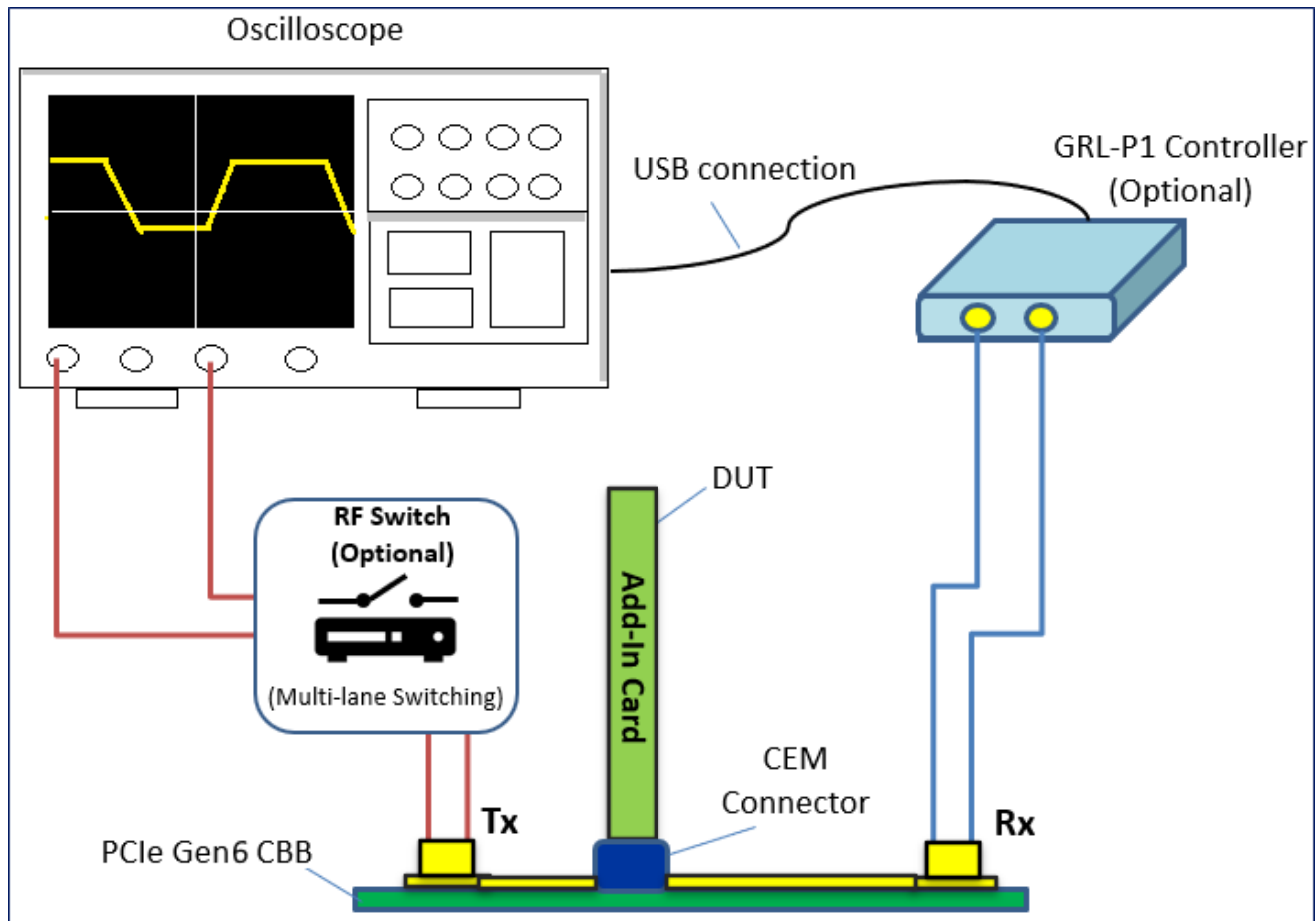


FIGURE 31. CONCEPTUAL PCIe GEN6 ADD-IN CARD Tx TEST SETUP DIAGRAM USING GRL-P1 (WITH RF SWITCH)

Note: The use of GRL-P1 and RF switch in the setup is optional.

1. Using the same connections from Figure 30, connect the Tx+ and Tx- Data Lanes from the CBB to the RF Switch Inputs.
2. Connect Output+ from the RF Switch to Channel 1 of the Scope.
3. Connect Output- from the RF Switch to Channel 3 of the Scope.
4. If using ISI, connect a 12.5 dB ISI in between the RF Switch outputs and Scope channels (Figure 32 below).

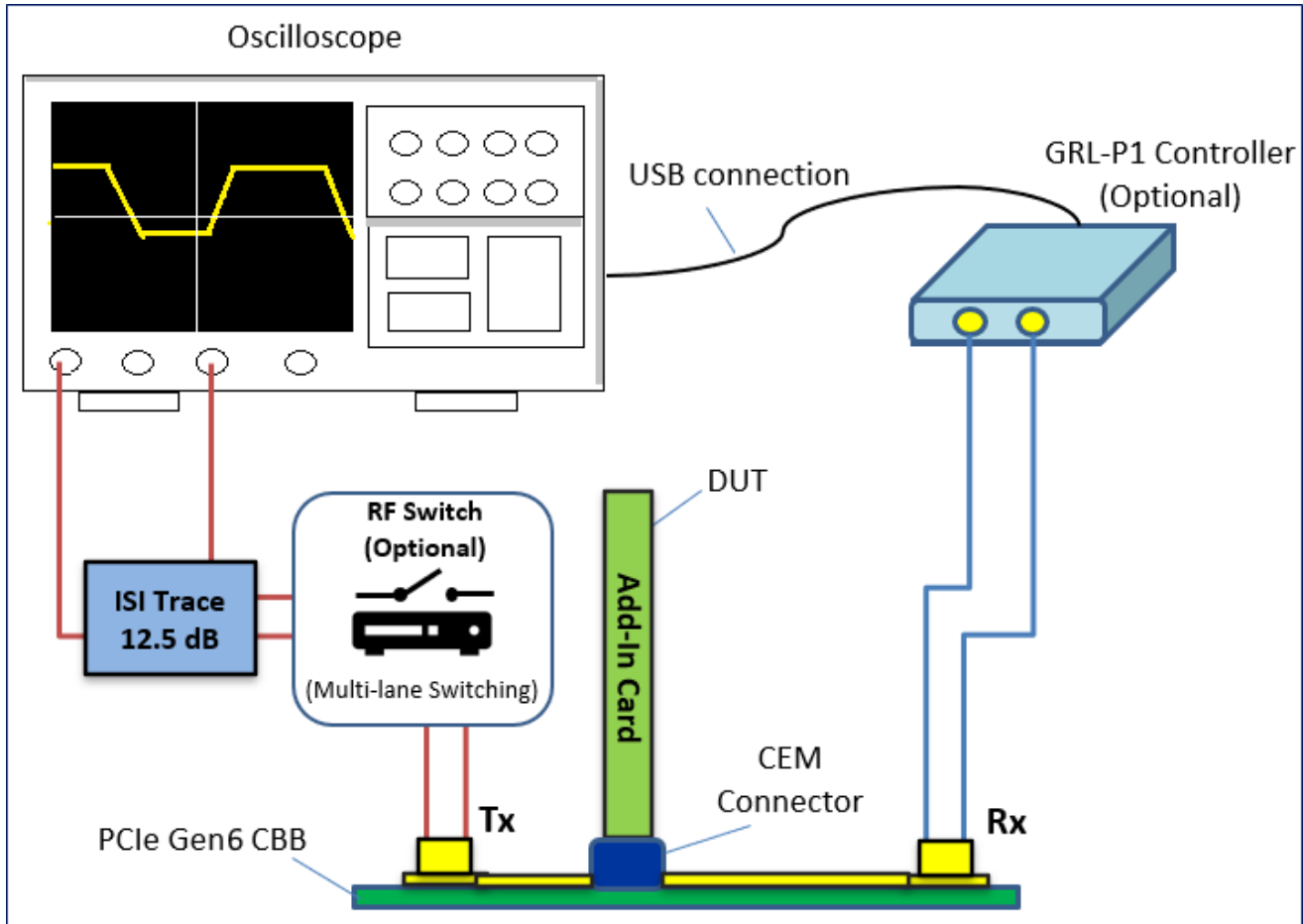


FIGURE 32. CONCEPTUAL PCIe GEN6 ADD-IN CARD TX TEST SETUP DIAGRAM USING GRL-P1 (WITH RF SWITCH AND ISI)

4.2.2.2 Setup Using Manual Compliance Toggle

The following diagrams describe how to connect the equipment if not using any controller with a PCIe Compliance Base Board (CBB), a PCIe Gen3 U.2 (SFF-8639) CBB or a PCIe Gen3 M.2 CBB test fixture. *Note: With no controller connected, the compliance toggle must be initiated manually by pressing the compliance toggle button on the CBB.*

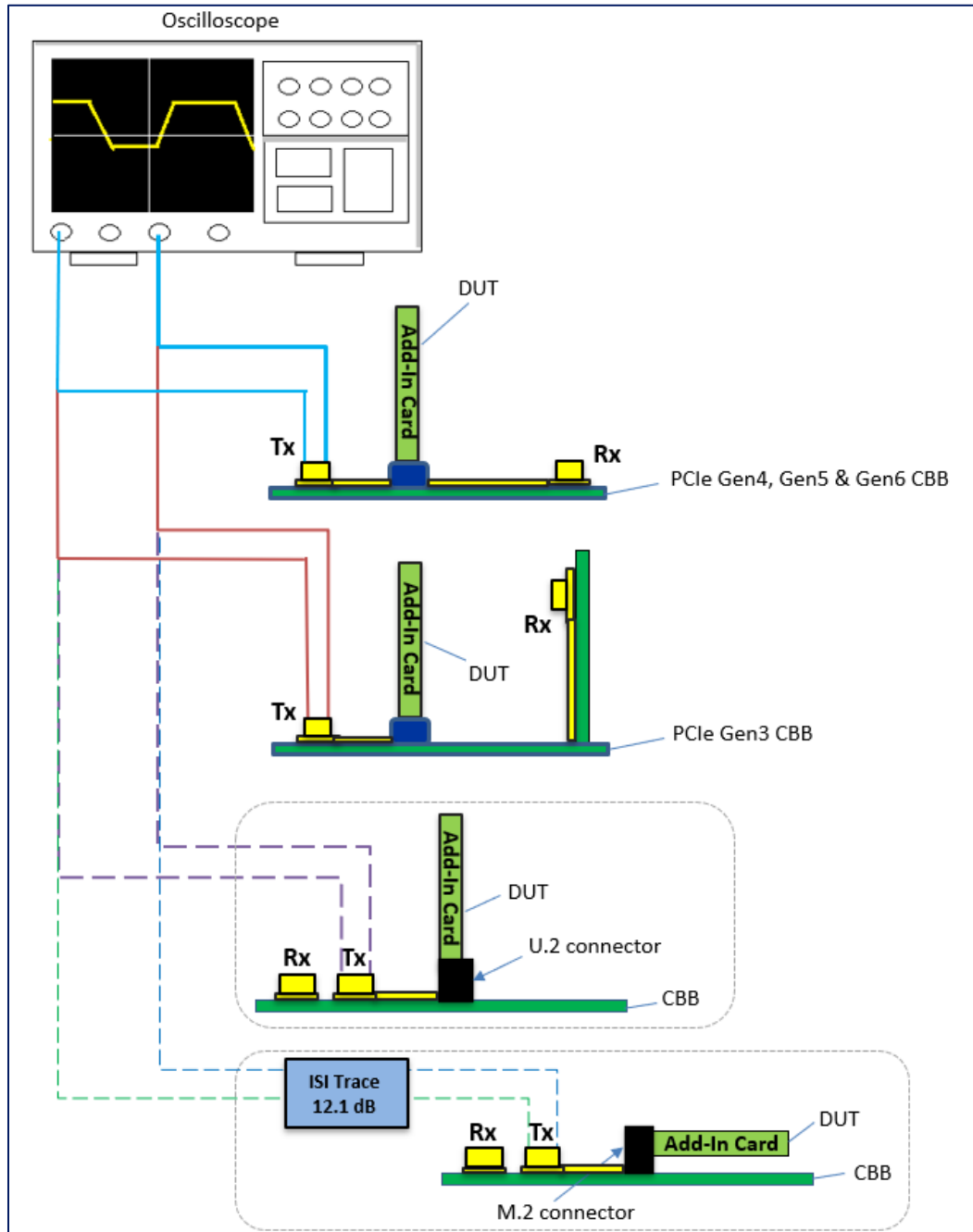


FIGURE 33. CONCEPTUAL PCIe ADD-IN CARD TX TEST SETUP DIAGRAM USING MANUAL COMPLIANCE TOGGLE (WITHOUT RF SWITCH)

1. Attach the DUT to the designated slot on the CBB.
2. Connect the Tx+ Data Lane from the CBB to Channel 1 of the Scope.
3. Connect the Tx- Data Lane from the CBB to Channel 3 of the Scope.
4. If using the PCIe M.2 CBB, connect a 12.1 dB ISI to the M.2 CBB Tx Data Lanes.
5. Connect the power control adapter cable from the ATX power supply to the CBB.

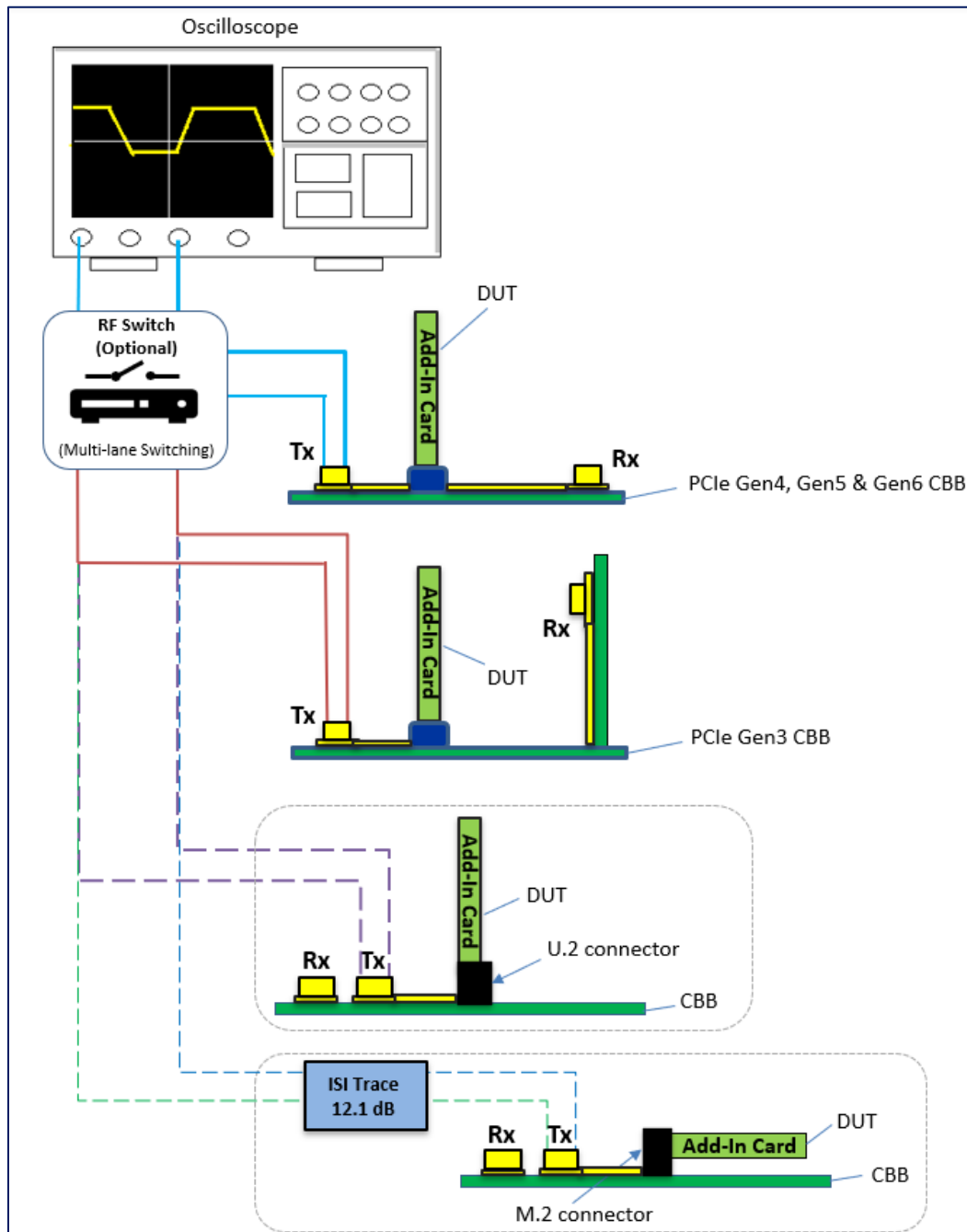


FIGURE 34. CONCEPTUAL PCIe ADD-IN CARD TX TEST SETUP DIAGRAM USING MANUAL COMPLIANCE TOGGLE (WITH RF SWITCH)

Note: The use of RF switch in the setup is optional.

1. Using the same connections from Figure 33, connect the Tx+ and Tx- Data Lanes from the CBB to the RF Switch Inputs.
2. Connect Output+ from the RF Switch to Channel 1 of the Scope.
3. Connect Output- from the RF Switch to Channel 3 of the Scope.

4.2.3 Connect Equipment for System Ref Clock Jitter Test

The following connection diagram shows the recommended equipment setup to perform waveform acquisition and analysis for the PCIe Gen6 System Ref Clock Jitter Test.

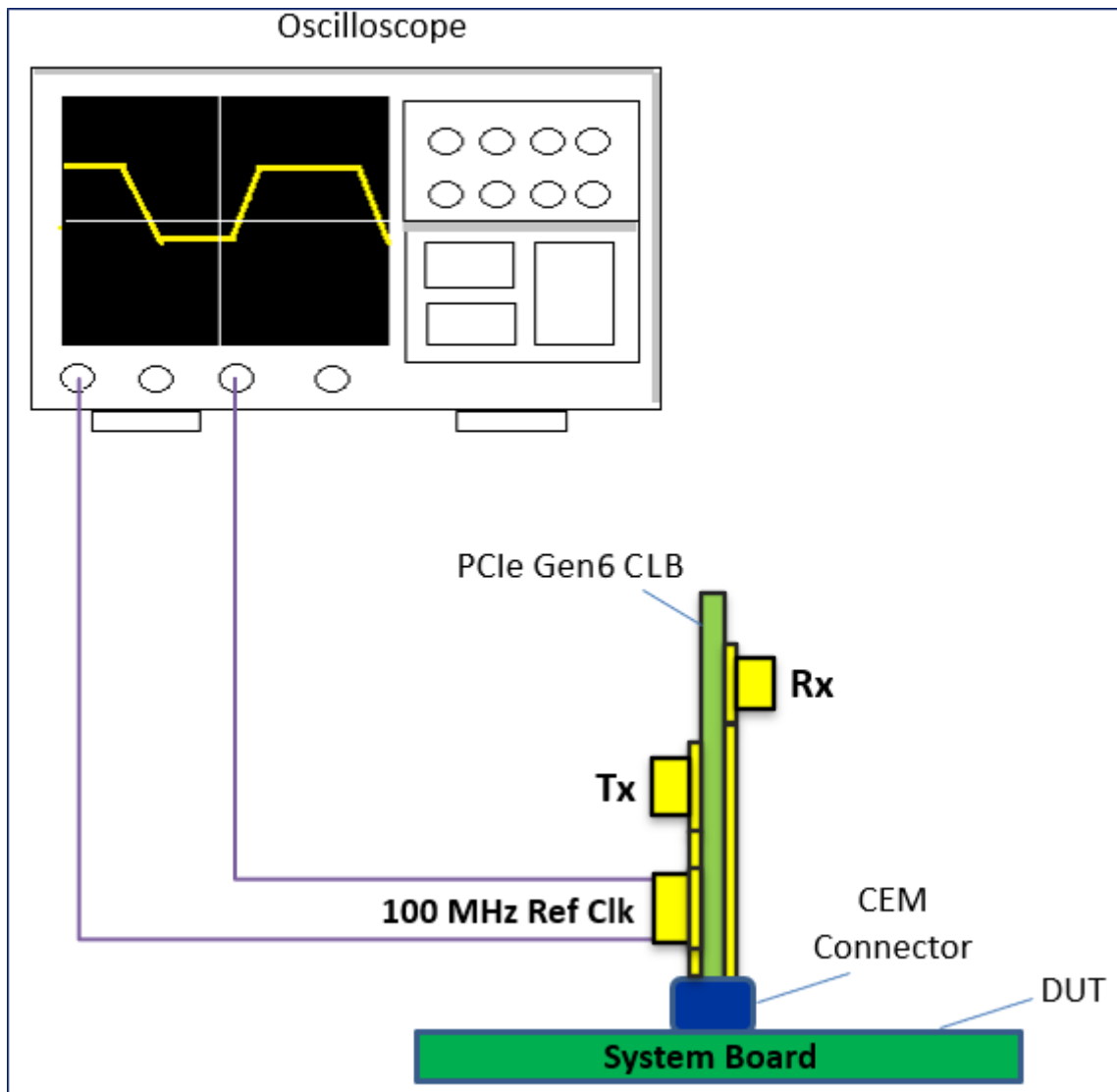


FIGURE 35. CONCEPTUAL PCIe GEN6 SYSTEM REF CLOCK JITTER TEST SETUP DIAGRAM

1. Insert the CLB into the designated slot on the DUT.
2. Connect Ref Clk+ from the CLB to Channel 1 of the Scope.
3. Connect Ref Clk- from the CLB to Channel 3 of the Scope.
4. Connect the power control adapter cable from the ATX power supply to the DUT.

4.2.4 Connection Setup for Scope Intrinsic Noise Measurement (For PCIe Gen6)

Figure 36 below shows the setup diagram to measure the intrinsic noise generated by the oscilloscope with no external signal applied for PCIe Gen6. The intrinsic noise waveforms will be captured and saved for SigTest processing in subsequent steps.

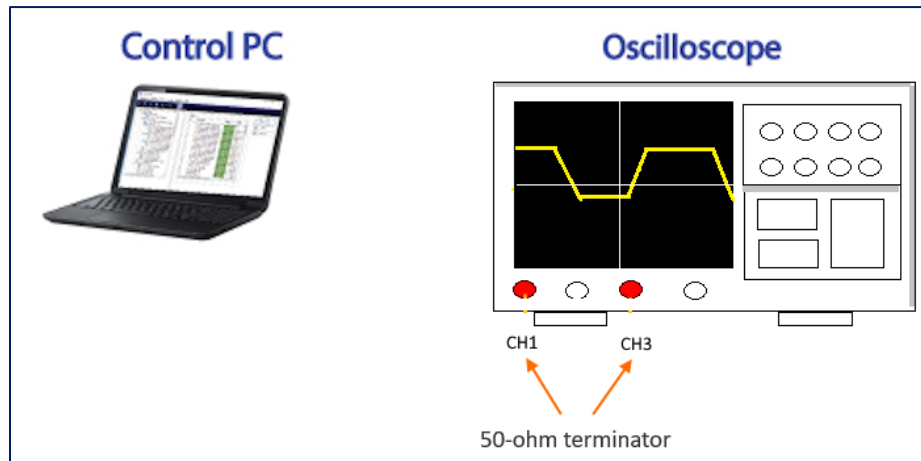


FIGURE 36. SETUP FOR SCOPE INTRINSIC NOISE MEASUREMENT (FOR PCIe GEN6)

Connection Step:

Connect 50-ohm terminators to the oscilloscope channels 1 and 3.

4.2.5 Set Up Test Requirements

After setting up the physical equipment, select  from the GRL-PXE-TX Test Application menu to access the Setup Configuration page. Select the DUT to be tested, set up and run SigTest/Seasim, and set up waveform processing to be applied for testing.

- Device Type** tab: Select to use either a PCIe System Board or Add-In Card as the DUT. Select to use either the standard PCIe CEM, PCIe Gen3 U.2 (SFF-8639) or PCIe Gen3 M.2 fixture connector as supported by the DUT.

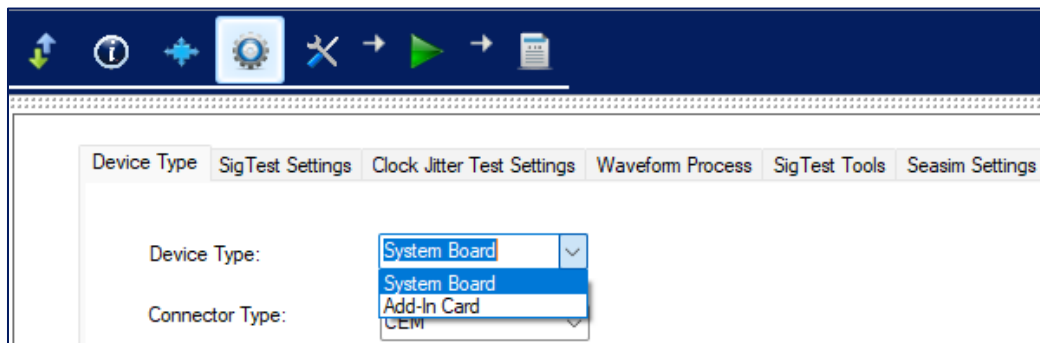


FIGURE 37. SELECT DUT TYPE

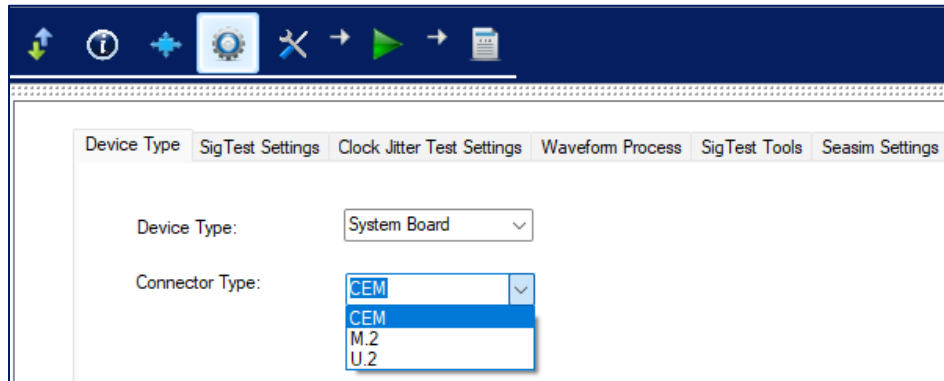


FIGURE 38. SELECT DUT FIXTURE CONNECTOR TYPE

b) **SigTest Settings** tab:

- *PCIe Gen1 (2.5Gb/s), Gen2 (5Gb/s) and Gen3 (8Gb/s)* – Select to run either the pre-defined Version “3.2.0.3” or a “Custom” Version of the SigTest. If “Custom” is selected, enter the Version number of the Custom SigTest and also make sure that the SigTest is already installed in the system.
- *PCIe Gen4 (16Gb/s)* – Enter the SigTest Version for running Signal Quality (SQ) or Preset Tests and also make sure that the SigTest is already installed in the system.
- *PCIe Gen5 (32Gb/s)* – Enter the SigTest Version for running Signal Quality (SQ) or Preset Tests and also make sure that the SigTest is already installed in the system.
- *PCIe Gen6 (64Gb/s)* – Enter the SigTest Version for running Signal Quality (SQ) or Preset Tests and also make sure that the SigTest is already installed in the system.

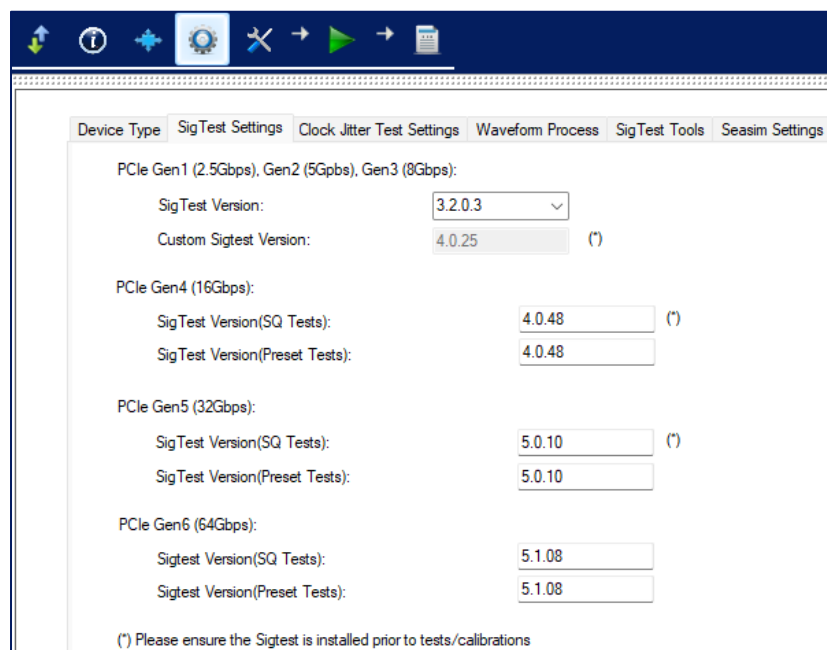


FIGURE 39. SET UP SIGTEST

- c) **Clock Jitter Test Settings** tab: Enter the version of the Clock Jitter Tool for PCIe Gen4/ Gen5/Gen6, and select the type and file directory of the template to be used for the System Ref Clock Jitter Test.

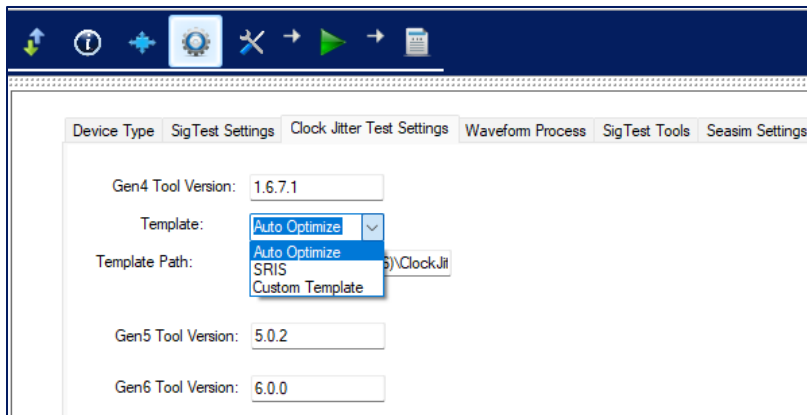


FIGURE 40. CONFIGURE SETTINGS FOR SYSTEM REF CLOCK JITTER TEST

- d) **Waveform Process** tab: Select “Live Capture” to acquire PCIe waveforms by the GRL Platform Solutions software, or select “Process Pre-captured waveforms” to use existing waveforms that have been previously captured and saved for analysis. *Note that selecting “Process Pre-captured waveforms” will remove the “Waveform Acquisition” group from the Select Tests page. See Section 4.2.6.1.*

If “Process Pre-captured waveforms” is selected, enter the directory of the saved waveform file in the Pre-Captured Waveform Path field.

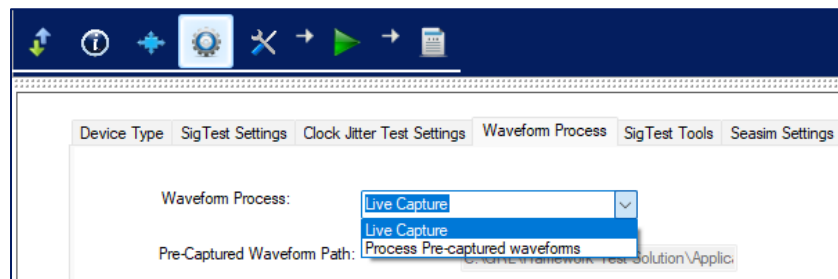


FIGURE 41. SET UP WAVEFORM PROCESSING

- e) **Seasim Settings** tab: Select the Seasim software version as supported for PCIe Gen6 to validate the stressed eye of the Tx signal.

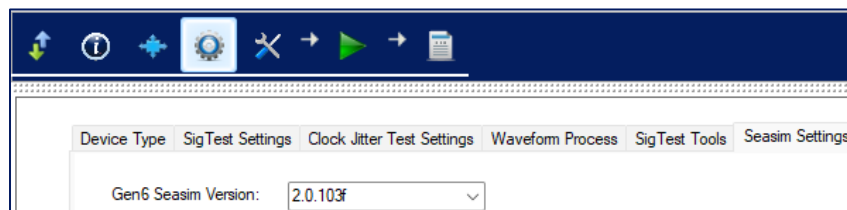


FIGURE 42. SELECT SEASIM VERSION FOR PCIe GEN6

4.2.6 Select Compliance Tests

Once test requirements are defined, select **Test List** from the top “Windows” drop-down menu to display and access all tests available for the selected DUT type. User can select any of these tests to perform DUT compliance testing for all PCIe parameters.

Note: The Select Tests page will only list DUT-specific tests. For example, if System Board is selected as the DUT, only those tests applicable for System Board will be shown. Other test parameters such as desired data rates and presets that were previously configured may also affect the test selection.

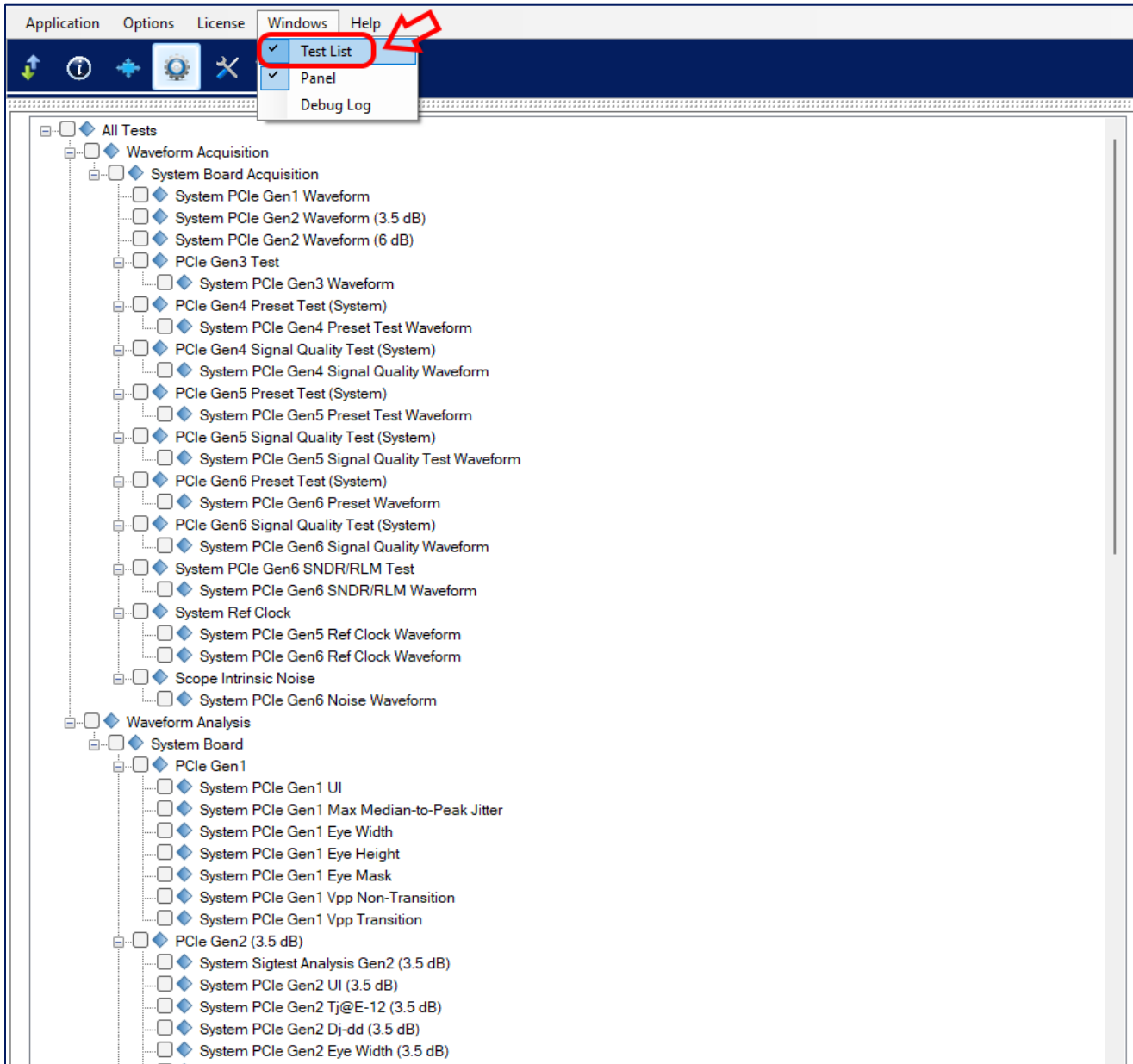


FIGURE 43. SELECT TESTS PAGE

4.2.6.1 Select to Acquire Waveforms and Measure PCIe Gen6 Scope Intrinsic Noise

Under “Waveform Acquisition”, select the waveforms to capture for the required PCIe data rates. The software will run a live capture of the selected waveforms prior to analysis.

Also for PCIe Gen6, select “Scope Intrinsic Noise” to capture and save the intrinsic noise waveforms for SigTest processing.

Note: Waveform Acquisition can only be selected if “Live Capture” is set under the Waveform Process tab on the Setup Configuration page. See Section 4.2.4.

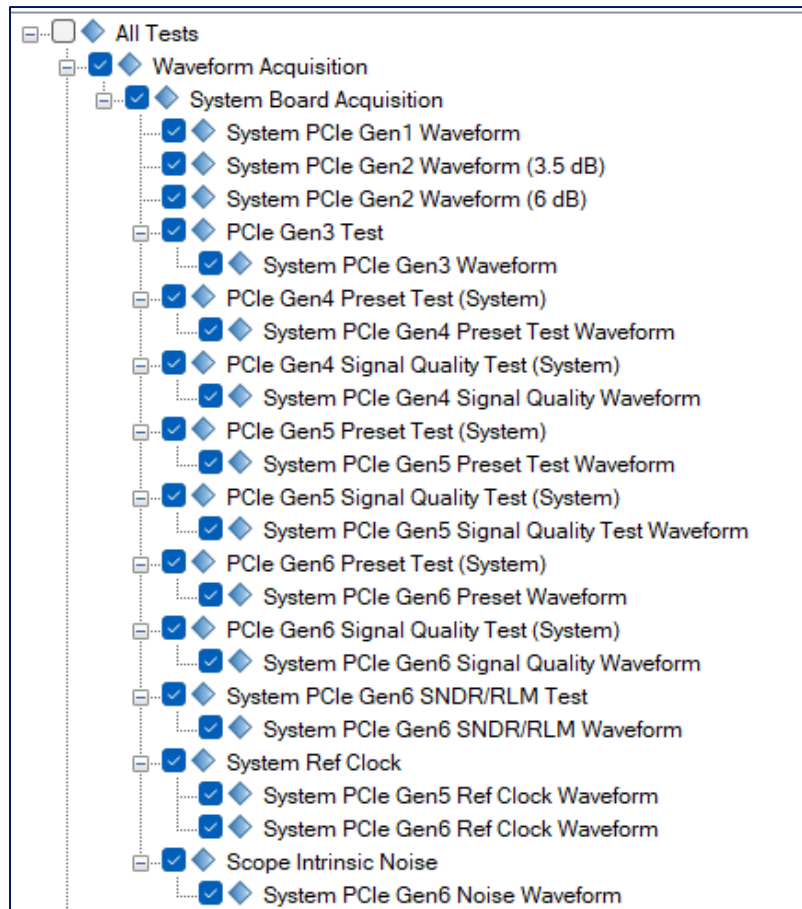


FIGURE 44. SELECT WAVEFORM TO CAPTURE AND PCIe GEN6 SCOPE INTRINSIC NOISE MEASUREMENT

4.2.6.2 Select Waveform Analysis Tests

Under “Waveform Analysis”, select to perform the SigTest analysis (or Seasim for PCIe Gen6), jitter and eye measurements, and preset test for the applicable PCIe waveform. The software will automatically run the selected tests when initiated.

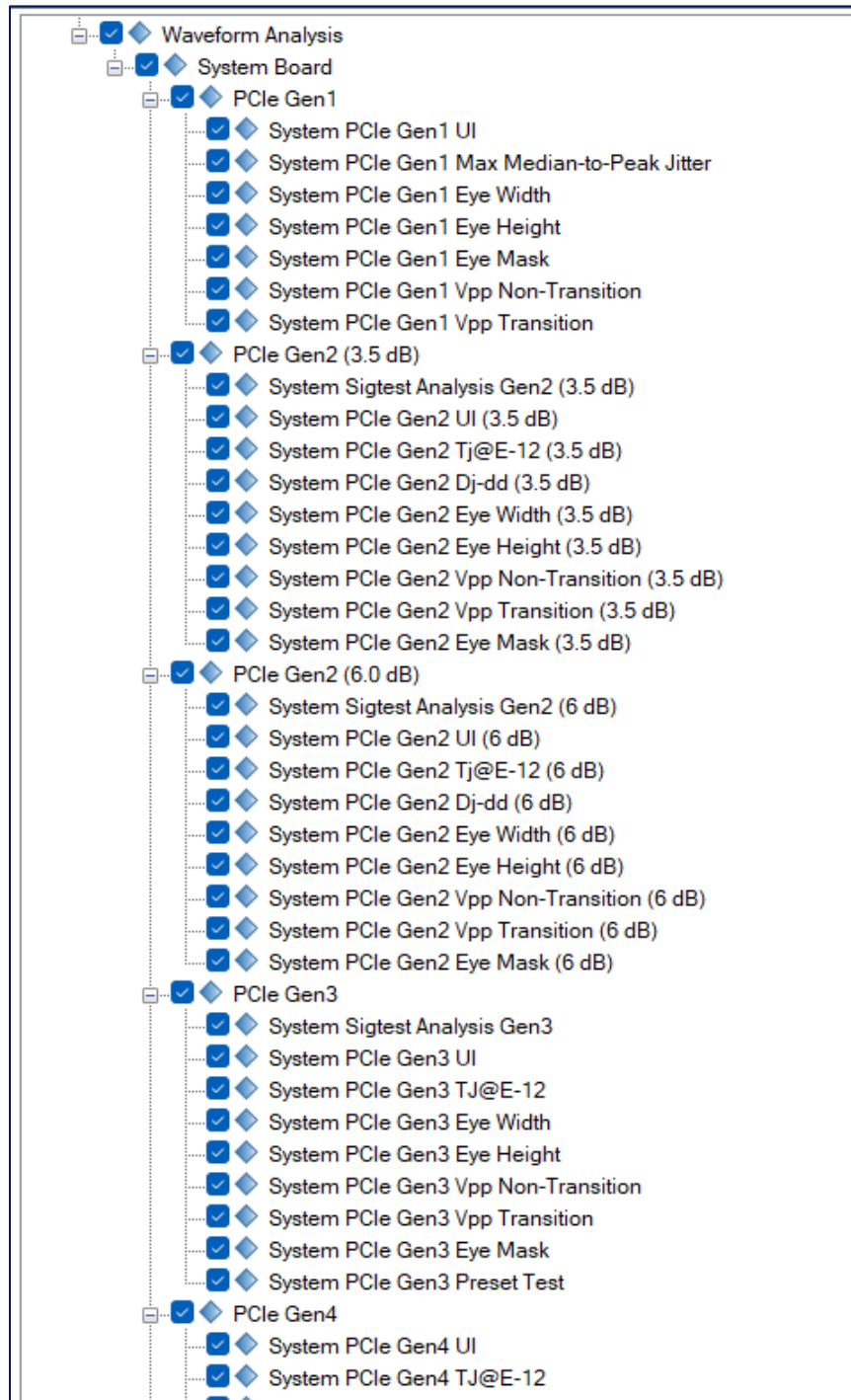


FIGURE 45. SELECT WAVEFORM ANALYSIS TESTS

4.2.7 Configure Test Parameters

After selecting the desired tests, select  from the menu to access the Configurations page. Set the required parameters for testing as described below.

To return all parameters to their default values, select the 'Set Default' button.

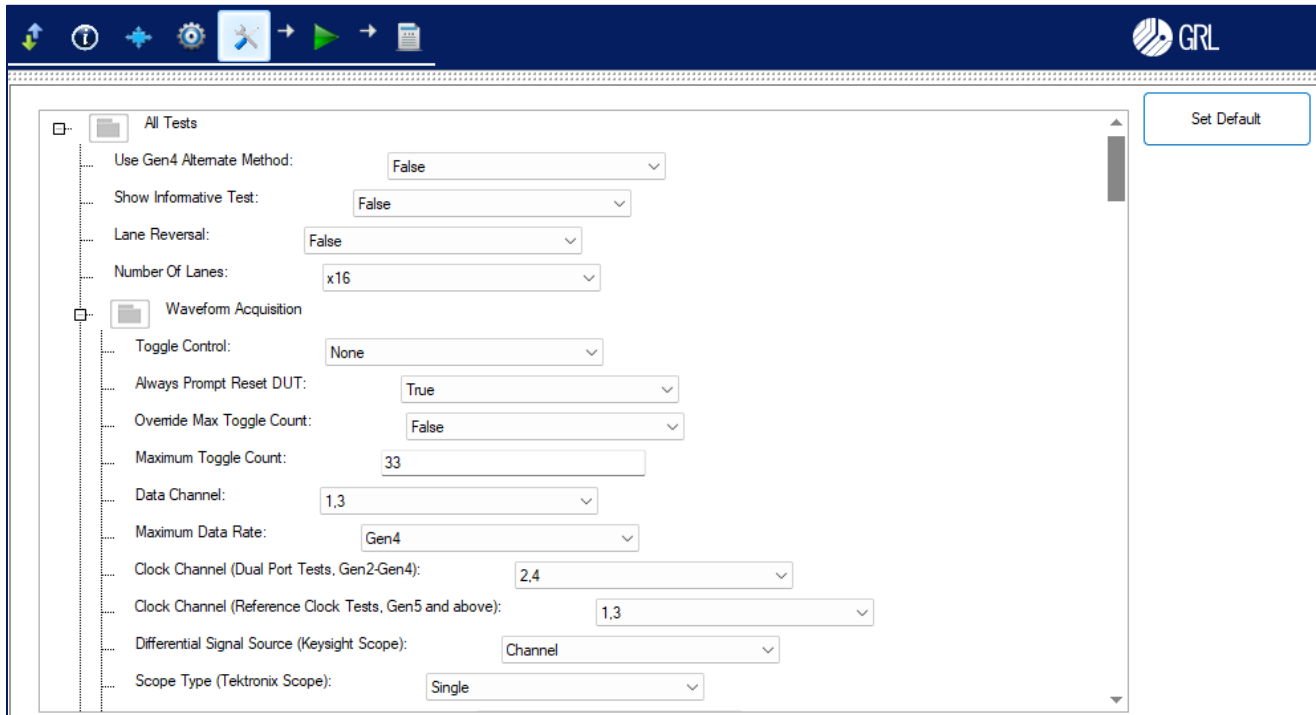


FIGURE 46. TEST PARAMETERS CONFIGURATION PAGE

TABLE 4. TEST PARAMETERS DESCRIPTION

Parameter	Description
Use Gen4 Alternate Method	Select “True” to enable the alternative method of performing PCIe Gen4 System Signal Quality test where the Data and 100 MHz Reference Clock can be captured and post-processed separately.
Show Informative Test	Select “True” to enable tests that are run for information purpose only to be displayed in the test list.
Lane Reversal	Select “True” to enable the connection of PCIe lanes between the host and the peripheral device to be reversed.
Number Of Lanes	Select the number of PCIe lanes to be used as follows: X2: 2 lanes x4: 4 lanes x8: 8 lanes x16: 16 lanes

Parameter	Description
<i>Waveform Acquisition</i>	
Toggle Control	Select to use the GRL-P1 hardware controller or an embedded test script to provide compliance toggle signal to control the compliance state of the DUT. Select “None” if using manual compliance toggle.
Always Prompt Reset DUT	Select “True” to allow the GRL Platform Solutions software to send prompts for DUT reset during waveform acquisition.
Override Max Toggle Count	Select “True” to override the maximum limit of compliance toggle signal switching that is set in the “Maximum Toggle Count” field below.
Maximum Toggle Count	Specify the maximum limit for compliance toggle signal switching.
Data Channel	Select the Scope channels that are connected to the Data Lanes of the respective test fixture.
Maximum Data Rate	Select the highest level for the PCIe data rate to perform tests.
Clock Channel (Dual Port Tests, Gen2-Gen4)	Select the Scope channels that are connected to the Reference Clock of the respective test fixture for 2-port testing. This is only applicable for PCIe Gen2 to Gen4.
Clock Channel (Reference Clock Tests, Gen5 and above)	Select the Scope channels that are connected to the Reference Clock of the respective test fixture. This is only applicable for PCIe Gen5 and above.
Differential Signal Source (Keysight Scope)	If using the Keysight Scope, select the channel or function to be used as the differential signal source.
Scope Type (Tektronix Scope)	If using the Tektronix Scope, select the Single-shot based Scope or the Tektronix’ owned Dual Asynchronous Time Interleaving (Dual ATI) based Scope.
Attenuation (Tektronix ATI Scope) (dB)	If using the Tektronix ATI based Scope, enter the attenuation value.
Channel Skew (Tektronix ATI Scope) (ps)	If using the Tektronix ATI based Scope, enter the channel skew or timing to perform alignment of the Scope channels.
Fixture Type	Select a PCIe compliance test fixture in use.
Always AutoScale	Select “True” to always enable autoscaling for connected channels on the Scope.
Data/Clock Channel Auto Scale	Select “True” to enable autoscaling for connected Data or Reference Clock channels on the Scope.
Data/Clock Vertical V_{Diff} Range (V)	Set the vertical range of the Scope to easily detect a change to the voltage level when running tests.

Parameter	Description
Gen3 Apply Embedding	Select “True” to enable embedding to be performed during tests for PCIe Gen3.
Gen4 Apply Embedding	Select “True” to enable embedding to be performed during tests for PCIe Gen4.
Gen5 Apply Embedding	Select “True” to enable embedding to be performed during tests for PCIe Gen5.
Gen6 Apply Embedding	Select “True” to enable embedding to be performed during tests for PCIe Gen6.
Gen6 Apply BT4 Filter	Select “True” to enable the 4th order Bessel-Thomson filter on the scope for PCIe Gen6.
Enable Deembedding (Tektronix ATI Scope)	If using the Tektronix ATI based Scope, select “True” to enable de-embedding to be performed during tests.
Positive Channel Deembedding File (Tektronix ATI Scope)	If using the Tektronix ATI based Scope, enter the name of the de-embedding filter file (.flt) for the data positive signal.
Negative Channel Deembedding File (Tektronix ATI Scope)	If using the Tektronix ATI based Scope, enter the name of the de-embedding filter file (.flt) for the data negative signal.
Auto Reset	Select the option to automatically power cycle the controller during tests.
Switch Matrix	Select “True” to enable using an RF switch in the test setup.
Wait Time After Reset (ms)	If “Auto Reset” has been enabled for the controller, specify the time interval in milliseconds to stand by after reset.
Lane to Test Preset	Select the lane to be tested across PCIe presets.
#Average (SNDR Test)	Set the scope averaging value for Signal to Noise and Distortion Ratio (SNDR) calculation.
Remote File Server IP Address	Enter the IP address for the GRL Platform Solutions Remote Proxy Server. See Section 3.2.1 on how to set up the remote file server.
Remote File Server Port Number	Enter the Port number for the GRL Platform Solutions Remote Proxy Server. See Section 3.2.1 on how to set up the remote file server.
<i>Add-In Card PCIe Gen3 Test</i>	
Gen3 System Embedding File	If “Gen3 Apply Embedding” has been set to “True”, select a standard or custom embedding file template to be used for embedding of the PCIe Gen3 system channel.

Parameter	Description
Gen3 Custom System Embedding File	If “Gen3 Apply Embedding” has been set to “True” and the “Custom” embedding file template has been selected, enter the name of the file template to be used for embedding of the PCIe Gen3 system channel.
<i>Add-In Card PCIe Gen4 Signal Quality Test</i>	
Gen4 System Embedding File	If “Gen4 Apply Embedding” has been set to “True”, select a standard or custom embedding file template to be used for embedding of the PCIe Gen4 system channel.
Gen4 Custom System Embedding File	If “Gen4 Apply Embedding” has been set to “True” and the “Custom” embedding file template has been selected, enter the name of the file template to be used for embedding of the PCIe Gen4 system channel.
<i>Add-In Card PCIe Gen5 Signal Quality Test</i>	
Gen5 System Embedding File	If “Gen5 Apply Embedding” has been set to “True”, select a standard or custom embedding file template to be used for embedding of the PCIe Gen5 system channel.
Gen5 Custom System Embedding File	If “Gen5 Apply Embedding” has been set to “True” and the “Custom” embedding file template has been selected, enter the name of the file template to be used for embedding of the PCIe Gen5 system channel.
<i>Add-In Card PCIe Gen6 Signal Quality Test</i>	
Gen6 System Embedding File	If “Gen6 Apply Embedding” has been set to “True”, select a standard or custom embedding file template to be used for embedding of the PCIe Gen6 system channel.
Gen6 Custom System Embedding File	If “Gen6 Apply Embedding” has been set to “True” and the “Custom” embedding file template has been selected, enter the name of the file template to be used for embedding of the PCIe Gen6 system channel.
<i>System Board Acquisition PCIe Gen3 Test</i>	
Gen3 AIC Embedding File	If “Gen3 Apply Embedding” has been set to “True”, select a standard or custom embedding file template to be used for embedding of the PCIe Gen3 add-in card channel.
Gen3 Custom AIC Embedding File	If “Gen3 Apply Embedding” has been set to “True” and the “Custom” embedding file template has been selected, enter the name of the file template to be used for embedding of the PCIe Gen3 add-in card channel.
<i>PCIe Gen4 Signal Quality Test (System)</i>	
Gen4 AIC Embedding File	If “Gen4 Apply Embedding” has been set to “True”, select a standard or custom embedding file template to be used for embedding of the PCIe Gen4 add-in card channel.

Parameter	Description
Gen4 Custom AIC Embedding File	If “Gen4 Apply Embedding” has been set to “True” and the “Custom” embedding file template has been selected, enter the name of the file template to be used for embedding of the PCIe Gen4 add-in card channel.
<i>PCIe Gen5 Signal Quality Test (System)</i>	
Gen5 AIC Embedding File	If “Gen5 Apply Embedding” has been set to “True”, select a standard or custom embedding file template to be used for embedding of the PCIe Gen5 add-in card channel.
Gen5 Custom AIC Embedding File	If “Gen5 Apply Embedding” has been set to “True” and the “Custom” embedding file template has been selected, enter the name of the file template to be used for embedding of the PCIe Gen5 add-in card channel.
<i>PCIe Gen6 Signal Quality Test (System)</i>	
Gen6 AIC Embedding File	If “Gen6 Apply Embedding” has been set to “True”, select a standard or custom embedding file template to be used for embedding of the PCIe Gen6 add-in card channel.
Gen6 Custom AIC Embedding File	If “Gen6 Apply Embedding” has been set to “True” and the “Custom” embedding file template has been selected, enter the name of the file template to be used for embedding of the PCIe Gen6 add-in card channel.
<i>System Ref Clock</i>	
Ref Clock Scope Bandwidth (GHz)	Set the scope bandwidth for the system reference clock.
System Clock Cycles	Set the number of times to generate the system reference clock.
Min Sample Rate (GSa/s)	Set the minimum sampling rate for the system reference clock.
<i>Gen 1 to Gen 6 (2.5G – 64.0G)</i>	
UI (M) [Gen1/Gen2/Gen3/Gen4/Gen5/Gen6]	Specify the number of sample points to capture for each data rate.
Sample Rate (GSa/s) [Gen1/Gen2/Gen3/Gen4/Gen5/Gen6]	Specify the real-time sample rate in Gb/s to capture the required waveform data.
Gen3/Gen4/Gen5/Gen6 Signal Quality Test Preset	Select the preset to be applied for the PCIe Gen3, Gen4, Gen5 or Gen6 signal quality test.
Use Real Edge (Keysight Scope) (Gen5 or Gen6)	Select “True” to use real edge channels on the Keysight scope for PCIe Gen5 or Gen6 compliance testing.

Parameter	Description
Gen5/Gen6 SQ Test Custom Presets	Set custom presets for the PCIe Gen5 or Gen6 signal quality waveform test.
Gen3/Gen4/Gen5/Gen6 Scope Bandwidth (GHz)	Set the scope bandwidth for the PCIe Gen3, Gen4, Gen5 or Gen6 waveform acquisition.
Gen5/Gen6 Number of Waveforms	Specify the number of waveforms to acquire for PCIe Gen5 or Gen6.
Gen5/Gen6 Waveform Index to Process	If “Gen5/Gen6 Number of Waveforms” have been set to > 1, then specify which waveform to be processed using the zero based index protocol for PCIe Gen5 or Gen6. For example, if the number of waveforms to be acquired have been set to “3” and “0” is entered as the “Waveform Index to Process”, this means that the first of the three acquired waveforms will be processed. If the index is set to “1” or “2”, the second or third waveform will be processed respectively.
<i>Waveform Analysis</i>	
SigTest Run Mode	Select the SigTest to run Sequential or Parallel signal quality testing to ensure waveform compliance.
SigTest Max Thread	Specify the maximum number of threads for each SigTest run.
SSC Support	Select “True” to enable Spread Spectrum Clock (SSC) capabilities for testing (if supported by the DUT).
Clock Jitter Noise Floor De-Embed	Select “True” to enable de-embedding of the clock jitter and voltage noise in the data stream.
SigTest Noise Floor De-Embed (Gen6 and above)	Select “True” to enable de-embedding of the SigTest noise floor signal for PCIe Gen6 and above.
SNDR Measurement Method	Select to use SigTest or GRL Platform Solutions method to read the saved waveform file and compute the SNDR value.
<i>Add-In Card (PCIe Gen6)</i>	
CTLE Setting (Preset Tests)	Select to use the SigTest PCIe Gen6 No_CTLE template file or an appropriate CTLE index (behavioral CTLE from -5 dB to -15 dB) template file to read the saved waveform files and compute the preset values for the add-in card.
CTLE Setting (Jitter Tests)	Select to use the SigTest PCIe Gen6 No_CTLE template file or 64.0 GT/s Add-in Card transmitter test Optimize CTLE template file or an appropriate CTLE index (behavioral CTLE from -5 dB to -15 dB) template file to read the saved waveform files and measure the jitter parameters for the add-in card.
CTLE Setting (Signal Quality Tests)	Select to use the SigTest PCIe Gen6 No_CTLE template file or 64.0 GT/s Add-in Card transmitter test Optimize CTLE template file or an appropriate CTLE index (behavioral CTLE

	from -5 dB to -15 dB) template file to read the saved waveform files and measure the eye height & eye width using the SigTest analysis program for the add-in card.
Seasim Fallback Jitter	Select to use Fixed or Measured jitter when the jitter occurs in a fallback state of the PCIe link (at a slower speed). If not, select 'None'.
TX-UPW-TJ (ps)	Set the value of the Uncorrelated Total Pulse Width Jitter ($T_{TX-UPW-TJ}$) in ps to be used for the add-in card measurement.
TX-UPW-DJDD (ps p-p)	Set the value of the Uncorrelated Deterministic Pulse Width Jitter ($T_{TX-UPW-DJDD}$) in ps p-p to be used for the add-in card measurement.
TX-UTJ (ps)	Set the value of the Uncorrelated Total Jitter (T_{TX-UTJ}) in ps to be used for the add-in card measurement.
TX-UDJDD (ps p-p)	Set the value of the Uncorrelated Deterministic Jitter ($T_{TX-UDJDD}$) in ps p-p to be used for the add-in card measurement.
System Board (PCIe Gen6)	
CTLE Setting (Preset Tests)	Select to use the SigTest PCIe Gen6 No_CTLE template file or an appropriate CTLE index (behavioral CTLE from -5 dB to -15 dB) template file to read the saved waveform files and compute the preset values for the system board.
CTLE Setting (Jitter Tests)	Select to use the SigTest PCIe Gen6 No_CTLE template file or 64.0 GT/s System Board transmitter test Optimize CTLE template file or an appropriate CTLE index (behavioral CTLE from -5 dB to -15 dB) template file to read the saved waveform files and measure the jitter parameters for the system board.
CTLE Setting (Signal Quality Tests)	Select to use the SigTest PCIe Gen6 No_CTLE template file or 64.0 GT/s System Board transmitter test Optimize CTLE template file or an appropriate CTLE index (behavioral CTLE from -5 dB to -15 dB) template file to read the saved waveform files and measure the eye height & eye width using the SigTest analysis program for the system board.

4.3 Run Automation Tests

Once tests have been selected and set up from the previous sections, the tests are now ready to be run.

Select  from the menu to access the Run Tests page. The GRL-PXE-TX software automatically runs the selected tests when initiated.

Before running the tests, select the option to:

- **Skip Test if Result Exists** – If results from previous tests exist, the software will *skip* those tests.
- **Replace if Result Exists** – If results from previous tests exist, the software will *replace* those tests with new results.

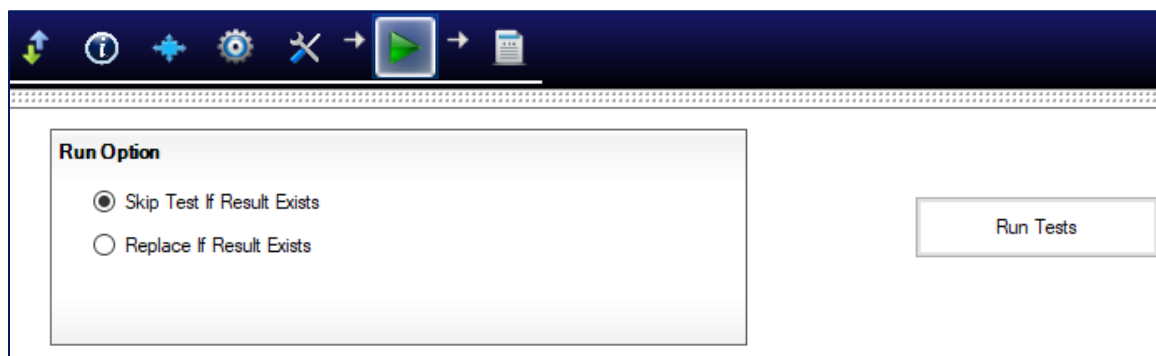


FIGURE 47. RUN TESTS PAGE

Select the **Run Tests** button to start running the selected tests. The connection diagram for the test being run will initially appear to allow the user to make sure that the test environment has been properly set up before testing can proceed. Follow the step-by-step instructions to complete the entire testing.

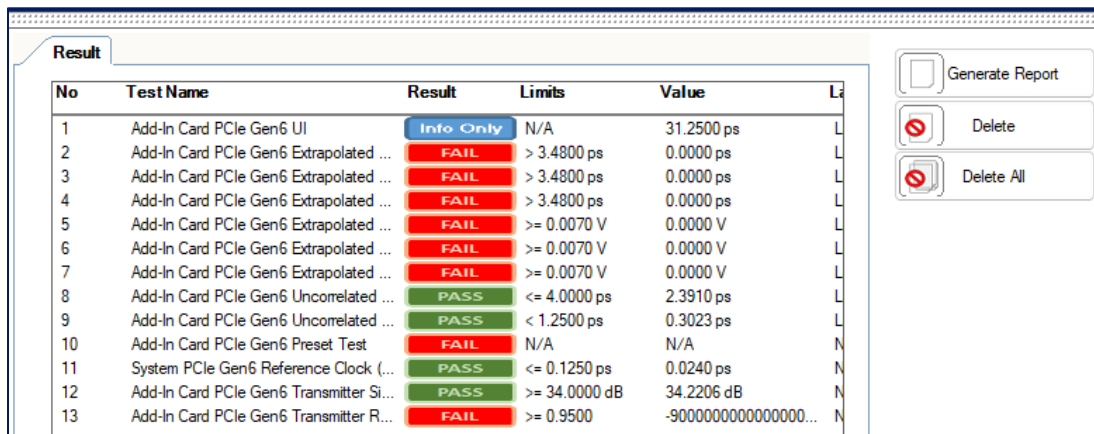
5 Interpreting GRL-PXE-TX Test Report

When all test runs have completed from Section 4, the GRL-PXE-TX software will automatically display the test results on the **Report** page.

Select  from the menu to access the Report page to view the results from each test run.

If some of the results are not desired, they can be individually deleted by selecting the **Delete** button.

Also select the **Generate Report** button to generate a detailed test report in the PDF format.



No	Test Name	Result	Limits	Value	La
1	Add-In Card PCIe Gen6 UI	Info Only	N/A	31.2500 ps	L
2	Add-In Card PCIe Gen6 Extrapolated ...	FAIL	> 3.4800 ps	0.0000 ps	L
3	Add-In Card PCIe Gen6 Extrapolated ...	FAIL	> 3.4800 ps	0.0000 ps	L
4	Add-In Card PCIe Gen6 Extrapolated ...	FAIL	> 3.4800 ps	0.0000 ps	L
5	Add-In Card PCIe Gen6 Extrapolated ...	FAIL	>= 0.0070 V	0.0000 V	L
6	Add-In Card PCIe Gen6 Extrapolated ...	FAIL	>= 0.0070 V	0.0000 V	L
7	Add-In Card PCIe Gen6 Extrapolated ...	FAIL	>= 0.0070 V	0.0000 V	L
8	Add-In Card PCIe Gen6 Uncorrelated ...	PASS	<= 4.0000 ps	2.3910 ps	L
9	Add-In Card PCIe Gen6 Uncorrelated ...	PASS	< 1.2500 ps	0.3023 ps	L
10	Add-In Card PCIe Gen6 Preset Test	FAIL	N/A	N/A	N
11	System PCIe Gen6 Reference Clock (...)	PASS	<= 0.1250 ps	0.0240 ps	N
12	Add-In Card PCIe Gen6 Transmitter Si...	PASS	>= 34.0000 dB	34.2206 dB	N
13	Add-In Card PCIe Gen6 Transmitter R...	FAIL	>= 0.9500	-9000000000000000...	N

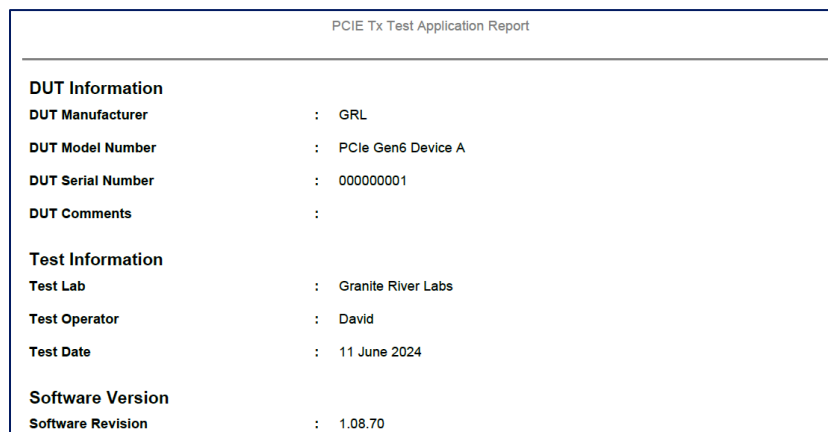
FIGURE 48. TEST REPORT PAGE

5.1 Understand Test Report Information

This section gives a general overview of the test report to help users familiarize themselves with the format. Select the **Generate report** button to generate the test report.

5.1.1 Test Session Information

This portion displays the information previously entered on the **Session Info** page.



PCIE Tx Test Application Report	
DUT Information	
DUT Manufacturer	: GRL
DUT Model Number	: PCIe Gen6 Device A
DUT Serial Number	: 000000001
DUT Comments	:
Test Information	
Test Lab	: Granite River Labs
Test Operator	: David
Test Date	: 11 June 2024
Software Version	
Software Revision	: 1.08.70

FIGURE 49. TEST SESSION INFORMATION EXAMPLE

5.1.2 Test Summary Table

This table provides an overall view of all the tests performed along with their test conditions and results.

PCIE Tx Test Application Report							
No	TestName	Limits	Value	Results	Lane	Data Rate	Preset
1	Add-In Card PCIe Gen6 U	N/A	31.2500 ps	InfoOnly	Lane0	64.0 GT/s - Gen6	P7
2	Add-In Card PCIe Gen6 Extrapolated Eye Width (01 Eye)	> 3.4800 ps	0.0000 ps	Fail	Lane0	64.0 GT/s - Gen6	P7
3	Add-In Card PCIe Gen6 Extrapolated Eye Width (12 Eye)	> 3.4800 ps	0.0000 ps	Fail	Lane0	64.0 GT/s - Gen6	P7
4	Add-In Card PCIe Gen6 Extrapolated Eye Width (23 Eye)	> 3.4800 ps	0.0000 ps	Fail	Lane0	64.0 GT/s - Gen6	P7
5	Add-In Card PCIe Gen6 Extrapolated Eye Height (01 Eye)	>= 0.0070 V	0.0000 V	Fail	Lane0	64.0 GT/s - Gen6	P7
6	Add-In Card PCIe Gen6 Extrapolated Eye Height (12 Eye)	>= 0.0070 V	0.0000 V	Fail	Lane0	64.0 GT/s - Gen6	P7
7	Add-In Card PCIe Gen6 Extrapolated Eye Height (23 Eye)	>= 0.0070 V	0.0000 V	Fail	Lane0	64.0 GT/s - Gen6	P7
8	Add-In Card PCIe Gen6 Uncorrelated PWJ TI @ F-6	<= 4.0000 ps	2.3910 ps	Pass	Lane0	64.0 GT/s - Gen6	N/A
9	Add-In Card PCIe Gen6 Uncorrelated PWJ DI @ F-6	< 1.2500 ps	0.3023 ps	Pass	Lane0	64.0 GT/s - Gen6	N/A
10	Add-In Card PCIe Gen6 Preset Test	N/A	N/A	Fail			
11	System PCIe Gen6 Reference Clock (100MHz) Jitter	<= 0.1250 ps	0.0240 ps	Pass	N/A	64.0 GT/s - Gen6	N/A
12	Add-In Card PCIe Gen6 Transmitter Signal-to-Noise and Distortion Ratio (SNDRTX)	>= 34.0000 dB	34.2206 dB	Pass			
13	Add-In Card PCIe Gen6 Transmitter Ratio of Level Mismatch (RLM-TX)	>= 0.9500	-	Fail			

FIGURE 50. TEST SUMMARY TABLE EXAMPLE

5.1.3 Test Results

This portion displays the results of each test performed in detail.

12. Add-In Card PCIe Gen6 Transmitter Signal-to-Noise and Distortion Ratio (SNDRTX)	
Pass/Fail Stats	: Pass
Test Limits	: >= 34.0000 dB
Result	: 34.2206 dB
Test completed time	: 08 May 2024 23:36:53 PM

7. Add-In Card PCIe Gen6 Extrapolated Eye Height (23 Eye) [Lane0,Gen6,P7]	
Pass/Fail Stats	: Fail
Test Limits	: >= 0.0070 V
Result	: 0.0000 V
SigTest Version	: 6.1.00
DUT Type:	: Add-In Card
Extrap EH_23	: 0E-3
Connector Type	: CEM
Test completed time	: 03 June 2024 1:11:05 AM

FIGURE 51. TEST RESULTS EXAMPLE

5.2 Delete Test Results

Select the **Delete** button to delete individual test results or **Delete All** to delete all test results.

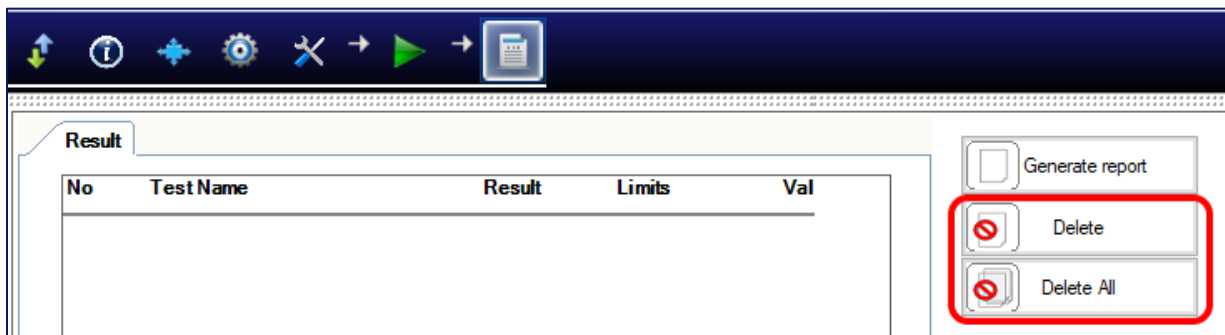


FIGURE 52. DELETE TEST RESULTS

6 Saving and Loading GRL-PXE-TX Test Sessions

The usage model for the GRL-PXE-TX software is that the test results are created and maintained as a 'Live Session' in the application. This allows the user to quit the application and return later to continue where the user left off.

Save and Load Sessions are used to save a test session that the user may want to recall later. The user can 'switch' between different sessions by saving and loading them when needed.

- To **save a test session**, with all of the test parameter information, test results, and any waveforms, select the Options drop-down menu and then select "Save Session".
- To **load a test session** back into the application, including the saved test parameter settings, select Options → "Load Session".
- To **create a new test session** and return the application back to the default configuration, select Options → "New Session".

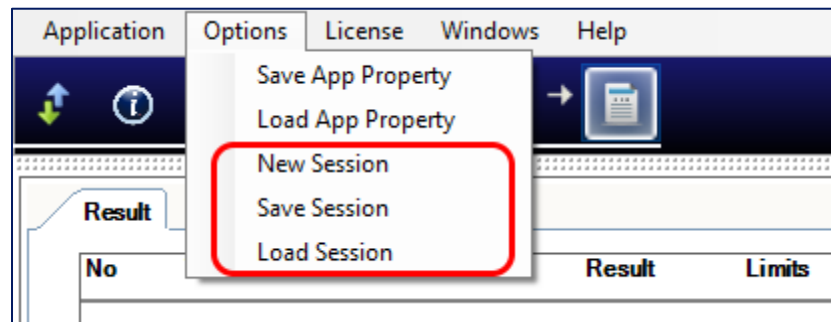


FIGURE 53. SAVE/LOAD/CREATE TEST SESSIONS

The test configuration and session results are saved in a file with the '.ses' extension, which is a compressed zip-style file, containing a variety of information.

7 Appendix A: Method of Implementation (MOI) for Manual PCIe 6.0 Transmitter Measurements

This section describes how to manually perform PCIe 6.0 CEM based Tx compliance testing following the recommended test procedure from the PCI Express Architecture PHY Test Specification Rev 6.0.

The following steps give a general overview for testing the PCIe 6.0 CEM based Tx DUT:

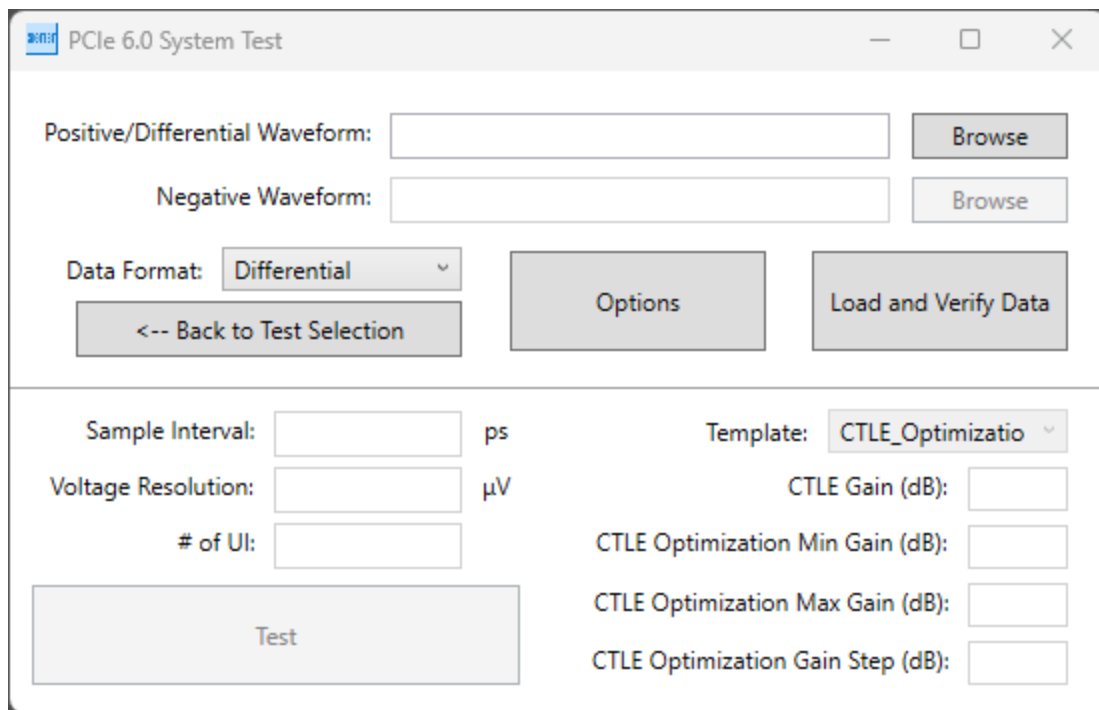
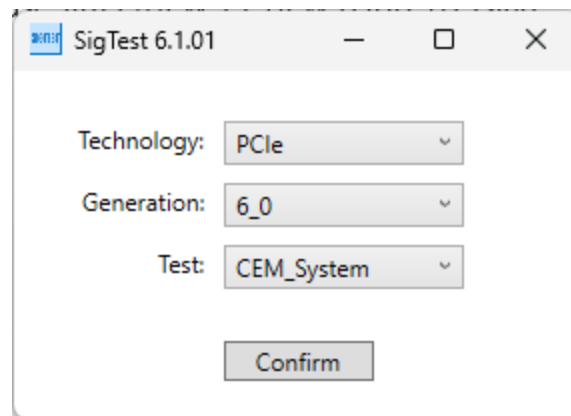
- i) Test for System Board & Add-in Card DUT Tx Signal Quality compliance:
 - 3.0M UI acquisition for any Tx EQ Preset (Q0-Q10)
 - Post-processing of acquired waveforms with SigTest Phoenix for:
 - Top Eye Width ≥ 3.48 ps and Top Eye Height ≥ 7 mV (for Add-In Card DUT)
 - Top Eye Width ≥ 3.13 ps and Top Eye Height ≥ 6 mV (for System Board DUT)
- ii) Test for Add-in Card DUT Base Jitter (UPW-TJ, UPW-DJDD, UTJ and UDJDD) compliance:
 - 3.0M UI acquisition and post-processing of acquired waveforms with SigTest for:
 - $UPW-TJ \leq 4$ ps
 - $UPW-DJDD \leq 1.25$ ps
 - $UTJ \leq 4$ ps
 - $UDJDD \leq 1.563$ ps
- iii) Test for System Board 100 MHz Refclk Jitter compliance:
 - 80000 clock cycle acquisition:
 - $RJ < 125$ fs

7.1 System Board Tx Signal Quality Test

Note: Make sure to terminate lanes that are not being tested with 50-ohm MMPX terminators.

1. Set up the test equipment as described in Section 4.2.1.
2. Adjust the Scope to capture 3M UI's using the following configuration:
 - Bandwidth: 50 GHz
 - Sampling Rate: ≥ 192 GSa/s
3. Refer to "Appendix C, Section C.12, Target Loss Values – Tx Signal Quality" in the *PCI Express Architecture PHY Test Specification, Revision 6.0* to determine the target loss and locate the S4P file to be embedded on the Scope.
4. Push the compliance toggle on the DUT to transmit 64 GT/s compliance pattern by injecting 1 ms pulse of 100 MHz clock signal into Rx Lane 0.
5. On the Scope, capture 3.0M UI's for any Tx EQ Preset (Q0-Q10). Save the captured waveforms to be used for post-processing.

6. To test for signal quality, load the saved waveform files in SigTest Phoenix (by selecting **PCIe** → **6_0** → **CEM_System** → **Browse** → **Load and Verify Data**). *[Make sure the file contains the appropriate trace loss and embedded package model losses.]*

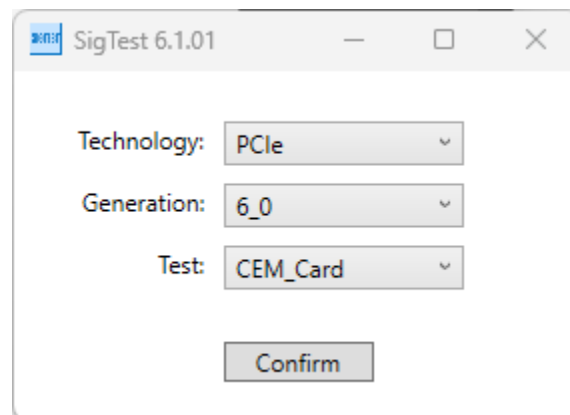


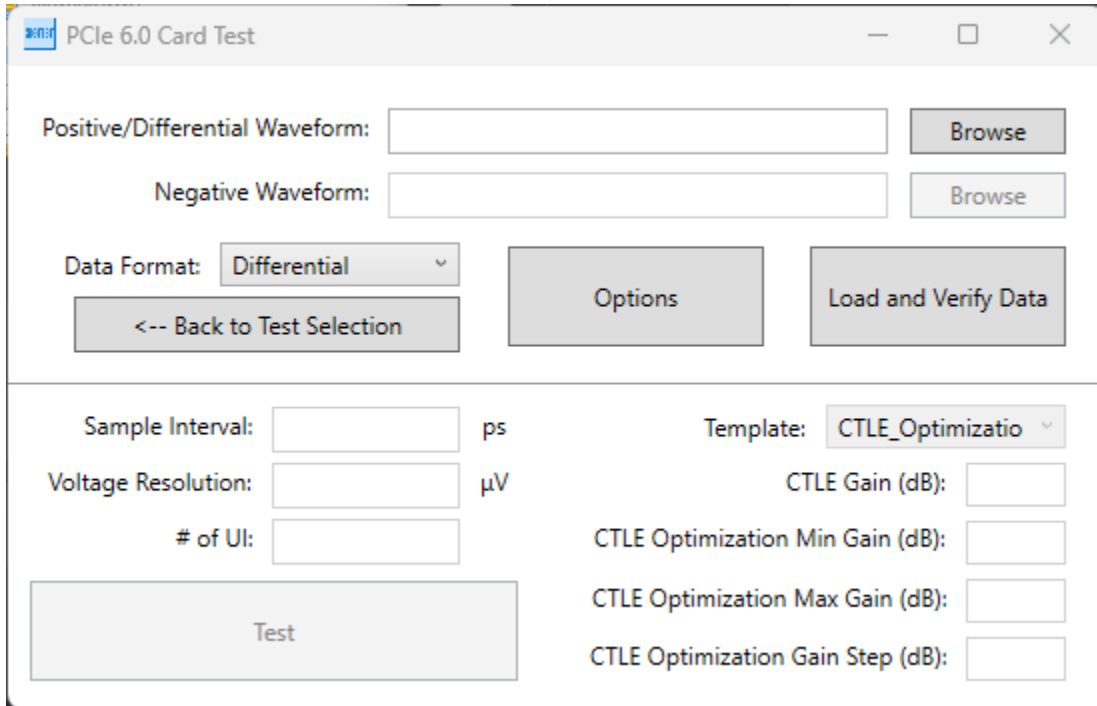
7. Measure both the Eye Height and Eye Width @1e-6 on the SigTest. Use the “Templates\PCIe\6_0\System\Optimize_CTLE.dat” template file if SSC is Off. Use the “Templates\PCIe\6_0\System\Optimize_CTLE_SSC.dat” template file if SSC is On.
8. Make sure that each DUT test lane achieves the following target Eye Height and Eye Width values for at least one Tx EQ Preset:
- Eye Width ≥ 3.13 ps
 - Eye Height ≥ 6 mV

7.2 Add-in Card Tx Signal Quality Test

Note: Make sure to terminate lanes that are not being tested with 50-ohm MMPX terminators.

1. Set up the test equipment as described in Section 4.2.2.
2. Turn on SSC on the CBB (-0.5% SSC down-spread).
3. Adjust the Scope to capture 3M UI's using the following configuration:
 - Bandwidth: 50 GHz
 - Sampling Rate: ≥ 192 GSa/s
4. Refer to "Appendix C, Section C.12, Target Loss Values – Tx Signal Quality" in the *PCI Express Architecture PHY Test Specification, Revision 6.0*, to determine the target loss and locate the S4P file to be embedded on the Scope.
5. Push the compliance toggle on the DUT to transmit 64 GT/s compliance pattern by injecting 1 ms pulse of 100 MHz clock signal into Rx Lane 0.
6. On the Scope, capture 3.0M UI's for any Tx EQ Preset (Q0-Q10). Save the captured waveforms to be used for post-processing.
7. To test for signal quality, load the saved waveform files in SigTest Phoenix (by selecting **PCIe** → **6_0** → **CEM_Card** → **Browse** → **Load and Verify Data**) (*Make sure the file contains the appropriate trace loss and package model losses embedded with the captured waveform.*)





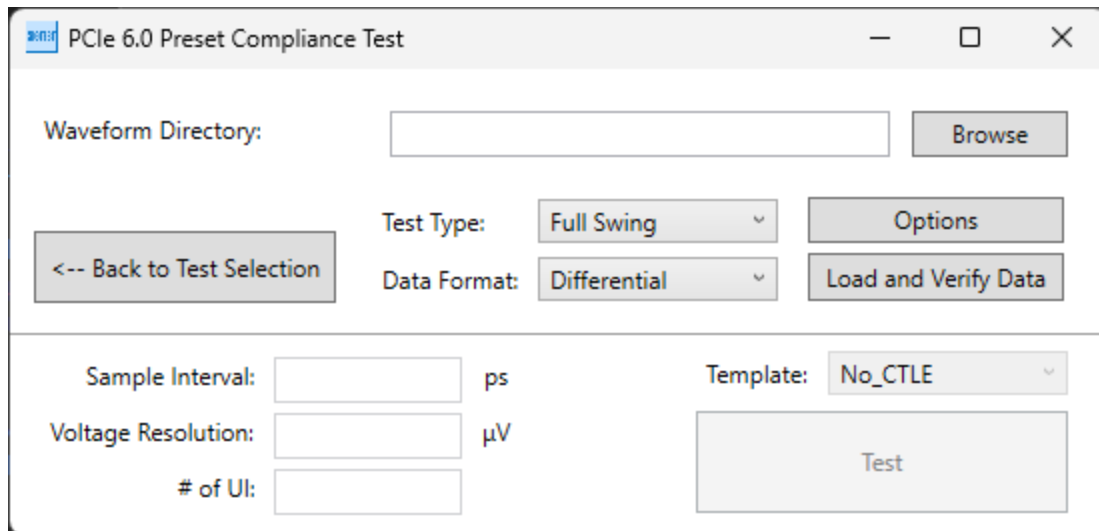
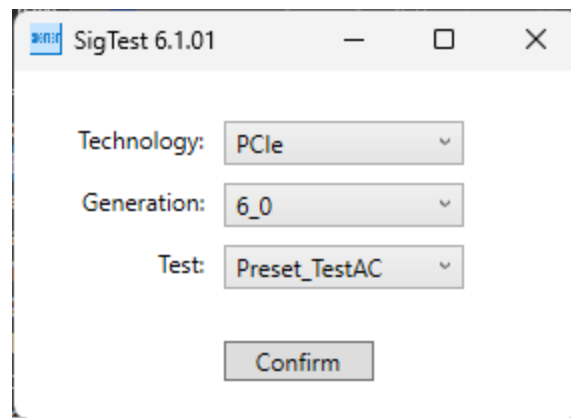
8. Measure both the Eye Height and Eye Width @1e-6 on the SigTest. Use the “PCIe\6_0\Card\optimize_CTLE.dat” template file.
9. Make sure that each DUT test lane achieves the following target Eye Height and Eye Width values for at least one Tx EQ Preset:
 - Eye Width ≥ 3.48 ps
 - Eye Height ≥ 7 mV

7.3 System Board Tx Preset Test

Note: Make sure to terminate lanes that are not being tested with 50-ohm MMPX terminators.

1. Set up the test equipment as described in Section 4.2.1.
2. Adjust the Scope to display Preset 0 (Q0) at 64 GT/s with the following configuration:
 - Bandwidth: 50 GHz
 - Sampling Rate: ≥ 192 GSa/s
 - No embedding
3. Push the compliance toggle on the DUT to capture Presets 0 to 10 (Q0-Q10) on Lane 0. Save the captured presets to be used for post-processing.
4. Save waveforms of all presets as “System_LaneX_Gen6_Q0Y_d_**wtf**”, where:
 - X = Lane number (0 to 15)
 - Y = Preset number (0 to 10)
 - wtf = waveform format (for example, .wfm for the Tekscope waveform or .bin for the Keysight waveform)

- To test the presets, load the saved preset files in SigTest (by selecting **PCIe** → **6_0** → **PresetTestAC** → **Template “No_CTLE”** → **Browse**) and run the preset tests (by selecting **Test**).



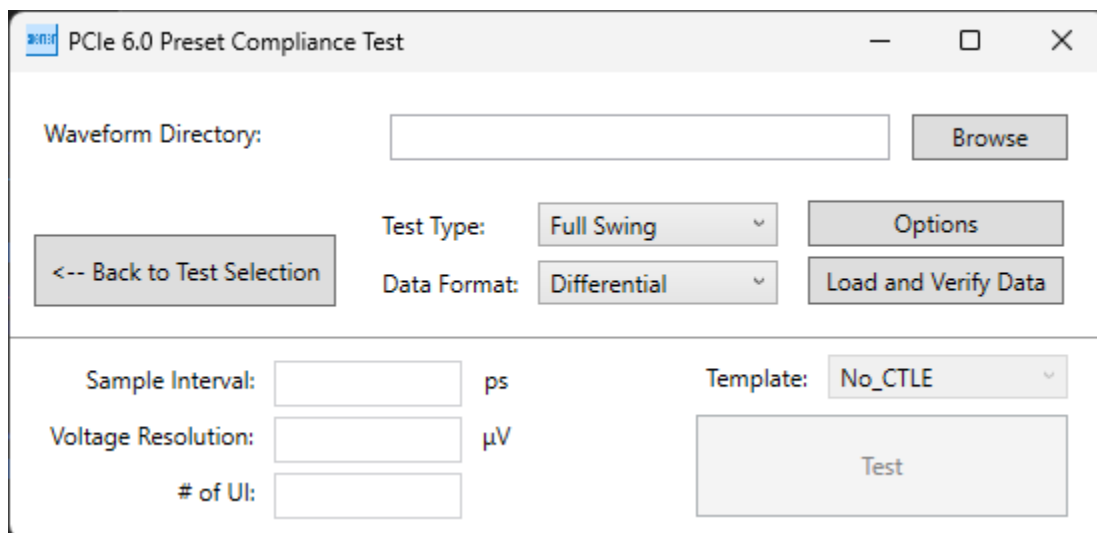
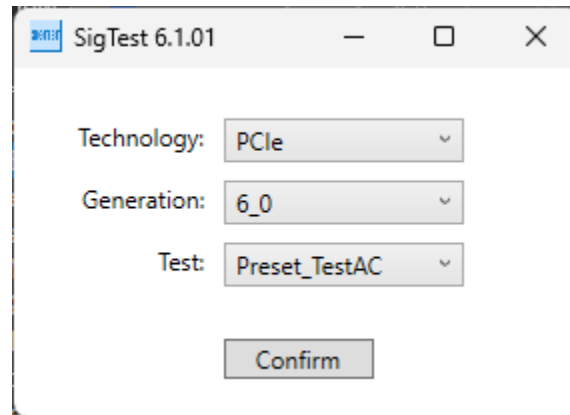
- When the preset tests have completed, select **Exit** to save the test results.

7.4 Add-In Card Tx Preset Test

Note: Make sure to terminate lanes that are not being tested with 50-ohm MMPX terminators.

- Set up the test equipment as described in Section 4.2.2.
- Turn on SSC on the CBB (-0.5% SSC down-spread).
- Adjust the Scope to display Preset 0 (Q0) at 64 GT/s with the following configuration:
 - Bandwidth: 50 GHz
 - Sampling Rate: ≥ 192 GSa/s
 - No embedding
- Push the compliance toggle on the DUT to capture Presets 0 to 10 (Q0-Q10) on Lane 0. Save the captured presets to be used for post-processing.

5. Save waveforms of all presets as “AIC_Lane**X**_Gen6_Q0**Y**_d_**wtf**”, where:
 - X = Lane number (0 to 15)
 - Y = Preset number (0 to 10)
 - wtf = waveform format (for example, .wfm for the Tekscope waveform or .bin for the Keysight waveform)
6. To test the presets, load the saved preset files in SigTest (by selecting **PCIe** → **6_0** → **PresetTestAC** → **Template “No_CTLE”** → **Browse**) and run the preset tests (by selecting **Test**).

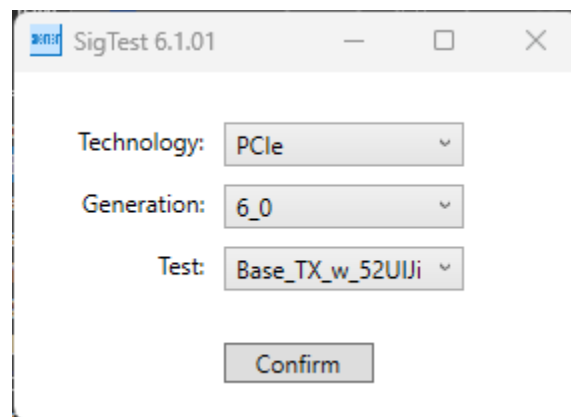


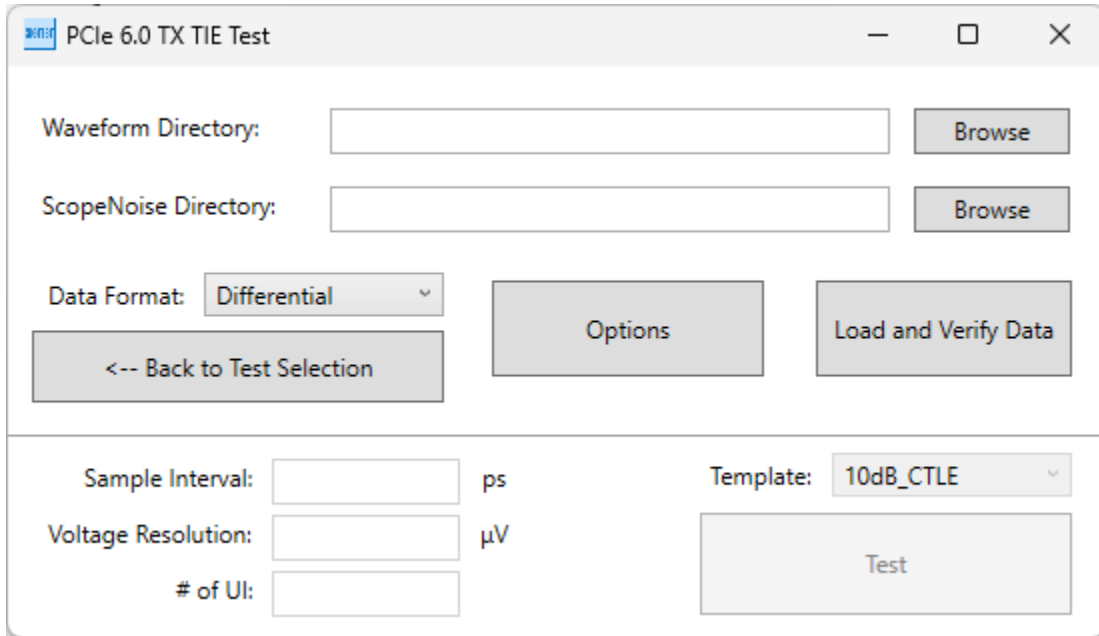
7. When the preset tests have completed, select **Exit** to save the test results.

7.5 Add-In Card Tx Base Jitter (UPW-TJ, UPW-DJDD, UTJ and UDJDD) Test

Note: Make sure to terminate lanes that are not being tested with 50-ohm MMPX terminators.

1. Set up the test equipment as described in Section 4.2.2.
2. Adjust the Scope to capture 3M UI's with the following configuration:
 - Bandwidth: 50 GHz
 - Sampling Rate: ≥ 192 GSa/s
 - Filter: 4th Order Bessel-Thomson @ 33 GHz
 - No embedding
3. Turn on SSC on the CBB (-0.5% SSC down-spread).
4. Push the compliance toggle on the DUT to transmit 64 GT/s Jitter Measurement pattern (setting #66 on Lane 0 in the PCIe 6.0 Base Specification and COMPAT on adjacent lanes) by injecting 1 ms pulse of 100 MHz clock signal into Rx Lane 0.
5. On the Scope, capture 3.0M UI's and save the captured waveforms to be used for post-processing.
6. To measure UTJ and UDJDD, load the saved waveform files in SigTest (by selecting **PCIe** → **6_0** → **Base_Tx_w_52UIJitterPattn** → **Browse** → **Load and Verify Data**).
7. Measure UTJ and UDJDD @1e-6 on the SigTest using the "PCIe/6_0/CEM_TX_Jitter/xx.dat" template file and select **Test** to start the measurements.





8. Push the compliance toggle on the DUT to transmit 64 GT/s High Swing Toggle pattern (setting #75 on Lane 0 in the PCIe 6.0 Base Specification and COMPAT on adjacent lanes) by injecting 1 ms pulse of 100 MHz clock signal into Rx Lane 0.
9. On the Scope, capture 3.0M UI's and save the captured waveforms to be used for post-processing.
10. To measure UPW-TJ, UPW-DJDD, load the saved waveform files in SigTest (by selecting **PCIe → 6_0 → Base_Tx_w_ClockPattn → Browse → Load and Verify Data**).
11. Measure UPW-TJ and UPW-DJDD @1e-6 on the SigTest using the "PCIe/6_0/CEM_TX_Jitter/ xx.dat" template file and select **Test** to start the measurements.
12. The test is considered as Pass if the following target jitter parameter values are met:
 - $UPW-TJ \leq 4 \text{ ps}$
 - $UPW-DJDD \leq 1.25 \text{ ps}$
 - $UTJ \leq 4 \text{ ps}$
 - $UDJDD \leq 1.563 \text{ ps}$

7.6 System Board Ref Clock (100 MHz) Jitter Test

Note: Make sure to terminate lanes that are not being tested with 50-ohm MMPX terminators.

1. Set up the test equipment as described in Section 4.2.3.
2. Adjust the Scope to capture >80K Clock Cycle (80000 * 10 ns = 0.8 ms).
3. SSC can be turned ON or OFF depending on the system board DUT.
4. Using the Clock Jitter Tool, measure the HF RJ RMS (Max Phase Jitter).
5. The test is considered as Pass if the HF RJ RMS (Max Phase Jitter) is $\leq 125 \text{ fs}$.

8 Appendix B: SigTest Tool Tab

The SigTest Tool allows the user to manually perform SigTest verification tests for the DUT using appropriate offline PCIe compliant SigTest template and waveform files. This function is used for debugging purposes.

1. Select  from the GRL-PXE-TX menu to access the Setup Configuration page.

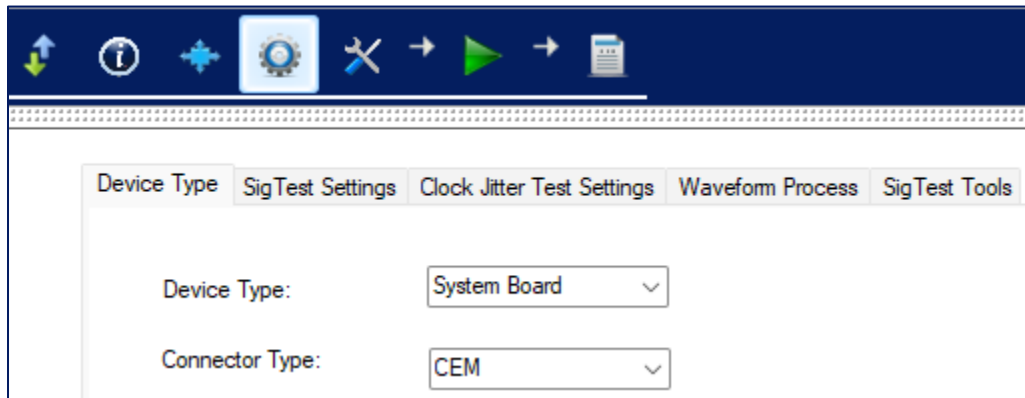


FIGURE 54. SETUP CONFIGURATION PAGE

2. Select the **SigTest Tools** tab.

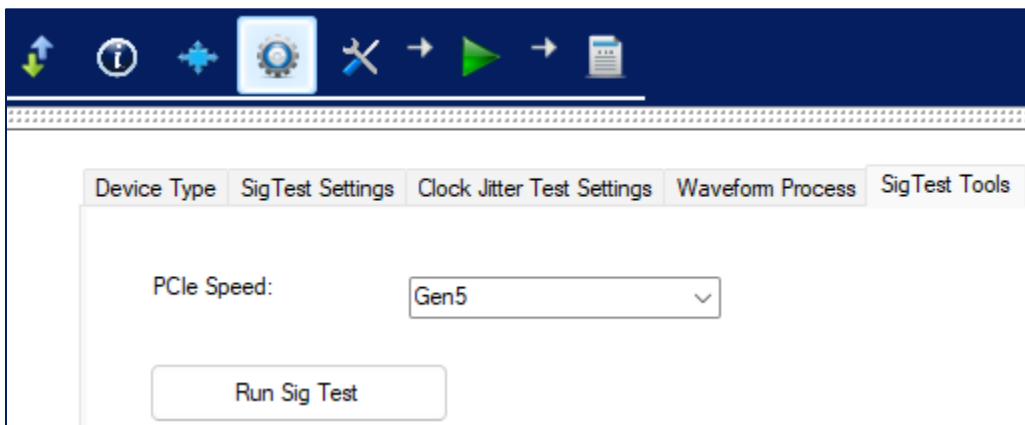


FIGURE 55. PERFORM SIGTEST DEBUGGING

3. Select the PCIe generation from the 'PCIe Speed' drop-down menu.
4. Then click on the 'Run SigTest' button to perform SigTest for the selected PCIe generation waveforms. The GRL-PXE-TX software will automatically run the SigTest for the waveforms as shown in the example below.

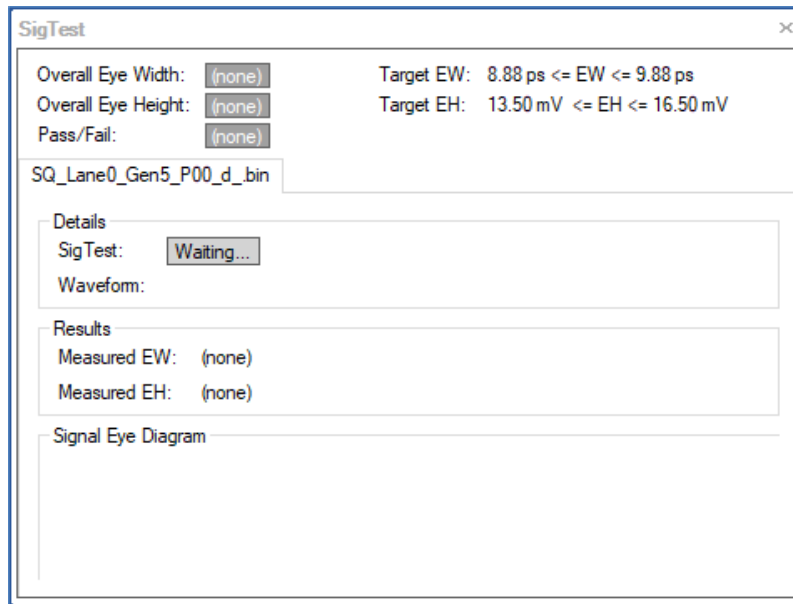


FIGURE 56. RUNNING OFFLINE SIGTEST VERIFICATION

- Once the test is completed, the results will be displayed like in the following example.

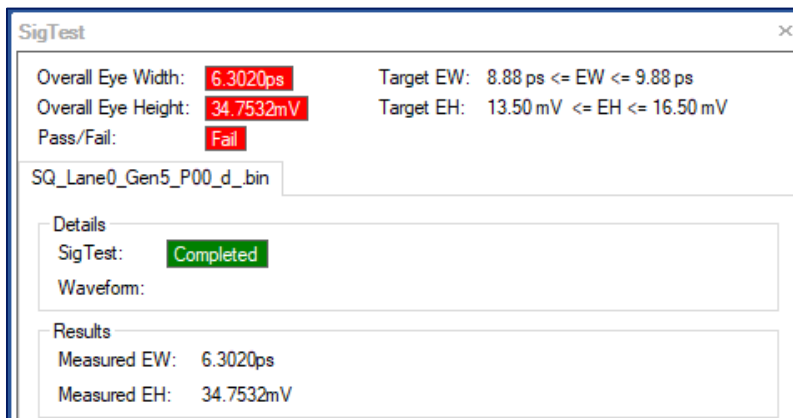


FIGURE 57. VIEWING SIGTEST ANALYSIS RESULTS

9 Appendix C: Connecting Keysight Oscilloscope to PC

If using a Keysight oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Keysight Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Keysight IO Libraries Suite software from the Keysight website and install on the PC.
2. When installed successfully, the IO icon () will appear in the taskbar notification area of the PC.
3. Select the IO icon to launch the **Keysight Connection Expert**.
4. Click Rescan.

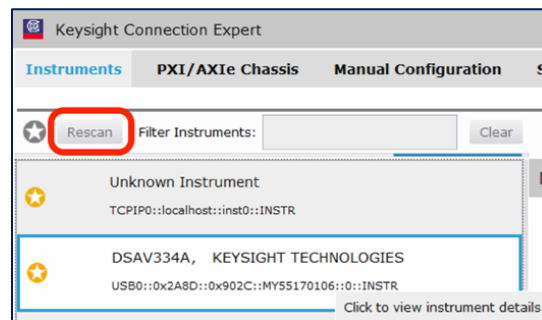


FIGURE 58. KEYSIGHT CONNECTION EXPERT

5. Refresh the system. The Keysight Scope is shown on the left pane and the VISA address is shown on the right pane.

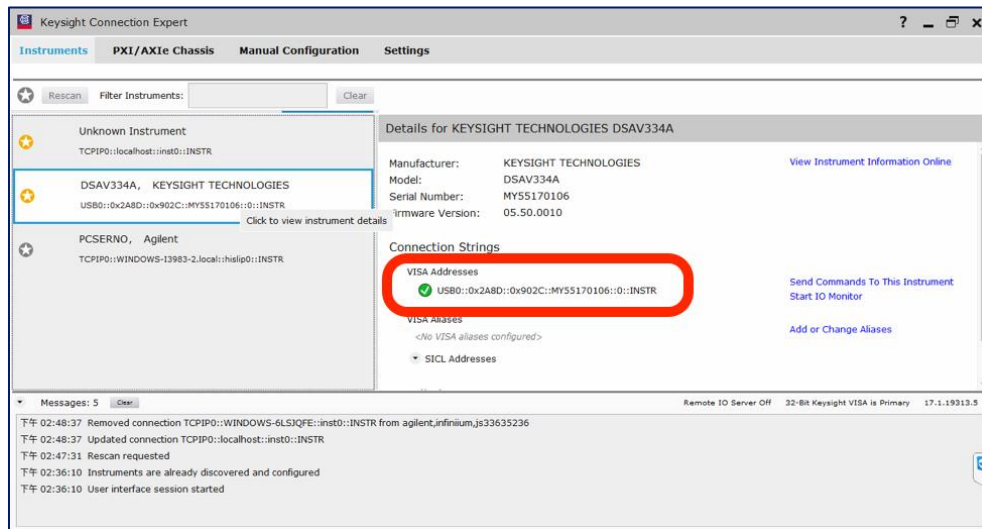


FIGURE 59. OSCILLOSCOPE'S VISA ADDRESS

6. When connecting the Keysight Scope to the PC through GPIB/USB, type in the VISA address into the 'Address' field on the Equipment Setup page of the GRL-PXE-TX Test Application. If connected via LAN, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to **omit** the Port number from the address.

10 Appendix D: Connecting Tektronix Oscilloscope to PC

If using a Tektronix DPOJET Series oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Tektronix Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Tektronix TekVISA software from the Tektronix website and install on the PC.
2. When installed successfully, open the OpenChoice Instrument Manager application.

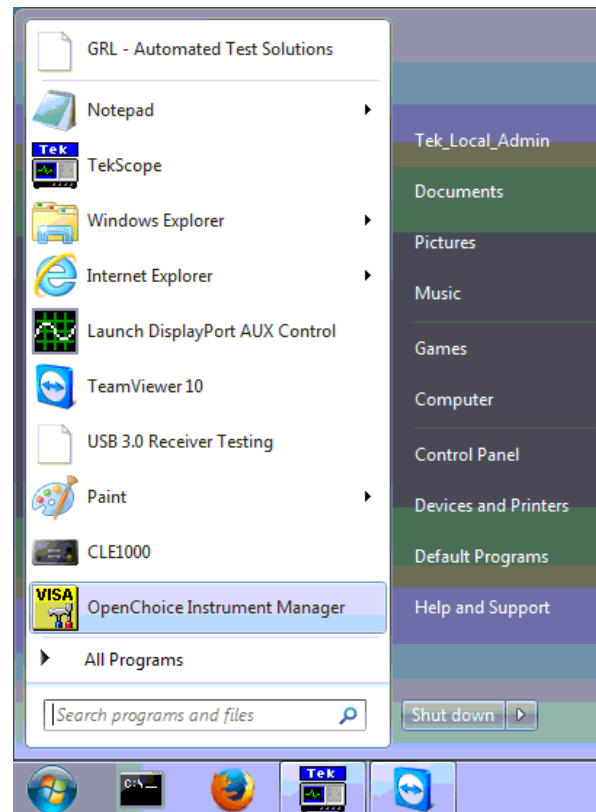


FIGURE 60. OPENCHOICE INSTRUMENT MANAGER IN START MENU

3. The left “Instruments” panel on the OpenChoice Instrument Manager will display all connected instruments. The functional buttons below the “Instruments” panel – “Instrument List Update”, “Search Criteria”, “Instrument Identify” and “Properties” can be used to detect the Scope in case it does not initially appear under “Instruments”.
 - a) “Instrument List Update”: Select to refresh the instrument list and locate new instruments connected to the PC.
 - b) “Search Criteria”: Select to configure the instrument search function.
 - c) “Instrument Identify”: Select to use a supported programming language to send a query to identify the selected instrument.
 - d) “Properties”: Select to display and view the selected instrument properties.

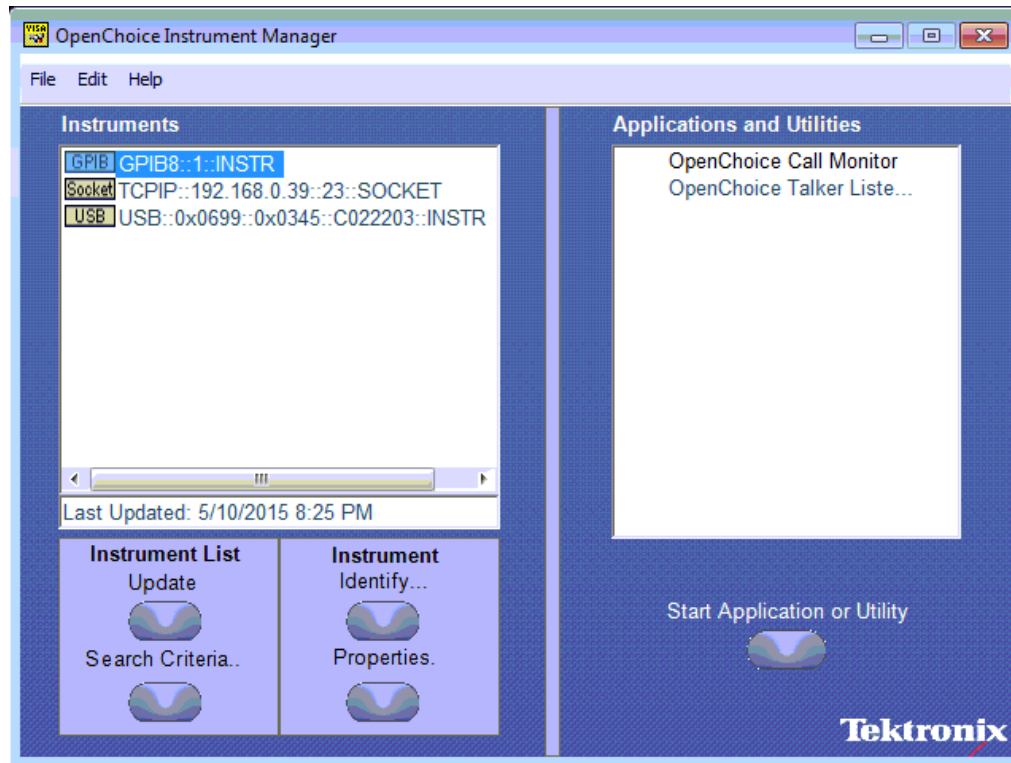


FIGURE 61. OPENCHOICE INSTRUMENT MANAGER MENU

4. If connecting the Tektronix Scope to the PC via USB, select the “Search Criteria” function to ensure that USB connection is enabled, and then select the “Instrument List Update” function. When the Scope appears on the “Instruments” panel, select it and then go to the “Instrument Identify” function. This will display the model and serial number of the Scope once detected. Select the “Properties” function to view the Scope address.
5. If connecting the Tektronix Scope to the PC via LAN, the Scope IP address must be pre-determined beforehand. Then select the “Search Criteria” function to ensure that LAN connection is enabled and type in the Scope IP address. When the Scope shows up in the list, select it followed by “Search”. The Scope should then appear on the “Instruments” panel. Select it and access the “Instrument Identify” function to view the Scope model and serial number as well as the “Properties” function to view the Scope address.
6. On the Equipment Setup page of the GRL-PXE-TX software, type in the Scope address into the ‘Address’ field. If the GRL-PXE-TX software is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example “GPIB8::1::INSTR”. If the GRL-PXE-TX software is installed on the PC to control the Scope, type in the Scope IP address, for example “TCPIP0::192.168.0.110::inst0::INSTR”. Note to **omit** the Port number from the address.

END_OF_DOCUMENT