



GRL Platform Solutions

**Anritsu_GRL-PXE6-CEM-RXA PCI Express Card
Electromechanical (CEM) 6.0 (64 GT/s)
Receiver Compliance Test Automation Solution User
Guide & MOI
Using Anritsu_GRL-PXE6-CEM-RXA Automation Test
Software,
Anritsu MP1900A BERT,
and
High Performance Oscilloscope**



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1 Introduction

This user manual provides information using the Anritsu_GRL-PXE6-CEM-RXA test automation solution to set up and test an electrical receiver (Rx) device to meet PCI Express Card Electromechanical (CEM) 6.0 compliance for 64 GT/s as per PCI Express (PCI-SIG) Standards.

The main body of this documentation first describes how to configure the Anritsu_GRL-PXE6-CEM-RXA test software to calibrate the stressed eye at the receiver of the device under test (DUT) in the PCIe Gen 6.0 system. This includes calibration to be performed at both the physical Test Point 3 (TP3) and the Long Channel at TP2. The Anritsu_GRL software will automate calibration without channel effect at TP3 before measuring the eye opening due to trace length. It also enables running the SigTest and Seasim post processing analysis application to ensure signal quality compliance. The final calibrated eye diagram uses both the SigTest and Seasim software to achieve the final stressed eye calibration.

After completing calibration, the Anritsu_GRL-PXE6-CEM-RXA software will automate compliance testing for the receiver using the First Bit Error Rate (FBER) as a metric. The BERT is used to transmit a modified compliance pattern to the receiver DUT and monitors that the loopback pattern conforms to a First Bit Error Rate (FBER) of less than 10^{-6} . The Anritsu_GRL software also provides an optional SJ margin search test for the DUT.

The Anritsu_GRL-PXE6-CEM-RXA software performs test automation according to PCI-SIG-approved Methods of Implementation (MOI's) with high performance real-time oscilloscopes and Anritsu BERT using existing PCI-SIG Compliance Base Boards (CBB's) and Compliance Load Boards (CLB's). The Anritsu_GRL software is run from the computer or oscilloscope to provide automation control to test the DUT for PCIe CEM 6.0 Rx electrical compliance. When combined with a satisfactory level of interoperability testing, these tests provide a reasonable level of confidence that the DUT's will function properly in most PCIe environments.

Note: For manual test methodology, refer to Appendix of this documentation or PCI-SIG for approved Method of Implementation (MOI's) as technical reference.

2 Resource Requirements

Note: Equipment requirements may vary according to the lab setup and DUT board. Below are the recommended lists of equipment for the typical test setup.

2.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS – SYSTEMS AND ACCESSORIES

System & Accessory	Qty.	Description/Key Spec Requirement
High Performance Real-time Oscilloscope [a]	1	≥ 50 GHz bandwidth [b]
Anritsu MP1900A BERT	1	MP1900A Signal Quality Analyzer, with following modules: • MU181000A/B 12.5 GHz Synthesizer [c] • MU181500B Jitter Modulation Source • MU196020A 64.2G bit/s or 64.2G baud PAM4 Pulse Pattern Generator [d] • MU196040B 58.2G bit/s or 58.2G baud PAM4 Error Detector • MU196060A 32G baud NRZ/PAM4 Re-Driver • MU195050A Noise Generator
PCI-SIG Compliance Base Board (CBB) or PCI-SIG Compliance Load Board (CLB)	1	For add-in cards For host system boards
External PCIe6 Re-Driver	1	J1900A or G0447A High loss back channels (DUT Tx to BERT Rx) may need additional equalization. Required for System DUT testing
ISI Source Generator	1	Compliant Variable ISI channel
Pick-off Tee (J1510A)	2	For connecting scope to CLB/CBB Tx lanes to perform link equalization tests
Terminator	1	J1632A Coaxial Terminator, for termination of unused MU196020A Aux Out connector during link equalization testing
V(m) - K(f) Adapter	2	34VKF50A Coaxial Adapter
Reference Clock Buffer	1	Z2029A PCIe Reference Clock Buffer for add-in cards
External Refclk Source	1	Required for System and Add-In Card DUT testing in the SRIS (independent Refclk) mode

System & Accessory	Qty.	Description/Key Spec Requirement
Computer/PC (laptop or desktop)	1	For automation control Minimum requirements: • Windows 10+ OS • Intel Core i5 processor • 120GB SSD storage • 16GB RAM • Gigabit Ethernet Recommended requirements: • Windows 10+ OS • Intel Core i7+ processor • 200GB SSD storage • 32GB RAM • Gigabit Ethernet

^[a] Oscilloscope with scope software requirements as specified in vendor specific MOI's. For example, when using the Keysight Scope, scope software such as Keysight InfiniiSim / EZ-JIT / Serial Data Analysis / Serial Data Equalization that are required for testing and signal processing must be pre-installed on the Scope. Similarly, the Tektronix Scope shall be used with DPOJET (Jitter and Eye Analysis Tools) software for making measurements.

^[b] Oscilloscope with scope bandwidth as specified in vendor specific MOI's.

^[c] MU181000B Option 02 is required for testing the System Board DUT.

^[d] The Anritsu_GRL-PXE6-CEM-RXA software supports the PAM4 signal with FEC modulation.

TABLE 2. EQUIPMENT REQUIREMENTS – CABLES

Cable ^[a]	Qty.
SMA-to-SMA cable	4
SMA coaxial cables	1 pair
Phase matched K-K coaxial cables	3 pairs
J1792A V-K cable set (to connect between MU196020A and MU195050A)	1
J1917A coaxial semi-rigid cable (to connect between MU196060A clock output and MU196040B clock input)	1
J1932A coaxial skew matched cable pair 0.8m, V connector (to connect between MU196060A data outputs and MU196040B data inputs)	1
J1789A coaxial cable (to connect between G0447A data outputs and MU196060A data inputs)	2
J1627A GND connection cable	1
BNC-to-SMA cable	1

^[a] Based on the standard test configuration. May require more or less cables depending on the DUT type.

2.2 Software Requirements

TABLE 3. SOFTWARE REQUIREMENTS

Software	Description/Source
Anritsu_GRL-PXE6-CEM-RXA	GRL Platform Solutions PCI Express Card Electromechanical 6.0 (64 GT/s) Automated Receiver Calibration and Compliance Test Solution – www.grlps.com
VISA (Virtual Instrument Software Architecture) API Software	VISA Software is required to be installed on the control PC running Anritsu_GRL-PXE6-CEM-RXA software. GRL Platform Solution's software framework has been tested to work with all three versions of VISA available on the Market: 1. NI-VISA: http://www.ni.com/download/ni-visa-17.0/6646/en/ 2. Keysight IO Libraries: www.keysight.com (Search on IO Libraries) 3. Tektronix TekVISA: www.tek.com (Downloads > Software > TekVisa)
MX183000A	Anritsu High-Speed Serial Data Test Software – For loopback FBER testing of the PCIe Gen 6 CEM DUT receiver. This software is located in the MP1900A BERT.
SigTest Application	Standard Post Processing Analysis Software – www.intel.com/content/www/us/en/design/technology/high-speed-io/tools.html
Seasim	Seasim tool for post-process analysis of the captured waveform (Eye Opening simulation software). Seasim is distributed with the Anritsu_GRL-PXE6-CEM-RXA software and is installed during the installation process.

3 Setting Up Anritsu_GRL-PXE6-CEM-RXA Automation Software

This section provides the procedures to start up and pre-configure the Anritsu_GRL-PXE6-CEM-RXA automation software before running tests. It also helps users familiarize themselves with the basic operation of the software.

Note: The Anritsu_GRL software installer will automatically create shortcuts in the Desktop and Start Menu when installing the software.

To start using the Anritsu_GRL software, follow the procedures in the following sections.

3.1 Download Anritsu_GRL-PXE6-CEM-RXA Software

Download and install the Anritsu_GRL software as follows:

1. If the Anritsu_GRL software is to be installed on a PC (where it is referred to as 'control PC'), install VISA (Virtual Instrument Software Architecture) on to the PC where Anritsu_GRL-PXE6-CEM-RXA is to be used (see Section 2.2).
2. Download the software ZIP file package from the GRL Platform Solutions support site.
3. The ZIP file contains:
 - **PCIECEMGen6_AN_PatternFilesInstallationxxxxxxxxSetup.exe** – Run this on the Anritsu MP1900A BERT Signal Quality Analyzer to install the pattern setup files.
 - **PCIECEMGen6_AN_RxTestApplicationxxxxxxxxSetup.exe** – Run this on the PC or on the oscilloscope to install the application.
 - **PCIECEMGen6_AN_RxTestScopeSetupFilesInstallationxxxxxxxxSetup.exe** – Run this on the oscilloscope to install the scope setup files.

3.2 Launch and Set Up Anritsu_GRL-PXE6-CEM-RXA Software

1. Once the Anritsu_GRL software is installed, open the GRL folder from the Windows Start menu. Click on **GRL – Automated Test Solutions** within the GRL folder to launch the Anritsu_GRL software framework.

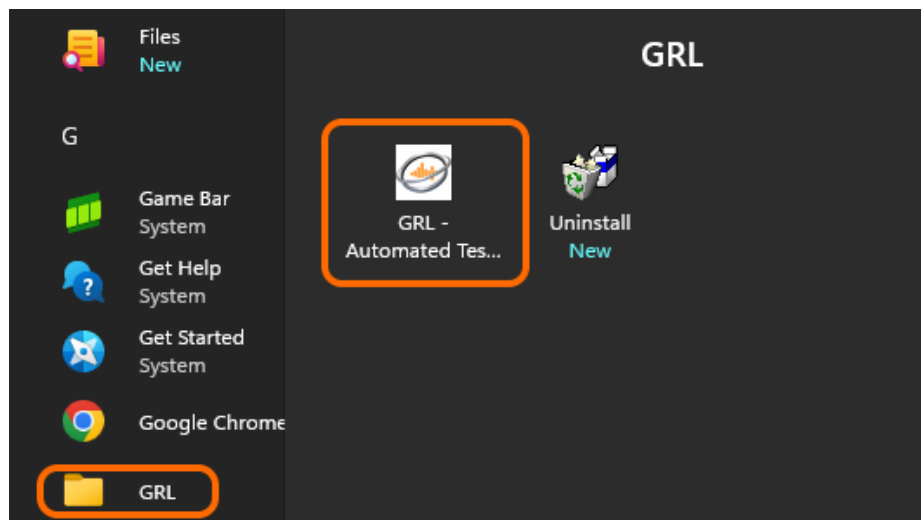


FIGURE 1. SELECT AND LAUNCH ANRITSU_GRL FRAMEWORK

2. From the Application → Rx Test Solution drop-down menu, select 'Anritsu PCIe CEM 6.0 Rx Test' to start the PCIe CEM 6.0 Rx Test Application. If the selection is grayed out, it means that your license has expired.

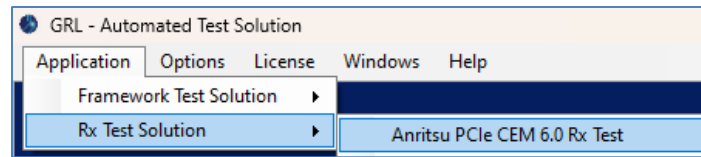


FIGURE 2. START PCIe CEM 6.0 RX TEST APPLICATION

3. To enable license, go to License → License Info.

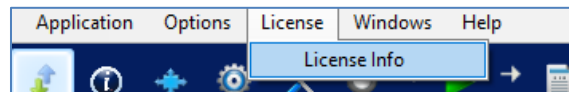


FIGURE 3. SEE LICENSE DETAILS

- a) Check the license status for the installed application.

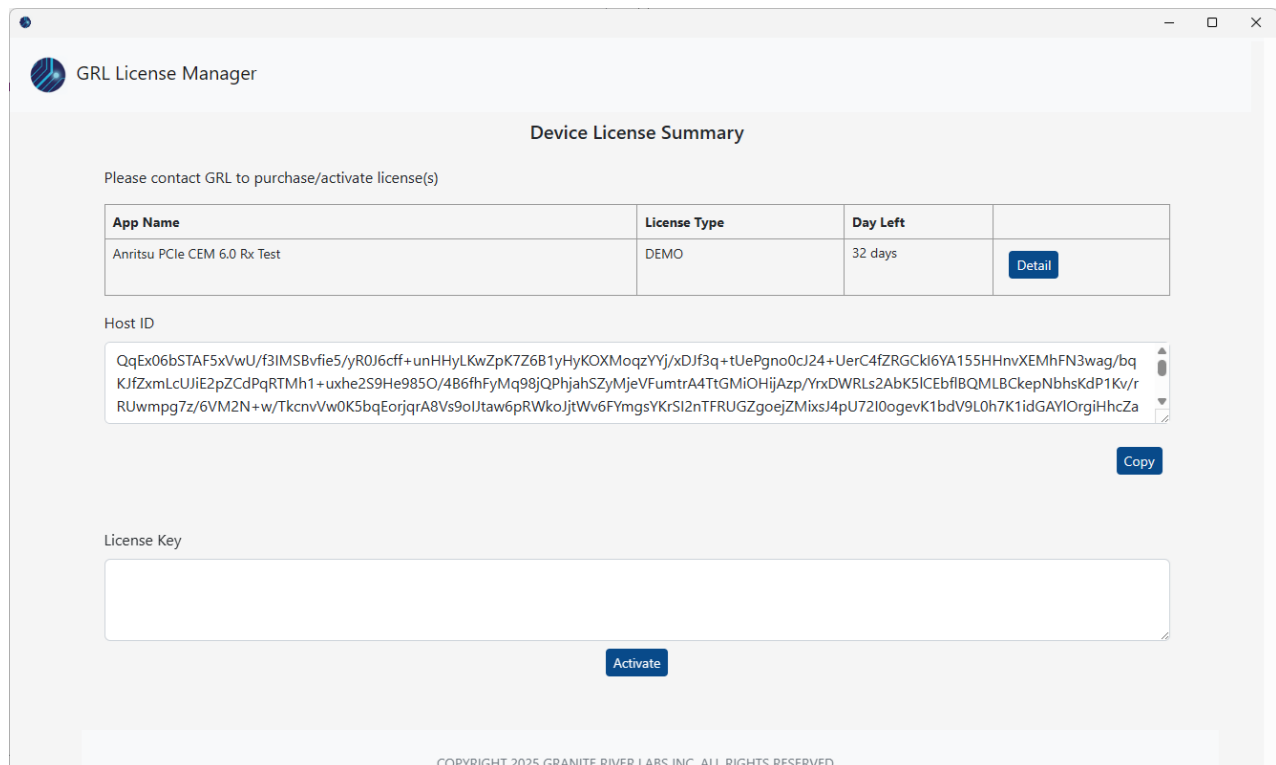


FIGURE 4. CHECK LICENSE FOR INSTALLED APPLICATIONS

- b) Activate a License:

- If you have an Activation Key, enter it in the **License Key** field provided and select **Activate**. The installed application is ready for use upon successful activation.
- If you do not have an Activation Key, close the above window to use a demo version of the application over a free 12-day trial period.

Note: Once the 12-day trial period ends, you will need to request an Activation Key to continue using the application on the same computer by contacting support@grlps.com.

4. Select the Equipment Setup icon  on the PCIe CEM 6.0 Rx Test Application menu.
5. Connect the Anritsu MP1900A BERT via LAN to the Anritsu_GRL automation control enabled Scope or PC. The BERT and MX183000A software can be connected using connection string formats similar to the following examples:

- BERT: “TCPIP0::192.168.0.14::5001::SOCKET” or “192.168.0.14:5001”
- MX183000A: “TCPIP0::192.168.0.14::5000::SOCKET” or “192.168.0.14:5000”

Note the IP addresses listed above are only examples and should be changed according to the actual network connection being used.

6. On the Scope or control PC, obtain the network addresses for all the connected instruments from the device settings. Note these addresses as they will be used to connect the instruments to the Anritsu_GRL automation software.
7. On the Equipment Setup page of the Anritsu_GRL PCIe CEM 6.0 Rx Test Application, type in the address of each connected instrument into the ‘Address’ field.

(Note: If the Anritsu_GRL software is installed on the **Tektronix Scope**, ensure the Scope is connected via GPIB and type in the GPIB network address, for example “GPIB8::1::INSTR”.)

If the Anritsu_GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example “TCPIP0::192.168.0.110::inst0::INSTR”. Note to **omit** the Port number from the address.

(Note: If the Anritsu_GRL software is installed on the **Keysight Scope**, and if there is error in connection, type in the Scope IP address as “TCPIP0::192.168.0.4::5025::SOCKET”.)

8. Then select the “lightning” button () for each connected instrument.

The “lightning” button should turn green () once the software has successfully established connection with each instrument.

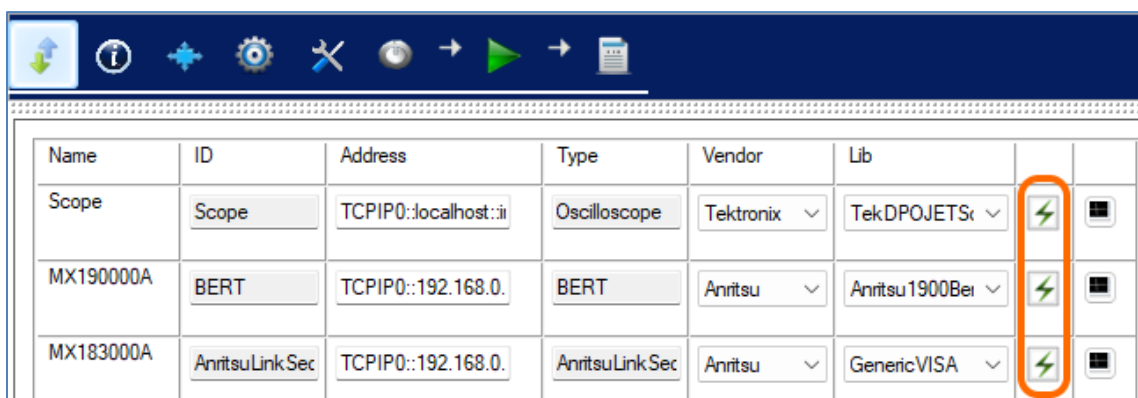


FIGURE 5. CONNECT INSTRUMENTS WITH ANRITSU_GRL SOFTWARE

Note: Additional information for connecting supported vendor oscilloscopes (Keysight and Tektronix) to the PC is provided in the Appendix of this document.

3.2.1 Set Up Remote File Server

1. The **GRLRemoteProxyServer.exe** will also be installed along with the **PCIECEMGen6_AN_RxTestScopeSetupFilesInstallationxxxxxxxxSetup.exe** on the Scope. The GRLRemoteProxyServer.exe is installed under the “C:\GRL\GRLRemoteProxyServer” directory.

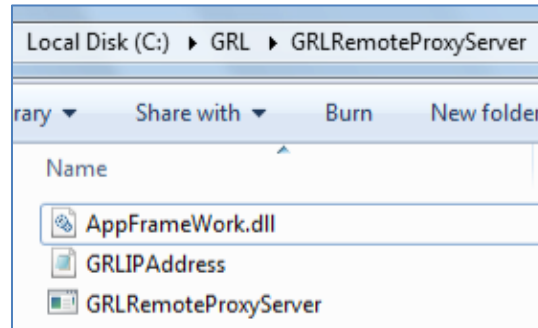


FIGURE 6. INSTALLED GRLREMOTEPROXYSERVER.EXE FILE DIRECTORY

2. If the Anritsu_GRL software is installed on the PC to control the Scope and SigTest is selected as the test method to be used (refer Section 4.7), the GRLRemoteProxyServer.exe must be run on the Scope to move large waveform files back to the control PC. The Anritsu_GRL software will then perform post-processing and analysis of these waveforms using SigTest.
3. When running the GRLRemoteProxyServer.exe, make sure that the control PC and Scope are connected to the same network, using IP addresses as in following example:
 - Control PC IP address: 192.168.100.8
 - Scope IP address: 192.168.100.35

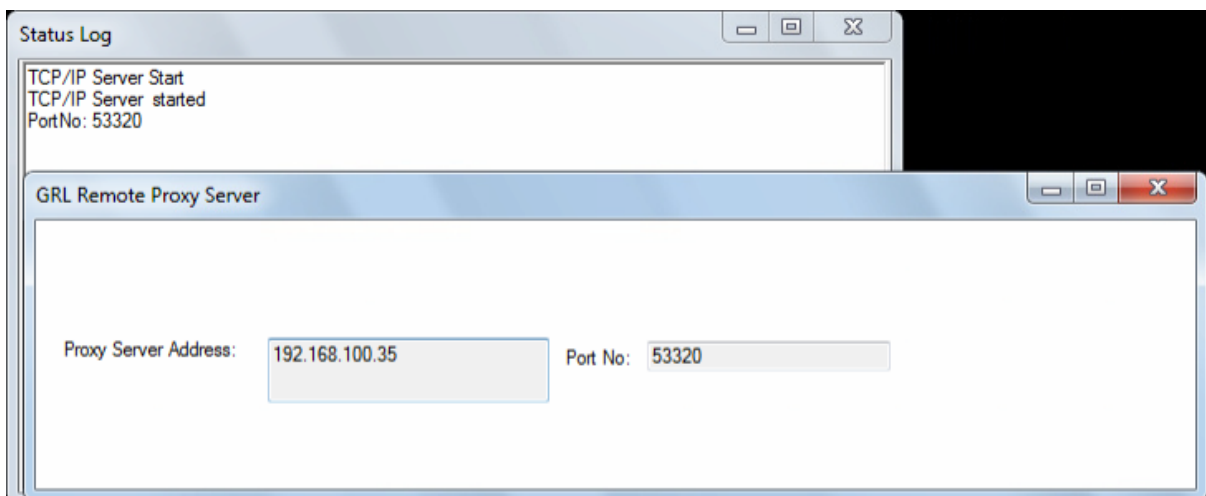


FIGURE 7. VERIFY PROXY SERVER CONNECTION FOR CONTROL PC AND SCOPE

4. On the Anritsu_GRL PCIe CEM 6.0 Rx Test Application, configure the “Remote Proxy IP” and “Remote Proxy Port” parameters on the Configurations  page to match the network settings of the GRL Remote Proxy Server as shown in the example below:

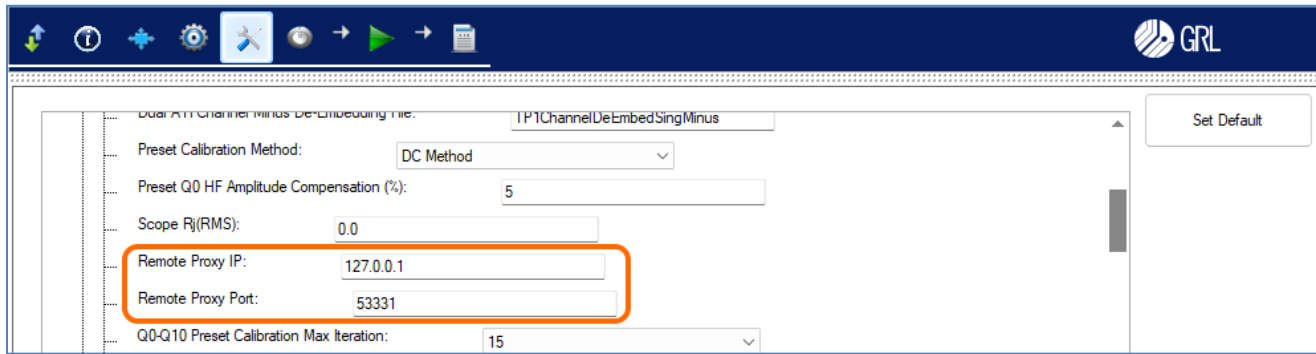


FIGURE 8. CONFIGURE GRL REMOTE PROXY SERVER NETWORK SETTINGS ON ANRITSU_GRL SOFTWARE

Refer Section 4.7 for more details on parameters available on the Configurations page.

3.3 Pre-Configure Software Before Calibration/Testing

Once all equipment is successfully connected from the previous section, proceed to set up the preliminary settings before going to the advanced measurement setup.

3.3.1 Enter Test Session Information

Select  from the menu to access the **Session Info** page. Enter the information as required for the test session that is currently being run. The information provided will be included in the test report generated by the software once tests are completed.

- The fields under **DUT Info** and **Test Info** are defined by the user.
- The **Software Info** field is automatically populated by the software.

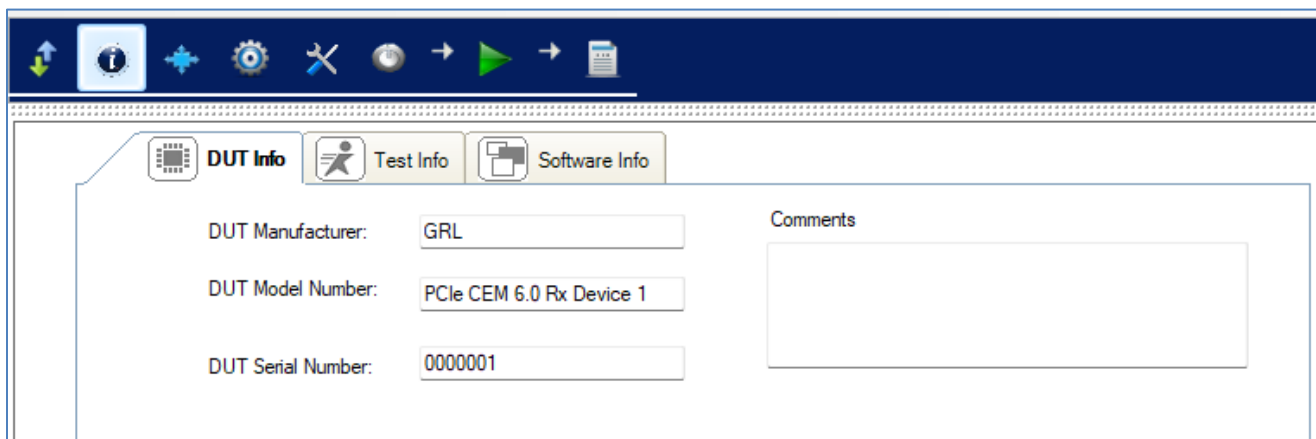


FIGURE 9. SESSION INFO PAGE

4 Calibrating Using Anritsu_GRL-PXE6-CEM-RXA Software

The Anritsu_GRL-PXE6-CEM-RXA test solution supports automated Rx calibration using the SigTest and Seasim signal quality and stress tolerance analysis applications for PCIe Gen 6 system boards and add-in cards. To perform calibration, the Anritsu_GRL-PXE6-CEM-RXA software is run from the PC or oscilloscope to enable automation control for each step of calibration and signal quality test sequence.

Calibration for the PCIe CEM 6.0 electrical specification will basically be performed at two physical test points: TP3 and TP2 (for the Long Channel). Test Point 3 (TP3) is a physical test point for calibration without the effect of a channel. An adjustable CEM connector will be used along with the calibration channel for testing the receiver. This will need to adjust the eye amplitude to specification values when measuring eye height/eye width. TP2 is a physical test point that will affect the eye opening due to trace length.

For the Long Channel TP2 calibration, a PCI-SIG compliance load board (CLB) test fixture will be used for the host system board or a PCI-SIG compliance base board (CBB) test fixture for the add-in card. The board will be connected between the BERT noise generator output and the oscilloscope which will validate the test pattern of the signal and measure for stress tolerance to final stressed eye compliance. Post processing analysis of the signal is performed at the TP2P test point using the Seasim or SigTest application to simulate the stressed eye opening after applying Rx Behavioral package, Rx CTLE and DFE (if required). When calibration is completed, the Anritsu_GRL software will generate a test report detailing all results obtained from the calibration.

4.1 Connection Setup for Scope Intrinsic Noise Measurement (Pre-Calibration)

Pre-calibration will be performed prior to calibration to measure the oscilloscope intrinsic noise.

Figure 10 below shows the setup diagram to measure the intrinsic noise generated by the oscilloscope with no external signal applied. The intrinsic noise waveforms will be captured and saved for SigTest processing in subsequent calibration steps.

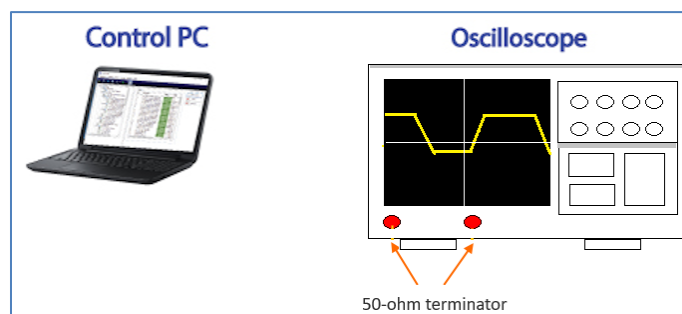


FIGURE 10. SETUP FOR SCOPE INTRINSIC NOISE MEASUREMENT

Connection Step:

Connect 50-ohm terminators to the oscilloscope channels.

4.1.1 Connection Setup with Tektronix ATI Based Oscilloscope

If the Tektronix ATI based oscilloscope is being used, proceed with the following scope intrinsic noise measurement setup.

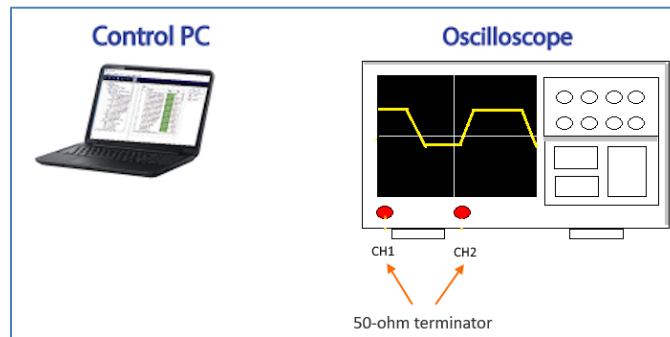


FIGURE 11. SETUP FOR SCOPE INTRINSIC NOISE MEASUREMENT USING TEKTRONIX ATI SCOPE

Connection Step:

Connect 50-ohm terminators to the Tektronix ATI based oscilloscope channels 1 and 2.

4.2 Set Up Automated Rx Calibration for TP3

Once the scope intrinsic noise measurement has been completed, continue with the following calibration setup at TP3 (output of the BERT generator) using a Anritsu_GRL automation control enabled oscilloscope and Anritsu MP1900A BERT.

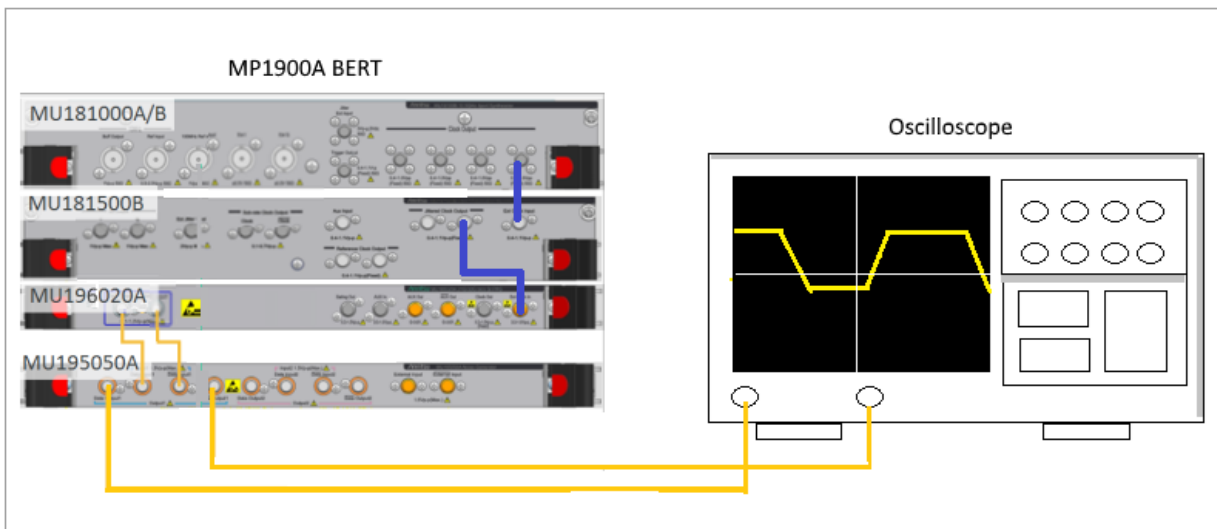


FIGURE 12. RECOMMENDED SETUP FOR TP3 Rx CALIBRATION

1. Using a SMA-SMA short cable, connect the MU181000A/B clock output to the MU181500B Ext clock input.
2. Using a SMA-SMA short cable, connect the MU181500B jittered clock output to the MU196020A Ext clock input.
3. Using coaxial cables, connect the MU196020A data outputs to the MU195050A data inputs.

4. Using phase matched K-K coaxial cables, connect the MU195050A data outputs to the oscilloscope channels.

4.2.1 TP3 Calibration Setup with Tektronix ATI Based Oscilloscope

If the Tektronix ATI based oscilloscope is being used, proceed with the following TP3 calibration setup.

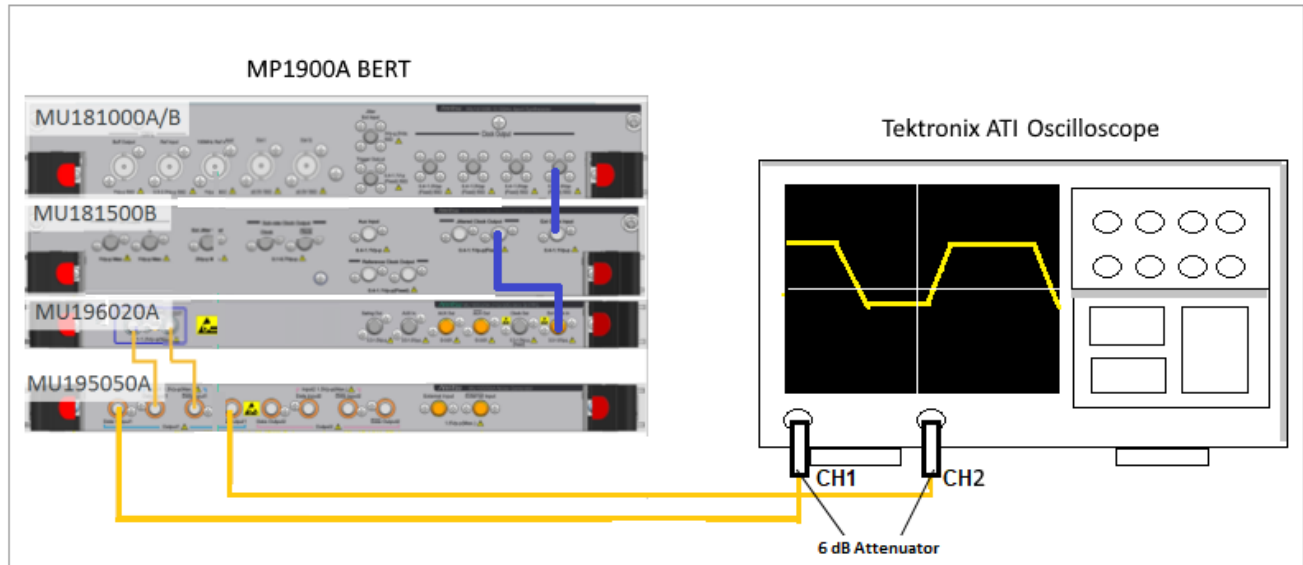


FIGURE 13. RECOMMENDED SETUP FOR TP3 RX CALIBRATION USING TEKTRONIX ATI SCOPE

*Note: Make sure that the “Tektronix Scope Type” is set to **Dual ATI** in the Configurations page (see Section 4.7).*

1. Follow back the same connections from step 1 to 3 in Section 4.2 above.
2. Then using phase matched K-K coaxial cables, connect the MU195050A data outputs to Channels 1 and 2 on the Tektronix ATI based oscilloscope through 6 dB attenuators.

4.3 Set Up Automated Rx Calibration for TP2

The next step is to calibrate the TP3-TP2 Channel (output of the Long Channel) with the following calibration setups using a Anritsu_GRL automation control enabled oscilloscope, Anritsu MP1900A BERT, and PCIe Gen 6 System Board or Add-In Card test fixtures. These calibration setups should also comply with insertion loss limits of 30 to 33 dB.

4.3.1 Connect Equipment for System Board Calibration

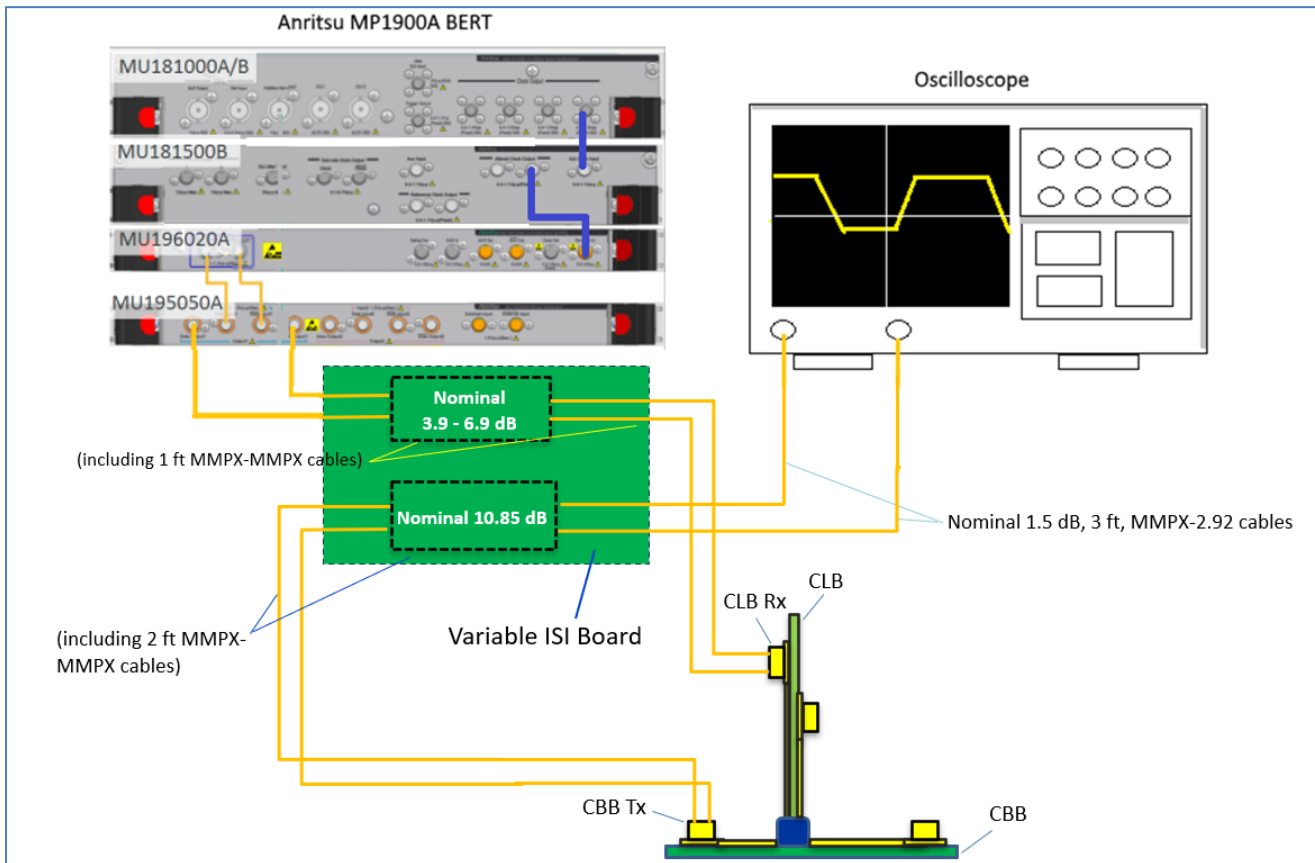


FIGURE 14. RECOMMENDED SETUP FOR TP2 LONG CHANNEL RX CALIBRATION (PCIe GEN 6 SYSTEM BOARD)

1. Using back the same BERT connections from the TP3 calibration, disconnect the MU195050A data outputs from the oscilloscope channels.
2. Connect the MU195050A data outputs to a Variable ISI board (Nominal 3.9 – 6.9 dB trace, including 1 ft MMPX-MMPX cables) and the CLB Rx Lane.
3. Connect the CBB Tx Lane to the Nominal 10.85 dB trace (including 2 ft MMPX-MMPX cables) on the Variable ISI board.
4. Using Nominal 1.5 dB, 3 ft, MMPX-2.92 cables, connect the Nominal 10.85 dB trace to the oscilloscope channels.

4.3.1.1 System Board Calibration Setup with Tektronix ATI Based Oscilloscope

If the Tektronix ATI based oscilloscope is being used, proceed with the following system board calibration setup.

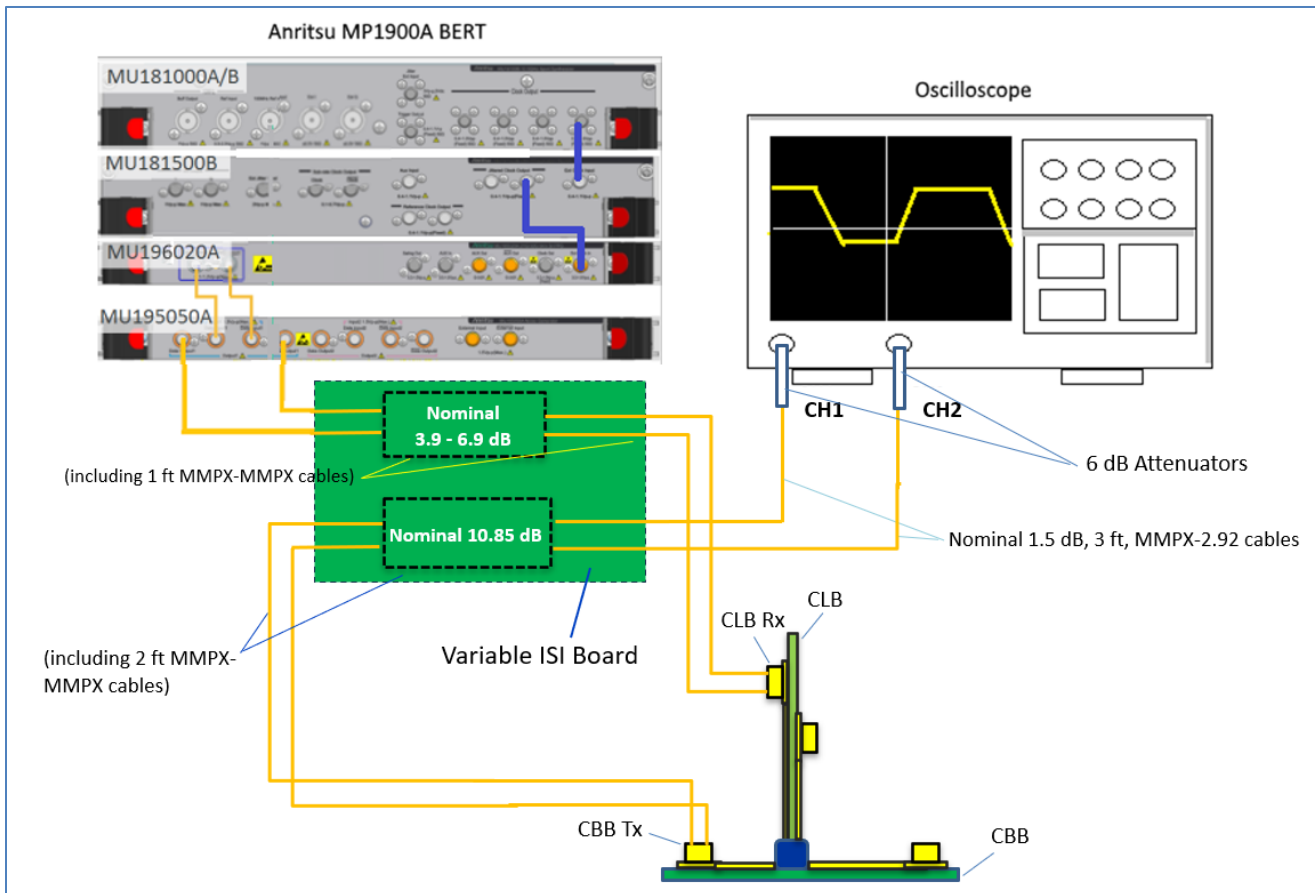


FIGURE 15. RECOMMENDED SETUP FOR TP2 LONG CHANNEL RX CALIBRATION (PCIe GEN 6 SYSTEM BOARD) USING TEKTRONIX ATI SCOPE

*Note: Make sure that the “Tektronix Scope Type” is set to **Dual ATI** in the Configurations page (see Section 4.7).*

1. Follow back the same connections from steps 1 to 4 in Section 4.3.1 above.
2. Then using Nominal 1.5 dB, 3 ft, MMPX-2.92 cables, connect the Nominal 10.85 dB trace to Channels 1 and 2 on the Tektronix ATI based oscilloscope through 6 dB attenuators.

4.3.2 Connect Equipment for Add-In Card Calibration

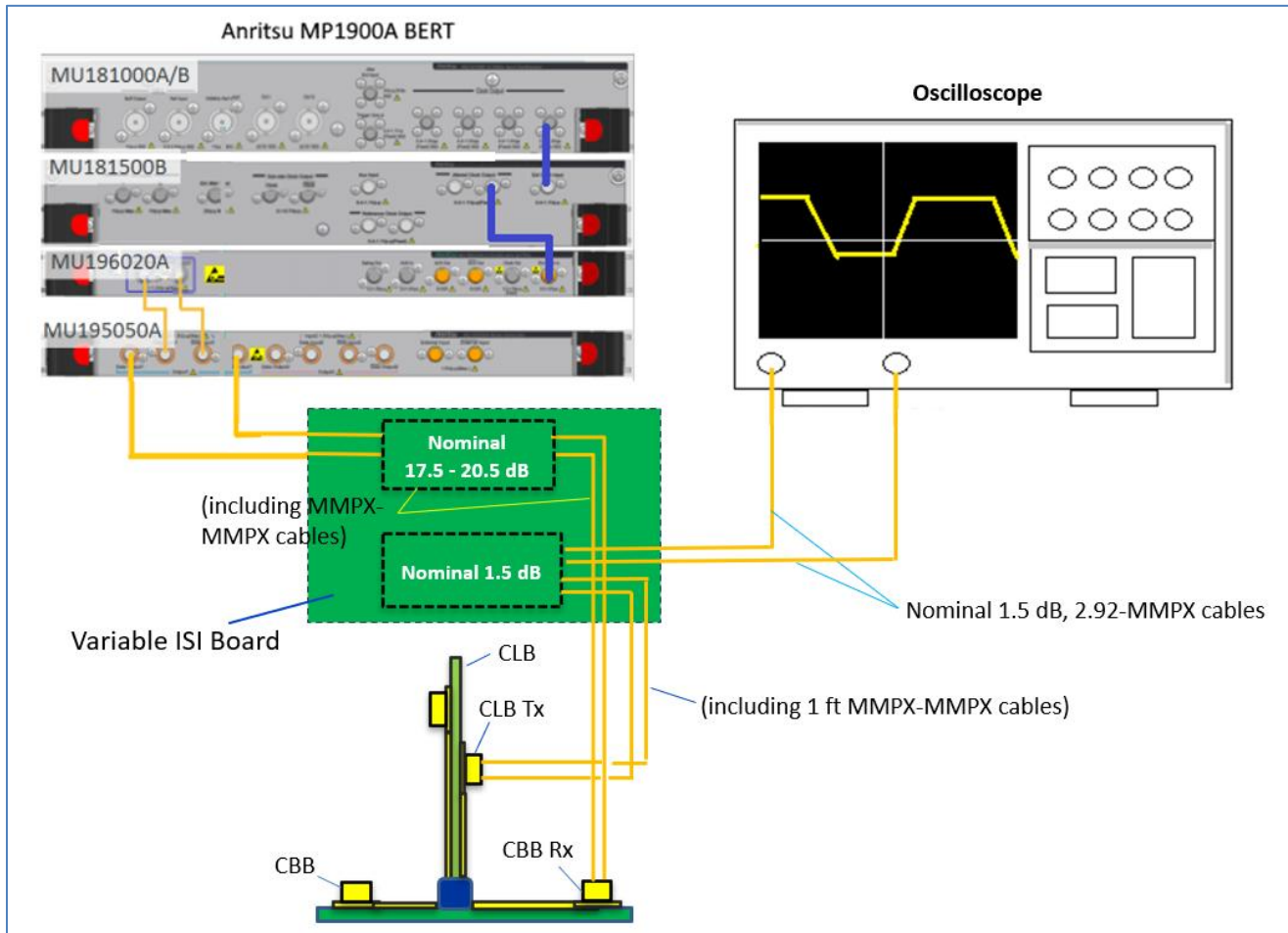


FIGURE 16. RECOMMENDED SETUP FOR TP2 LONG CHANNEL RX CALIBRATION (PCIe GEN 6 ADD-IN CARD)

1. Using back the same BERT connections from the TP3 calibration, disconnect the MU195050A data outputs from the oscilloscope channels.
2. Connect the MU195050A data outputs to a Variable ISI board (Nominal 17.5 – 20.5 dB trace, including MMPX-MMPX cables) and the CBB Rx Lane.
3. Connect the CLB Tx Lane to the Nominal 1.5 dB trace (including 1 ft MMPX-MMPX cables) on the Variable ISI board.
4. Using Nominal 1.5 dB, 2.92-MMPX cables, connect the Nominal 1.5 dB trace to the oscilloscope channels.

4.3.2.1 Add-In Card Calibration Setup with Tektronix ATI Based Oscilloscope

If the Tektronix ATI based oscilloscope is being used, proceed with the following add-in card calibration setup.

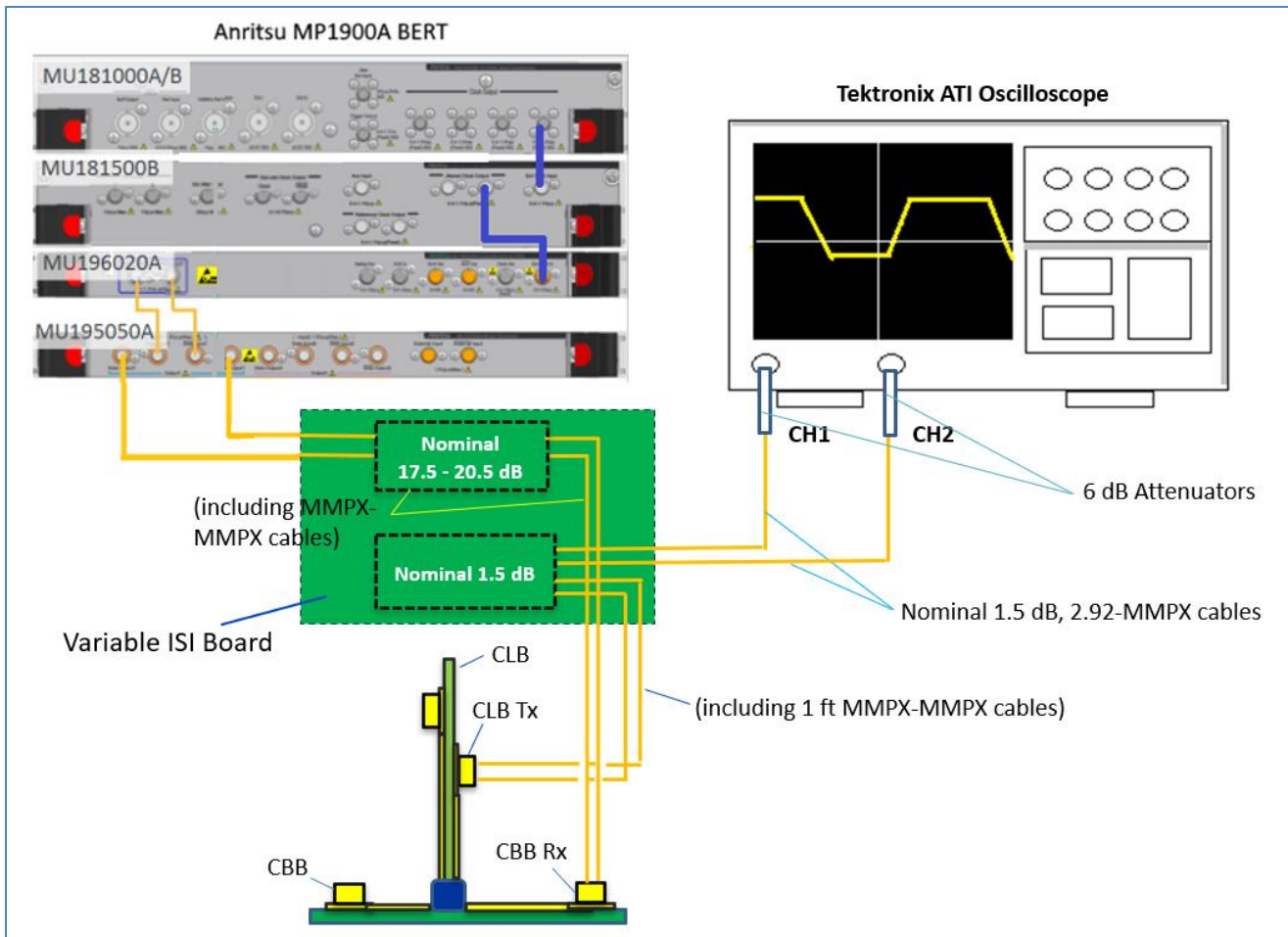


FIGURE 17. RECOMMENDED SETUP FOR TP2 LONG CHANNEL RX CALIBRATION (PCIe GEN 6 ADD-IN CARD) USING TEKTRONIX ATI SCOPE

*Note: Make sure that the “Tektronix Scope Type” is set to **Dual ATI** in the Configurations page (see Section 4.7).*

1. Follow back the same connections from steps 1 to 4 in Section 4.3.2 above.
2. Then using Nominal 1.5 dB, 2.92-MMPX cables, connect the Nominal 1.5 dB trace to Channels 1 and 2 on the Tektronix ATI based oscilloscope through 6 dB attenuators.

4.4 Set Measurement Conditions

Select  from the Anritsu_GRL PCIe CEM 6.0 Rx Test Application menu to access the **Conditions** page to set the conditions for calibration and testing. The Anritsu_GRL software will perform calibration and testing for selected defined SJ frequencies.

Recommended procedure:

- *Step 1:* When calibrating, select all conditions that may be used for testing, and perform the calibration.
- *Step 2:* Once calibration is completed and ready for testing, re-select the necessary test conditions. For example, if required to test for a single SJ frequency, then select only the required SJ frequency for testing.

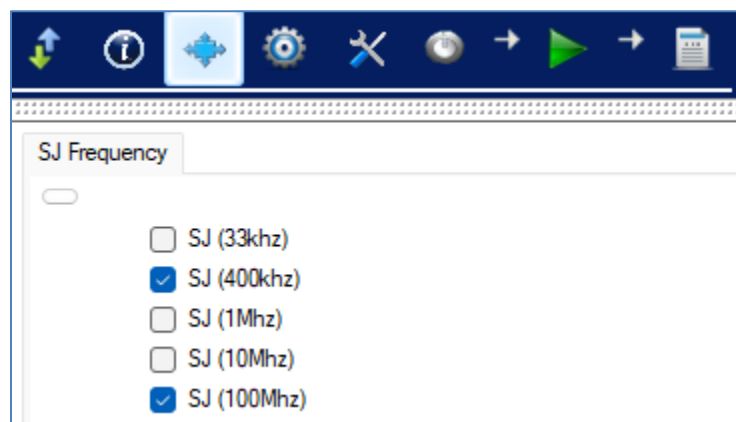


FIGURE 18. SELECT TEST CONDITION

4.5 Set Up Calibration Requirements

After setting up the physical equipment, select  from the Anritsu_GRL PCIe CEM 6.0 Rx Test Application menu to access the Setup Configuration page.



FIGURE 19. SET UP CALIBRATION REQUIREMENTS

4.5.1 Setup Tab

Select to use a compliant PCIe System Board or Add-In Card as the calibration device.

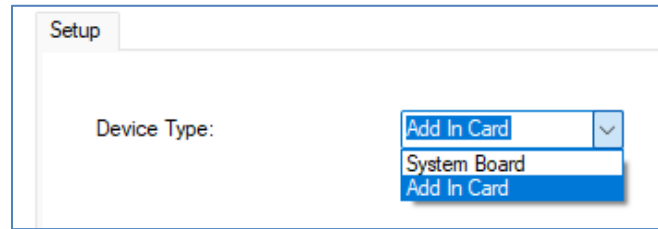


FIGURE 20. SELECT DEVICE FOR CALIBRATION

4.6 Select PCIe CEM 6.0 Rx Calibration

After selecting the device to be calibrated, access the **Select Tests** page on the left of the screen to select the available PCIe CEM 6.0 based receiver calibration to be performed. Select the check box(s) of the desired Rx calibration.

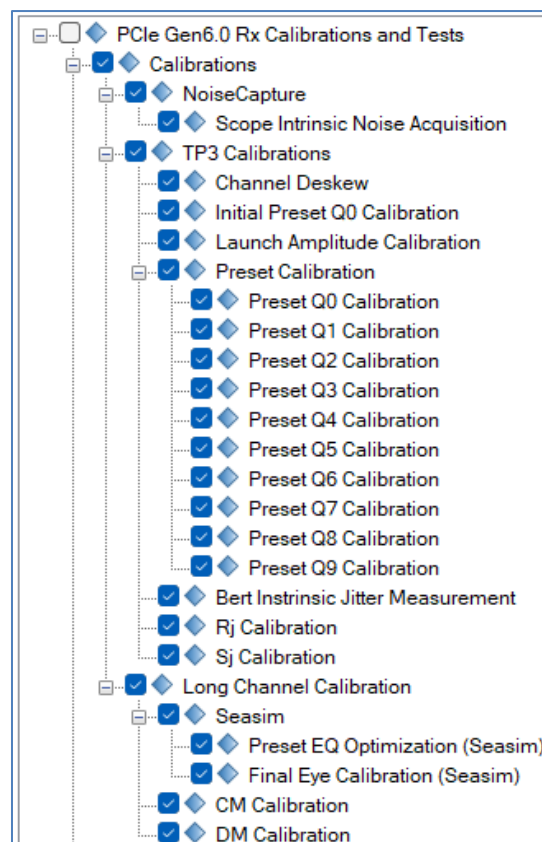


FIGURE 21. SELECT RX CALIBRATION

4.6.1 Select to Perform Noise Capture Verification

Under 'NoiseCapture', select to measure the oscilloscope intrinsic noise. The Anritsu_GRL software will automatically run the intrinsic noise waveform acquisition when initiated.

4.6.2 Select to Perform TP3 Calibration

Under 'TP3 Calibrations', select to calibrate for channel deskew, initial Tx equalization preset, launch amplitude, preset Q0 to Q9, BERT intrinsic jitter, random jitter (RJ) and sinusoidal jitter (SJ) (for PCIe Gen 6 frequencies as per PCIe CEM 6.0 Rx specs and forms a linear curve fit for each SJ frequency).

The Anritsu_GRL software will automatically run the selected calibration when initiated.

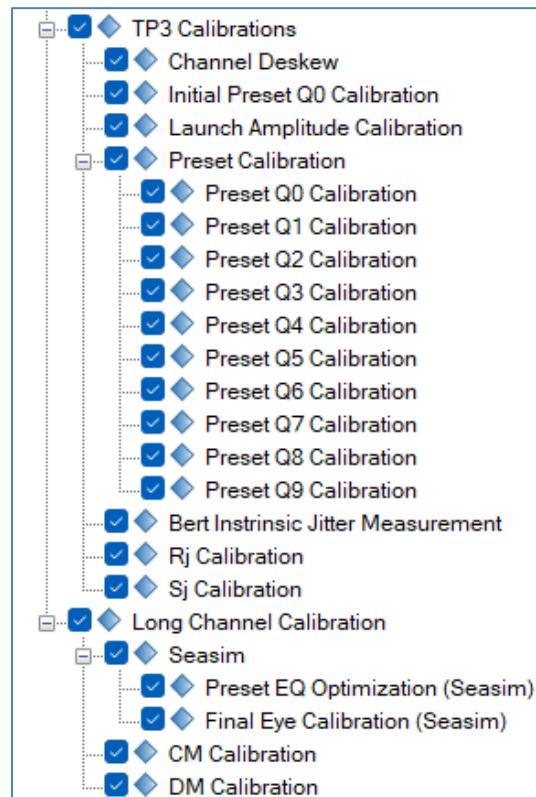


FIGURE 22. SELECT TP3 CALIBRATION

4.6.3 Select to Perform Long Channel TP2 Calibration

Under 'Long Channel Calibration', select to calibrate for Seasim preset equalization optimization & eye calibration parameters along with differential mode (DM) and common mode (CM) to achieve calibrated eye height and width to produce a final stressed eye diagram.

The Anritsu_GRL software will automatically run the selected calibration when initiated.

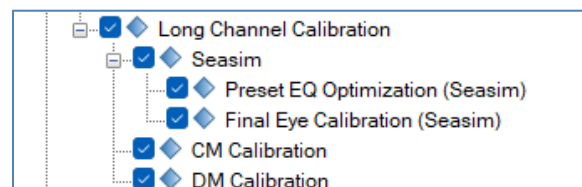


FIGURE 23. SELECT LONG CHANNEL TP2 CALIBRATION

4.7 Configure Calibration Parameters

After selecting the desired calibration, select  from the menu to access the Configurations page. Set the required parameters for calibration as described below.

To return all parameters to their default values, select the 'Set Default' button.

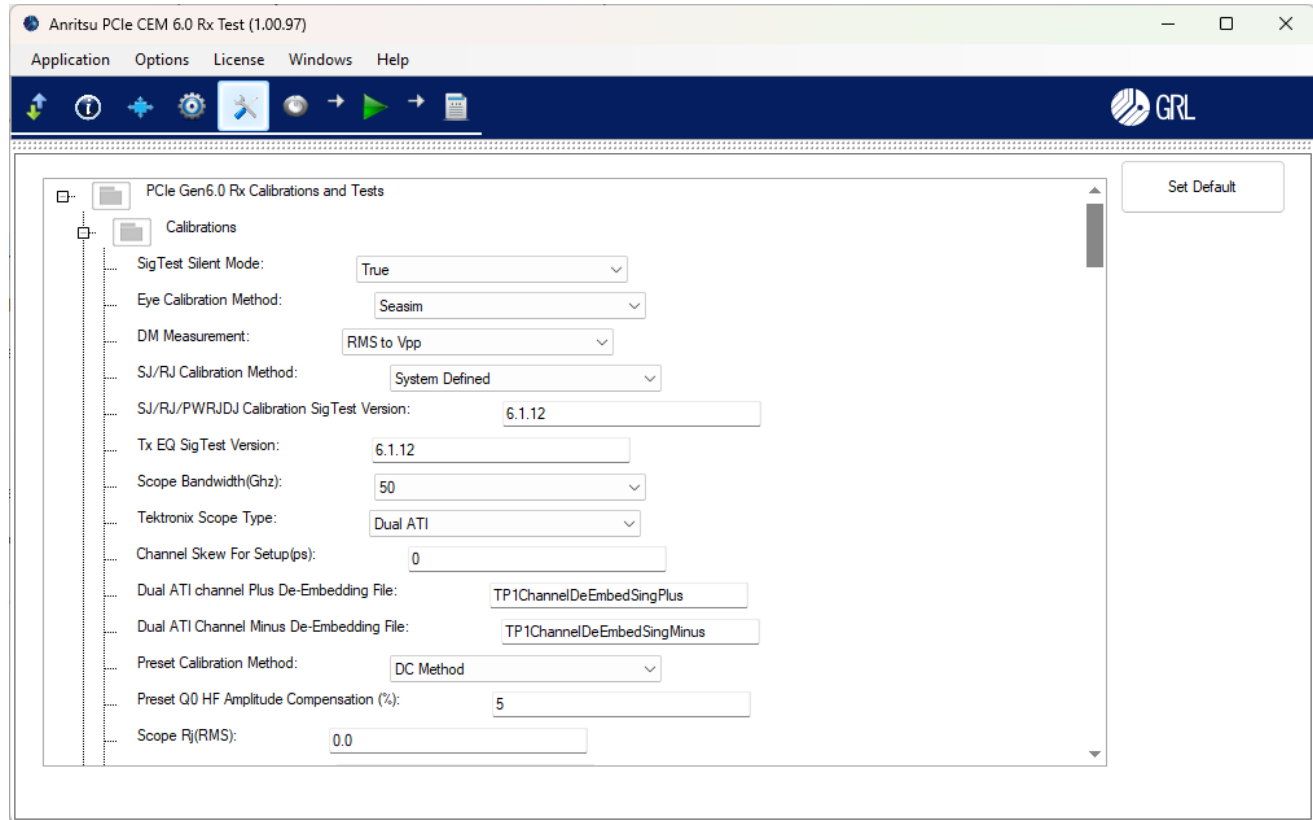


FIGURE 24. CALIBRATION PARAMETERS CONFIGURATION PAGE

TABLE 4. CALIBRATION PARAMETERS DESCRIPTION

Parameter	Description
SigTest Silent Mode	Select 'True' to enable running the SigTest in silent mode during calibration.
Eye Calibration Method	The Seasim application will be used for the final stressed eye calibration and post processing signal quality testing. Make sure that the Seasim application is already installed in the test controller system.
DM Measurement	Select the unit for measuring differential mode (DM).
SJ/RJ Calibration Method	"System Defined" will be used as the default method; otherwise select the "Vendor Specific" method to be used for the SJ or RJ calibration.

SJ/RJ/PWRJ/DJ Calibration SigTest Version	If the SigTest method is to be used during jitter calibration, enter the Version number of the SigTest to be used. Make sure that the SigTest application is already installed in the test controller system.
Tx EQ SigTest Version	If the SigTest method is to be used during Tx equalization, enter the Version number of the SigTest to be used. Make sure that the SigTest application is already installed in the test controller system.
Scope Bandwidth (GHz)	Select the appropriate bandwidth of the Scope being used for measurements.
Tektronix Scope Type	If the Tektronix Scope is to be used for measurements, select either the Single-shot based Scope or the Tektronix' owned Dual Asynchronous Time Interleaving (Dual ATI) based Scope.
Channel Skew For Setup (ps)	Enter the channel skew or timing to perform alignment of the Scope channels.
Dual ATI Channel Plus / Minus De-Embedding File	If the Tektronix ATI based Scope is to be used for measurements, specify the file name for de-embedding on the respective Scope channel.
Preset Calibration Method	Select the "DC Method" to be used for preset calibration.
Preset Q0 HF Amplitude Compensation (%)	Set the Preset Q0 high frequency amplitude loss compensation in percentage.
Scope Rj (ps RMS)	Set the random jitter (RJ) of the Scope in ps RMS.
Remote Proxy IP	Enter the IP address for the GRL Remote Proxy Server. See Section 3.2.1 on how to set up the remote file server.
Remote Proxy Port	Enter the Port number for the GRL Remote Proxy Server. See Section 3.2.1 on how to set up the remote file server.
Q0-Q10 Preset Calibration Max Iteration	Select the maximum number of runs or iterations to perform the Preset Q0 to Q10 calibration.
Q0-Q10 Preset Calibration Limit	Select the threshold limit value for the Preset Q0 to Q10 calibration.
SJ/RJ Calibration No of UI	Set the number of unit interval (UI) samples to acquire for the SJ or RJ calibration.
Opposite Emphasis Measurement by Median	Select 'True' to enable the median to be used as reference for the inverse emphasis measurement.
Feedback Gain Order	Select the CTLE gain value adjustment in controlled steps or variable mode to determine the lowest CTLE gain value that gives zero errors.

Preset Non Transition Region	Select the preset equalization setting during the stable operational 64 GT/s state of the link.
Launch Amplitude Cal Min Limit	Set the minimum limit value for the launch amplitude calibration.
Use Amplitude Feedback	Select 'True' to enable amplitude feedback via the link equalization training where the receiver will provide feedback to the transmitter for signal quality optimization.
Amplitude Feedback Limit (%)	If 'Use Amplitude Feedback' is set to 'True', select the allowable limit for the amplitude feedback.
Negative DeEmphasis Method	Select the method to emulate the effects of channel losses via negative de-emphasis to create high-frequency losses in the generated signal.
Preset Amplitude Trigger Setting	Select the "Auto" or "Custom" (user-defined) trigger method for preset amplitude.
Preset Amplitude Trigger Level (mV)	If "Custom" is selected as the trigger method for preset amplitude, enter the value for the trigger level.
Use Fast Autoscale	Select 'True' to enable fast autoscaling for TP3 calibration.
TP2 Scope Bandwidth (GHz)	Select the bandwidth of the Scope to be used for TP2 measurements.
Custom Final ISI Trace	Select 'True' to enable generating custom ISI trace for the final ISI calibration.
Apply Embedding	Select 'True' to embed the add-in card or system board DUT for calibration.
Add-In Card / System Embed File	Specify the file name for the embedded add-in card or system board.
Minimum & Maximum Preset for Eye Calibration	Select the range of presets to be applied for stressed eye calibration.
Preset to Exclude	Specify the preset that is not used for calibration.
CTLE Scan Start & End EQ Gain (dB)	Select the optimized CTLE Equalization Gain setting index to be used based on the CTLE model to measure the Eye area.
Use Real Edge	Select 'True' to use Real Edge connection for test setup on the Oscilloscope. <i>Note: This setting is only applicable for the Keysight Scope.</i>
Eye Width & Eye Height Min / Max Limit	Enter the limits for maximum and minimum eye calibration values.
DM Maximum / Minimum Limit	Enter the maximum and minimum limits for DM.

Final Preset	Select the optimal preset which gives the largest eye area or from the range of presets to be applied for the final calibrated eye.
Preset Scan Method on Subsequent Channel Loss	Select the method that allows the preset scan to adjust equalization/preset to compensate for channel loss.
Eye Opening Check Before Proceed Final Eye	Select to perform the eye opening pre-check at the minimum specs limit or 10% below the minimum specs limit. Otherwise, select “None” to skip this procedure.
Seasim Configuration:	
Final Eye Amplitude Cal On First Pass	Select ‘True’ to enable calibration for final eye amplitude to be performed upon the first successful calibration run.
Intrinsic Noise	Set the intrinsic noise/jitter (if required) to be used in the Seasim calculation.
Auto Measure PWJ Jitter	Select ‘True’ to enable auto measurement of the PWJ (pulse width) jitter.
PW RJ & PW DDJ	Enter the pulse width random jitter or deterministic jitter.
Seasim Version	Select the Seasim version to be used.
nUI Count	Enter the number of nUI to be captured.
Step Response Average	Enter the averaged step response value for converting saved waveforms to Seasim-compatible waveforms.
Pause on Each Cycle to Enter Value	Select ‘True’ to enable processing to be paused after every Seasim operation to enter the required value.
Start ISI	Select the ISI traces (dB) to start with when running Seasim.
Step Response Acquisition Count	Select the number of step responses to acquire when running Seasim.
Capture Response Only	Select ‘True’ to acquire only step responses when running Seasim.
DM Step Resolution	Select the step size value for DM measurements.
Enable BT Filter	Select “True” to enable the Bessel-Thomson filter on the scope.
Seasim SJ Sweep (mUI)	Select the SJ scan range or amplitude for Seasim measurements.
Parallel Seasim Process	Select “True” to simultaneously run multiple threads of Seasim processing and plot the results.
SJ Sweep Resolution (UI)	Set the resolution of the SJ varied at different frequencies within a specified range in UI.

4.8 Configure Calibration Target Values

For debugging purposes ONLY, the default calibration target values can be changed for the RJ, SJ, DM and CM calibration. To do this, select  from the menu to access the Calibration page.

By default, the calibration target values are those defined in the specification. To change the values, un-select the 'Use Default Value' checkbox. In case the default values are required again, just select the checkbox to allow all existing values to be reset to default.

Note: The PID Control setting is used to adjust the step width for steps calculation if the target measurement cannot be met with the current step. To adjust, use a lower PID Control value to reduce the subsequent step or increase the control value to make the subsequent step bigger.

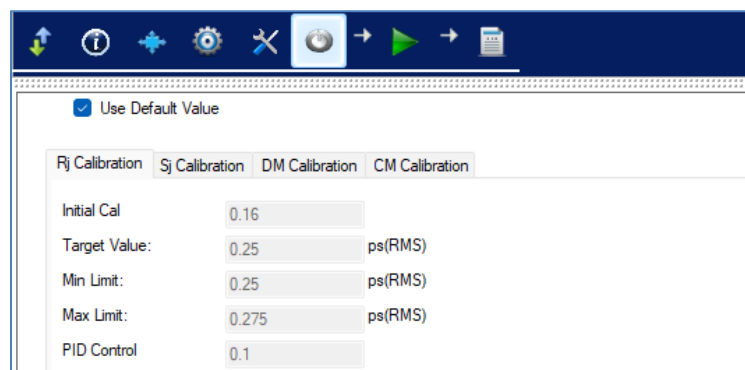


FIGURE 25. CALIBRATION TARGET OVERWRITE PAGE

4.9 Run Automation Calibration

Once calibration have been selected and set up from the previous sections, the calibration are now ready to be run.

Select  from the menu to access the Run Tests page. The Anritsu_GRL-PXE6-CEM-RXA software automatically runs the selected calibration when initiated.

Before running the calibration, select the option to:

- **Skip Test if Result Exists** – If results from previous calibration exist, the software will *skip* those calibration.
- **Replace if Result Exists** – If results from previous calibration exist, the software will *replace* those calibration with new results.

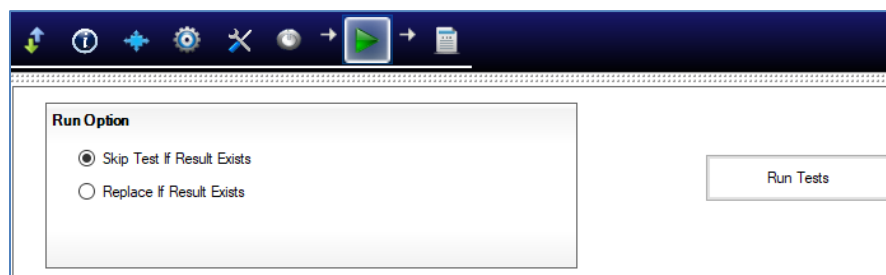


FIGURE 26. RUN TESTS PAGE

Select the **Run Tests** button to start running the selected calibration. The connection diagram for the calibration being run will initially appear to allow the user to make sure that the calibration environment has been properly set up before calibration can proceed. Below shows an example of the connection diagram pop-up for the system board Rx TP3 calibration.

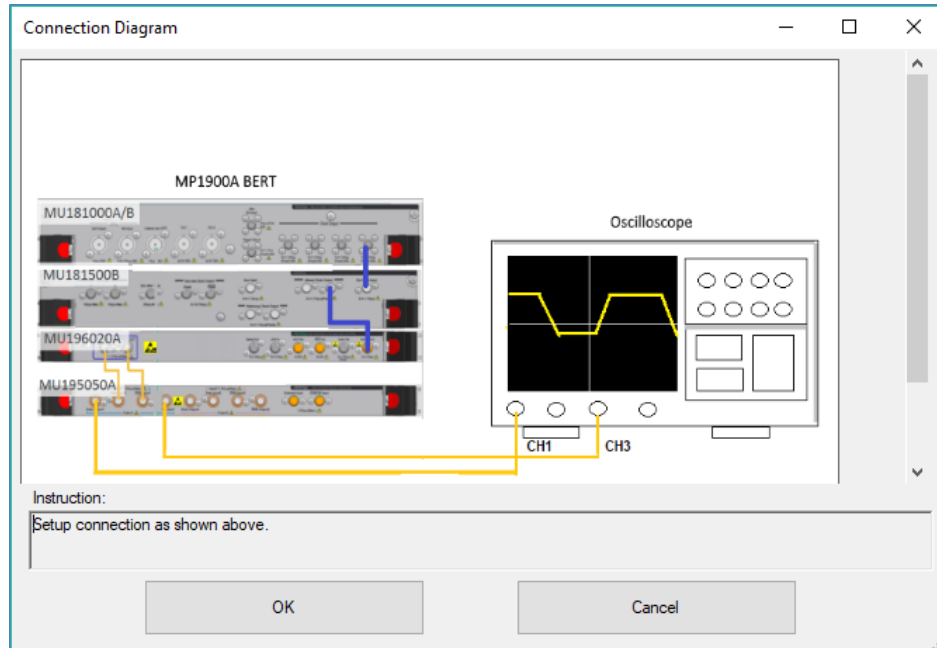


FIGURE 27. EXAMPLE CONNECTION POP-UP DIAGRAM FOR RX TP3 CALIBRATION

5 Testing Using Anritsu_GRL-PXE6-CEM-RXA Software

The Anritsu_GRL-PXE6-CEM-RXA test solution supports automated Rx compliance testing as well as optional SJ margin search testing for the PCIe Gen 6 system board and add-in card DUT's. Rx compliance testing includes Tx preset test, initial Tx equalization test, Tx link equalization response test, and Rx link equalization test performed at 64.0 GT/s. The Anritsu_GRL software will initially run through link training with the DUT to prepare it for Loopback mode. Once the DUT is ready for next transition state, the software will start to initiate loopback on the DUT and then measure the First Bit Error Ratio (FBER) using the calibration stressed signals. The Rx path is tested with worst case eye to ensure a FBER of less than $1E-6$ can be achieved.

When testing is completed, the Anritsu_GRL software will generate a test report detailing all results obtained from the test runs.

5.1 Overview of DUT Tx Preset Test

The PCIe Gen 6 system board or add-in card DUT will be tested for Tx preset compliance as defined by the PHY Test Specification at 64.0 GT/s. This will first ensure the DUT is able to generate the correct Tx equalization values for each of the total 11 presets before being tested for Tx equalization.

Note: This test requires the DUT to be in the polling.compliance state. No Variable ISI channel will be used in the setup.

5.1.1 System Board Tx Preset Test at 64.0 GT/s

The test setup should be based on the following:

- Attach the calibration revision 6.0 (for 64.0 GT/s) CLB to the system board DUT with no power applied.
- Connect the compliance toggle outputs on the CLB to the Rx lane 0 on the CLB.
- Connect the Tx lane under test on the CLB to the input of the oscilloscope. Make sure that the scope bandwidth is set to 50 GHz with sampling rate of minimum 6 samples per UI and a 4th order Bessel-Thomson filter with roll-off from DC value by 3 dB at 33 GHz.
- Make sure that the SSC enabled or SSC disabled clock is applied.

Note the setup will NOT include any Variable ISI channel.

Once the system board DUT is powered on, set the CLB compliance toggle to initially place the DUT in the 64 GT/s test state and capture the following:

- 3.0 million unit intervals of data ($3.0 \times 10^6 \times 31.25 \text{ ps} = 93.75 \text{ }\mu\text{s}$)

Save the captured waveform for the initial preset value, using a compliance pattern of 64 ones and 64 zeros. Then, repeat the test for all 11 presets at 64.0 GT/s.

Finally, read the saved waveform files and calculate the preset values using the SigTest Transmitter Preset Test option. The test is considered as successful if all preset values are within their allowable limit range as specified for 64.0 GT/s. Repeat the test for all lanes.

5.1.2 Add-In Card Tx Preset Test at 64.0 GT/s

The test setup should be based on the following:

- Attach the add-in card DUT to the calibration revision 6.0 (for 64.0 GT/s) CBB with no power applied.
- Connect the compliance toggle outputs (MMPX connectors J5 and J85) on the CBB main board to the Rx lane 0 (MMPX connectors J18 and J2) on the CBB.
- Apply 50-ohm terminations on all Tx lanes other than the Tx lane under test.
- Connect the Tx lane under test to the input of the oscilloscope. Make sure that the scope bandwidth is set to 50 GHz with sampling rate of minimum 6 samples per UI and a 4th order Bessel-Thomson filter with roll-off from DC value by 3 dB at 33 GHz.
- Make sure that the CBB is supplying SSC enabled clock (-0.5% down-spread) for this test.

Once the CBB is powered on, set the CBB compliance toggle to initially place the DUT in the 64 GT/s test state and capture the following:

- 3.0 million unit intervals of data ($3.0 \times 10^6 \times 31.25 \text{ ps} = 93.75 \text{ }\mu\text{s}$)

Save the captured waveform for the initial preset value, using a compliance pattern of 64 ones and 64 zeros. Then, repeat the test for all 11 presets at 64.0 GT/s.

Finally, read the saved waveform files and calculate the preset values using the SigTest Transmitter Preset Test option. The test is considered as successful if all preset values are within their allowable limit range as specified for 64.0 GT/s. Repeat the test for all lanes.

5.2 Overview of DUT Initial Tx Equalization Test

Note: This only applies for the add-in card DUT and is not required for the system board DUT.

The PCIe Gen 6 add-in card DUT will be tested for initial Tx equalization as defined by the PHY Test Specification at 64.0 GT/s. This will ensure the DUT is able to use the correct Tx equalization preset as required during the initial stage of testing.

5.2.1 Add-In Card Initial Tx Equalization Test at 64.0 GT/s

The test setup should be based on the following:

- Attach the add-in card DUT to the calibration revision 6.0 (for 64.0 GT/s) CBB with no power applied.
- Connect the Rx lane under test on the CBB to the BERT signal source.
- Connect the 100 MHz reference clock output from the BERT to the clock input on the CBB (with SSC disabled).
- Connect the Tx lane under test on the CBB main board to the input of the BERT error detector.
- Keep additional Tx lanes other than the Tx lane under test unterminated.
- Make sure that the scope bandwidth is set to 50 GHz with sampling rate of minimum 6 samples per UI and a 4th order Bessel-Thomson filter with roll-off from DC value by 3 dB at 33 GHz.

Once the CBB is powered on, the DUT should start link training and negotiation to 64.0 GT/s while requesting Q0 as the initial preset for the DUT. *Note that Tx equalization adjustments will not be required in phase 3. Ensure that the Tx equalization preset for the DUT is maintained when changing to 64.0 GT/s.*

Set the BERT error detector to place the DUT in the loopback state and capture the following:

- 3.0 million unit intervals of data ($3.0 \times 10^6 \times 31.25 \text{ ps} = 93.75 \text{ }\mu\text{s}$)

Save the captured waveform for preset Q0. Then, repeat the test with presets from Q1 to Q9 at 64.0 GT/s.

Finally, read the saved waveform files and calculate the preset values using the SigTest Transmitter Preset Test option. The test is considered as successful if all preset values are within their allowable limit range as specified for 64.0 GT/s.

5.3 Overview of DUT Tx Link Equalization Response Test

The PCIe Gen 6 system board or add-in card DUT will be tested for Tx link equalization response as defined by the PHY Test Specification at 64.0 GT/s. This will ensure the DUT can accurately respond to commands to adjust the transmitter equalization values during link training for DUT loopback.

5.3.1 System Board Tx Link Equalization Response Test at 64.0 GT/s

The test setup should be based on the following:

- Attach the calibration revision 6.0 (for 64.0 GT/s) CLB to the system board DUT with no power applied.
- Connect the Rx lane under test on the CLB to the BERT signal source.
- Connect the Tx lane under test on the CLB to the input of the BERT error detector.
- Make sure that the Tx/Rx lanes other than the lane under test are unterminated.
- Make sure that the scope bandwidth is set to 50 GHz with sampling rate of minimum 6 samples per UI.
- Make sure that the SSC enabled or SSC disabled clock is applied.

Note the setup will not include any Variable ISI channel.

Once the system board DUT is powered on, it should start link training and negotiation to 64.0 GT/s. Send a command from the BERT to the DUT to set the Tx equalization to the following:

- preset 0 (preshoot 1, preshoot 2 and de-emphasis to $0.0 \pm 0.5 \text{ dB}$)

Ensure that this Tx equalization transition is able to complete within a 1 microsecond response timeframe. Record the cursors reported by the DUT for that preset.

Set the BERT error detector to place the DUT in the loopback state and capture the following:

- 3.0 million unit intervals of data ($3.0 \times 10^6 \times 31.25 \text{ ps} = 93.75 \text{ }\mu\text{s}$)

Save the captured waveform for preset 0. Then, repeat the test with presets from Q1 to Q9.

Finally, read the saved waveform files and calculate the preset values using the SigTest Transmitter Preset Test option. The test is considered as successful if all preset values are within their allowable limit range as specified for 64.0 GT/s as well as able to complete within a 1 microsecond response timeframe.

The test should also be repeated with each request for the DUT Tx equalization using the cursors reported by the DUT for that preset.

5.3.2 Add-In Card Tx Link Equalization Response Test at 64.0 GT/s

The test setup should be based on the following:

- Attach the add-in card DUT to the calibration revision 6.0 (for 64.0 GT/s) CBB with no power applied.
- Connect the Rx lane under test on the CBB to the BERT signal source.
- Connect the 100 MHz reference clock output from the BERT to the clock input on the CBB.
- Connect the Tx lane under test on the CBB main board to the input of the BERT error detector.
- Make sure that the Tx/Rx lanes other than the lane under test are unterminated.
- Make sure that the scope bandwidth is set to 50 GHz with sampling rate of minimum 6 samples per UI and a 4th order Bessel-Thomson filter with roll-off from DC value by 3 dB at 33 GHz.

Note the setup will not include any Variable ISI channel.

Once the CBB is powered on, the DUT should start link training and negotiation to 64.0 GT/s. *(Note: An initial preset other than the following presets should be used.)* Send a command from the BERT to the DUT to set the Tx equalization to preset 0. *Ensure that this Tx equalization transition is able to complete within a 1 microsecond response timeframe. Record the cursors reported by the DUT for that preset.*

Set the BERT error detector to place the DUT in the loopback state and capture the following:

- 3.0 million unit intervals of data ($3.0 \times 10^6 \times 31.25 \text{ ps} = 93.75 \text{ }\mu\text{s}$)

Save the captured waveform for preset 0. Then, repeat the test with presets from Q1 to Q9.

Finally, read the saved waveform files and calculate the preset values using the SigTest Transmitter Preset Test option. The test is considered as successful if all preset values are within their allowable limit range as specified for 64.0 GT/s as well as able to complete within a 1 microsecond response timeframe.

The test should also be repeated with each request for the DUT Tx equalization using the cursors reported by the DUT for that preset.

5.4 Overview of DUT Rx Link Equalization Test

The PCIe Gen 6 system board or add-in card DUT will be tested for Rx link equalization as defined by the PHY Test Specification at 64.0 GT/s. This will ensure the DUT can

successfully send commands to adjust the transmitter equalization of its link partner as required.

5.4.1 System Board Rx Link Equalization Test at 64.0 GT/s

The test setup should be based on the following:

- Attach the calibration revision 6.0 (for 64.0 GT/s) CLB to the system board DUT with no power applied.
- Connect the Rx lane under test on the CLB to the signal source.
- Connect the Tx lane under test on the CLB to the input of the BERT error detector.
- Connect the CLB 100 MHz clock output from the system board DUT to the BERT synthesizer (that has passed PCIe 6.0 base specification PLL compliance or equivalent for the respective data rate).
- Make sure that the Tx/Rx lanes other than the lane under test are unterminated.
- Make sure that the SSC enabled or SSC disabled clock is applied.

Adjust the Tx equalization (EQ) of the BERT to align with the initial Tx EQ preset at 64.0 GT/s requested by the system board DUT.

Once the system board DUT is powered on, it should start link training and equalization sequence by the BERT at 64.0 GT/s, which should eventually place the DUT in the loopback state. Run the test for 15 seconds and ensure that the FBER is less than 1E-6 as the pass/fail criteria.

Note: Make sure that all the calibrated parameters (RJ, SJ, DMI, CMI, Vswing and preset) are enabled when the DUT is in the loopback state.

5.4.2 Add-In Card Rx Link Equalization Test at 64.0 GT/s

The test setup should be based on the following:

- Attach the add-in card DUT to the calibration revision 6.0 (for 64.0 GT/s) CBB with no power applied.
- Connect the Rx lane under test on the CBB to the signal source through a Variable ISI channel.
- Connect the Tx lane under test on the CBB main board to the input of the BERT error detector.
- Connect the 100 MHz reference clock output from the BERT to the clock input on the CBB with SSC enabled (-0.5% down-spread).
- Make sure that the Tx/Rx lanes other than the lane under test are unterminated.

Set the BERT to initially transmit with preset Q5. *(Note this is required only if the DUT does not request any preset to be transmitted by the BERT.)*

Once the CBB is powered on, the DUT should start link training and equalization sequence by the BERT, which should eventually place the DUT in the loopback state. Run the test for 15 seconds and ensure that the FBER is less than 1E-6 as the pass/fail criteria.

Note: Make sure that all the calibrated parameters (RJ, SJ, DMI, CMI, Vswing and preset) are enabled when the DUT is in the loopback state.

5.4.3 Link Training

During link training process, the DUT basically goes through multiple states via the status state machine (SSM) method to enter Loopback mode as shown below.

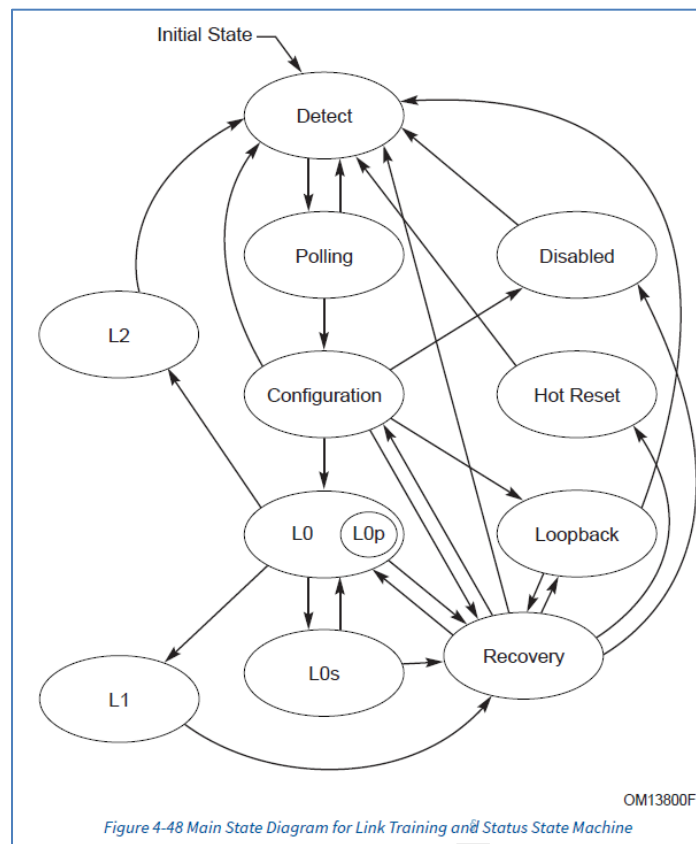


FIGURE 28. MAIN STATE DIAGRAM FOR LINK TRAINING AND STATUS STATE MACHINE (FROM PHY TEST SPECIFICATION)

Below is a loopback training sequence example from PHY Test Specification:

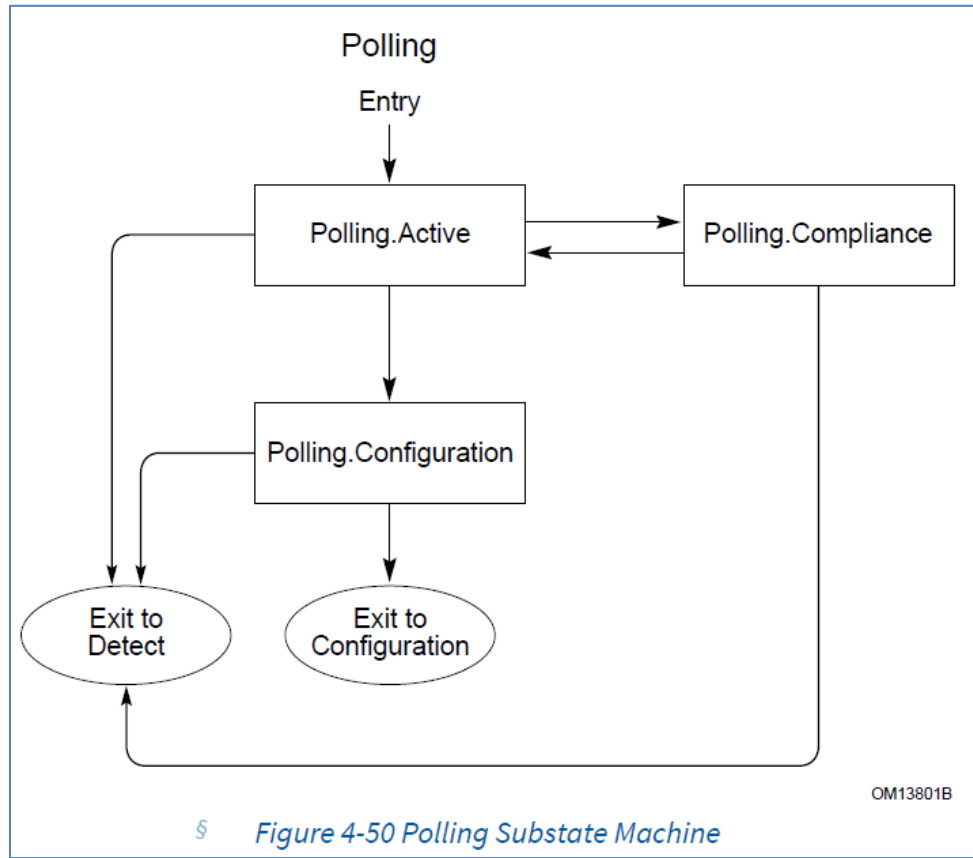


FIGURE 29. POLLING SUBSTATE MACHINE (FROM PHY TEST SPECIFICATION)

1. Enable the DUT to enter the Polling.Active state by sending TS1 with PAD (K23.7).
2. The DUT will go into the Polling.Configuration state after sending more than 1024 TS1 and 8 consecutive TS1 or TS2 with Pad or Loopback bit asserted have been received.
3. The DUT will next enter the Configuration state after 8 consecutive TS2 with PAD have been received and 16 TS2 have been transmitted after 1 TS2 has been received.
4. Start speed negotiation by sending TS1 at 2.5 GT/s advertising the supported speeds. Electrical idle for more than 1 ms allows the product to adjust to the requested speed unless the requested speed is 2.5 GT/s.
5. The DUT will finally switch to the Loopback mode after having two consecutive TS1 at the requested speed with Loopback bit asserted.

5.5 Set Up Automated DUT TxRx Link Equalization Test

Once calibration has been completed from Section 4, continue with the following setup to perform initial link equalization (EQ) tests to prepare the DUT for the final stage of Rx compliance testing. The setup requires the Anritsu MP1900A BERT (including the MU196040B PAM4 Error Detector), PCIe Gen 6 System Board or Add-In Card DUT, MU196060A Re-Driver, and oscilloscope to be used.

5.5.1 Connect Equipment for System Board TxRx Link EQ Testing

The following link EQ test setup uses a PCI-SIG compliance load board (CLB) test fixture for the PCIe Gen 6 System Board DUT.

Note: Before starting the System Board TxRx Link EQ Test, make sure to perform optimization of the Return Path (DUT Tx to BERT error detector).

Note: A Re-Driver may be required for System DUT testing. The return path of the Re-Driver needs to be optimized. The procedure for optimizing the Re-Driver return path is described in the manual at the link below:

<https://dl.cdn-anritsu.com/en-en/test-measurement/files/Application-Notes/Application-Note/mp1900a-pcie6-ef1500.pdf>

Note: Use logical Lane 0 for the following test setup.

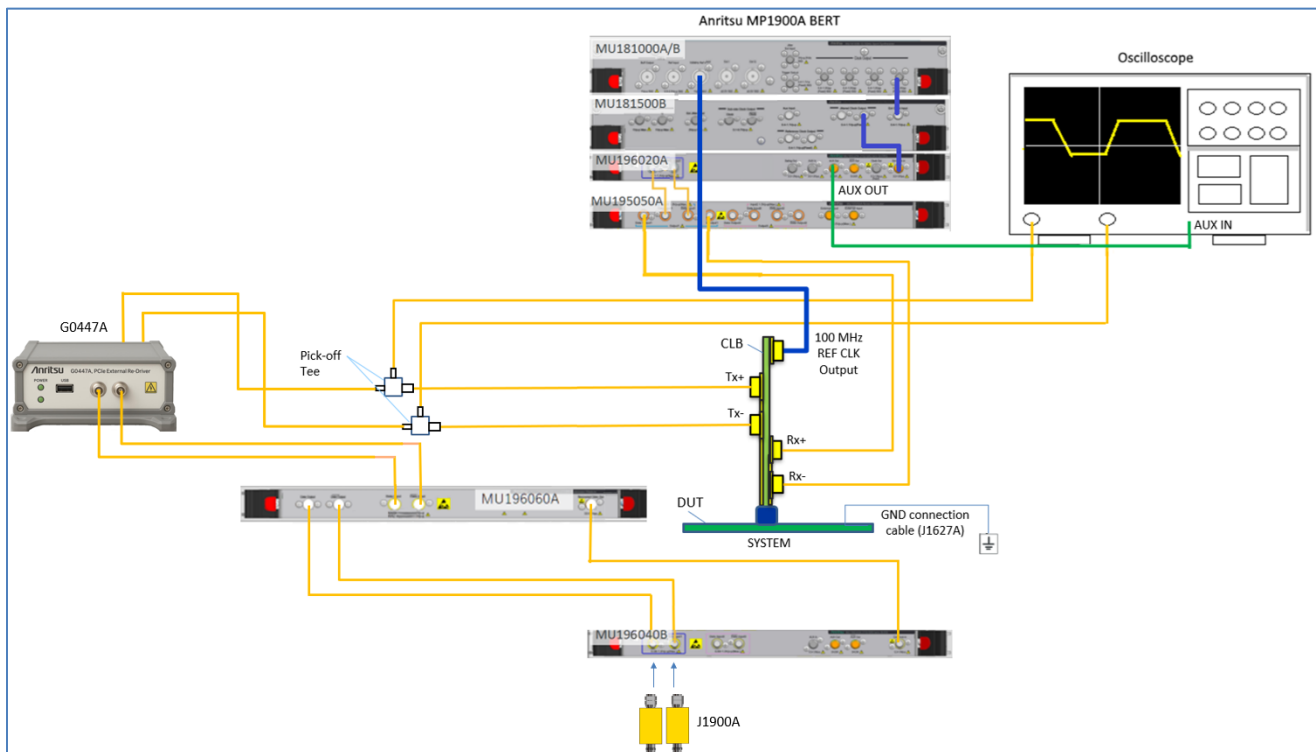


FIGURE 30. RECOMMENDED SETUP FOR DUT TxRx LINK EQ TESTING (PCIe GEN 6 SYSTEM BOARD)

1. Using back the same BERT connections from the Long Channel system board calibration, remove all Variable ISI channels and connect the Ref Clk of the CLB to the 100 MHz Ref Input on the MU181000A/B with a BNC cable.

2. Using a SMA cable, connect a MU196020A Aux Out connector to an Aux input on the oscilloscope. *Note the other unused MU196020A Aux Out connector must be terminated with the J1632A coaxial terminator due to differential signal output (not shown in above setup).*
3. Using coaxial cables, connect the CLB Tx Lanes to the pick-off tee IN ports.
4. Using phase matched cables, connect the oscilloscope channels to the pick-off tee PICK OFF ports.
5. Using coaxial cables, connect the pick-off tee OUT ports to the G0447A external PCIe6 Re-Driver data inputs.
6. Using the J1789A coaxial cables, connect the G0447A data outputs to the MU196060A Re-Driver data inputs.
7. Connect the MU196060A Re-Driver data outputs to the MU196040B data inputs for loopback error detection.
8. Connect the J1900A passive low frequency equalizer to the MU196040B data inputs.
9. Connect the MU196060A Re-Driver clock output to the MU196040B Ext Clock in.
10. Using the J1627A GND connection cable, connect the CLB to ground.

5.5.1.1 Independent Refclk Mode

The following link EQ test setup is similar to the above but uses an external Refclk source for testing in the IR Refclk mode.

Using back the same setup from Figure 30, remove the connection of the CLB's Ref Clk to the 100 MHz Ref Input on the MU181000A/B. The BERT will use its own internal Refclk which mimics an external Refclk source in this mode.

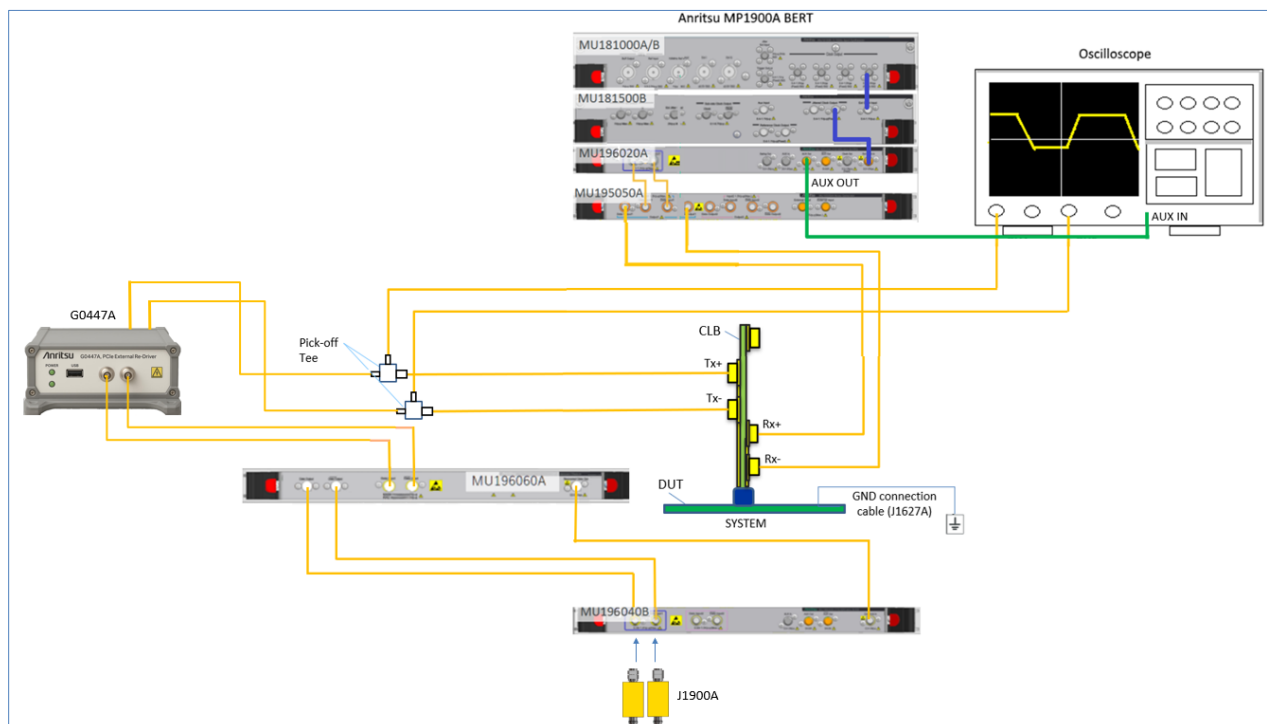


FIGURE 31. RECOMMENDED SETUP FOR DUT TxRx LINK EQ TESTING (PCIe GEN 6 SYSTEM BOARD) IN THE IR REFCLK MODE

5.5.2 Connect Equipment for Add-In Card TxRx Link EQ Testing

The following link EQ test setup uses a PCI-SIG compliance base board (CBB) test fixture for the PCIe Gen 6 Add-In Card DUT.

Note: Use logical Lane 0 for the following test setup.

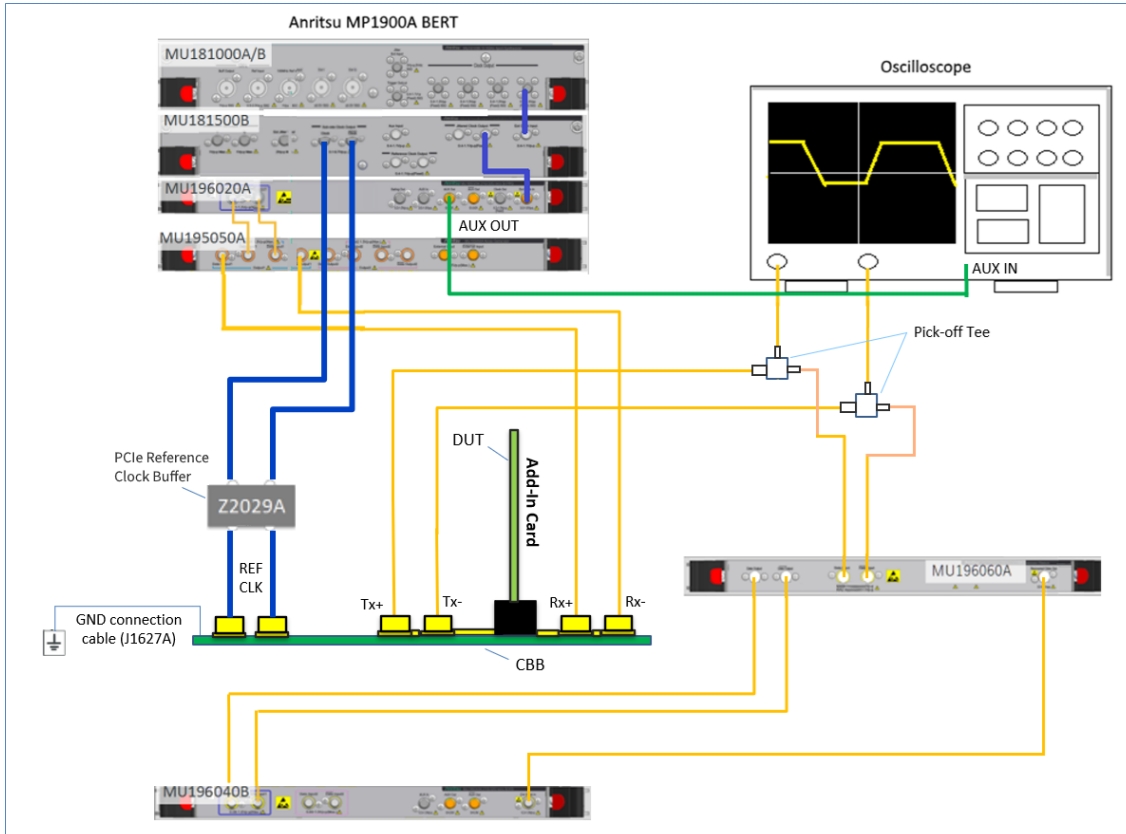


FIGURE 32. RECOMMENDED SETUP FOR DUT TxRx LINK EQ TESTING (PCIe GEN 6 ADD-IN CARD)

Note: Before starting the Add-in Card TxRx Link EQ Test, make sure to perform optimization of the Return Path (DUT Tx to BERT error detector).

1. Using back the same BERT connections from the Long Channel add-in card calibration, remove all Variable ISI channels.
2. Using coaxial cables, connect the MU181500B sub-rate clock outputs to the Ref Clk+/- of the CBB through a Z2029A PCIe reference clock buffer.
3. Using a SMA cable, connect a MU196020A Aux Out connector to an Aux input on the oscilloscope. *Note the other unused MU196020A Aux Out connector must be terminated with the J1632A coaxial terminator due to differential signal output (not shown in above setup).*
4. Using phase matched cables, connect the oscilloscope channels to the pick-off tee PICK OFF ports.
5. Using coaxial cables, connect the CBB Tx Lanes to the pick-off tee IN ports.
6. Using coaxial cables, connect the pick-off tee OUT ports to the MU196060A Re-Driver data inputs.

- ### 5.5.2.1 Independent Refclk Mode

Using back the same setup from Figure 32, remove the connections of the MU181500B sub-rate clock outputs to the Ref Clk+/- of the CBB. The user can choose to connect an external Refclk source to the Ref Clk+/- of the CBB or use the Board Refclk source from the CBB.

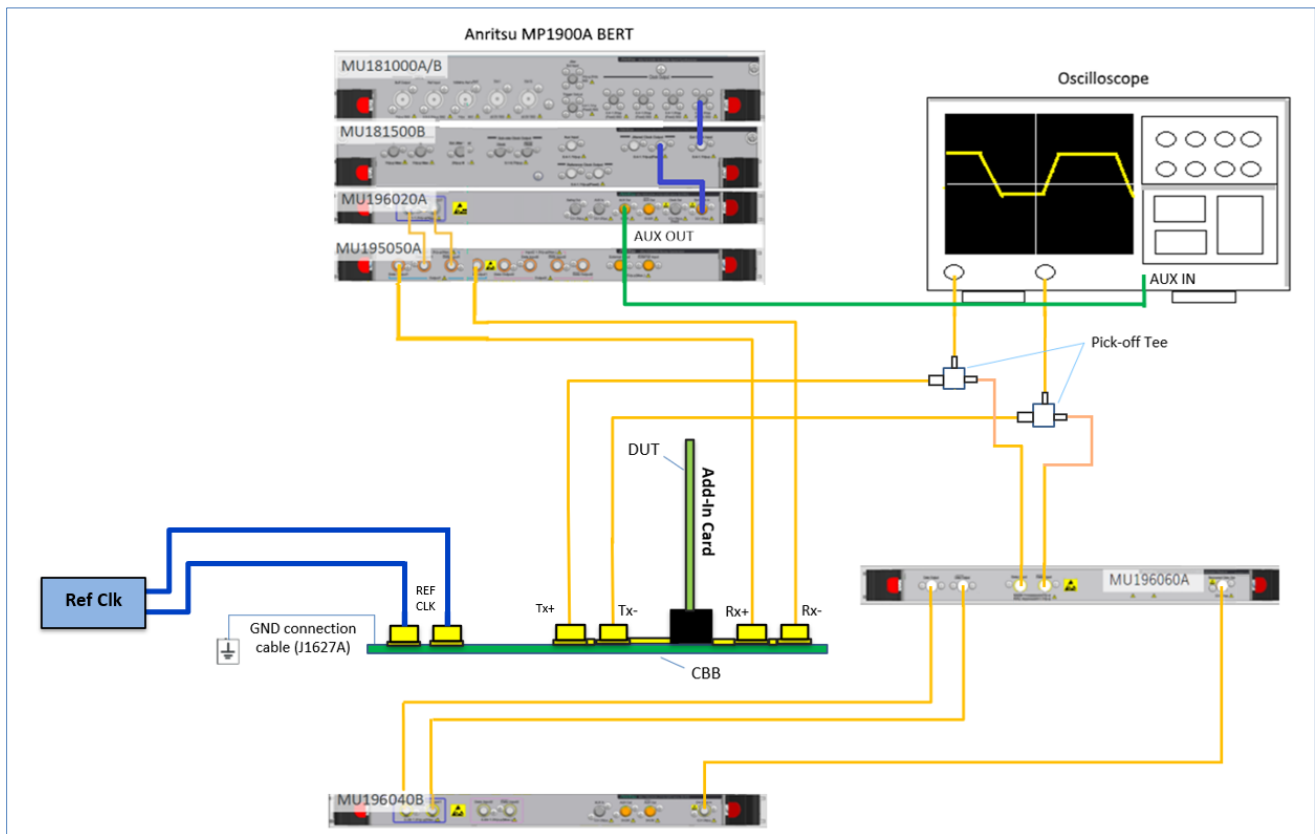


FIGURE 33. RECOMMENDED SETUP FOR DUT TxRx LINK EQ TESTING (PCIe GEN 6 ADD-IN CARD) IN THE IR REFCLK MODE

5.6 Set Up Automated DUT Rx Compliance Test

After the link EQ testing has successfully completed from previous section, proceed with testing for DUT Rx compliance with the following setup.

5.6.1 Connect Equipment for System Board Rx Compliance Testing

The following Rx compliance test setup uses a PCI-SIG compliance load board (CLB) test fixture for the PCIe Gen 6 System Board DUT.

Note: Before starting the System Board Rx Compliance Test, make sure to perform optimization of the Return Path (DUT Tx to BERT error detector).

Note: A Re-Driver may be required for System DUT testing. The return path of the Re-Driver needs to be optimized. The procedure for optimizing the Re-Driver return path is described in the manual at the link below:

<https://dl.cdn-anritsu.com/en-en/test-measurement/files/Application-Notes/Application-Note/mp1900a-pcie6-ef1500.pdf>

Note: Use logical Lane 0 for the following test setup.

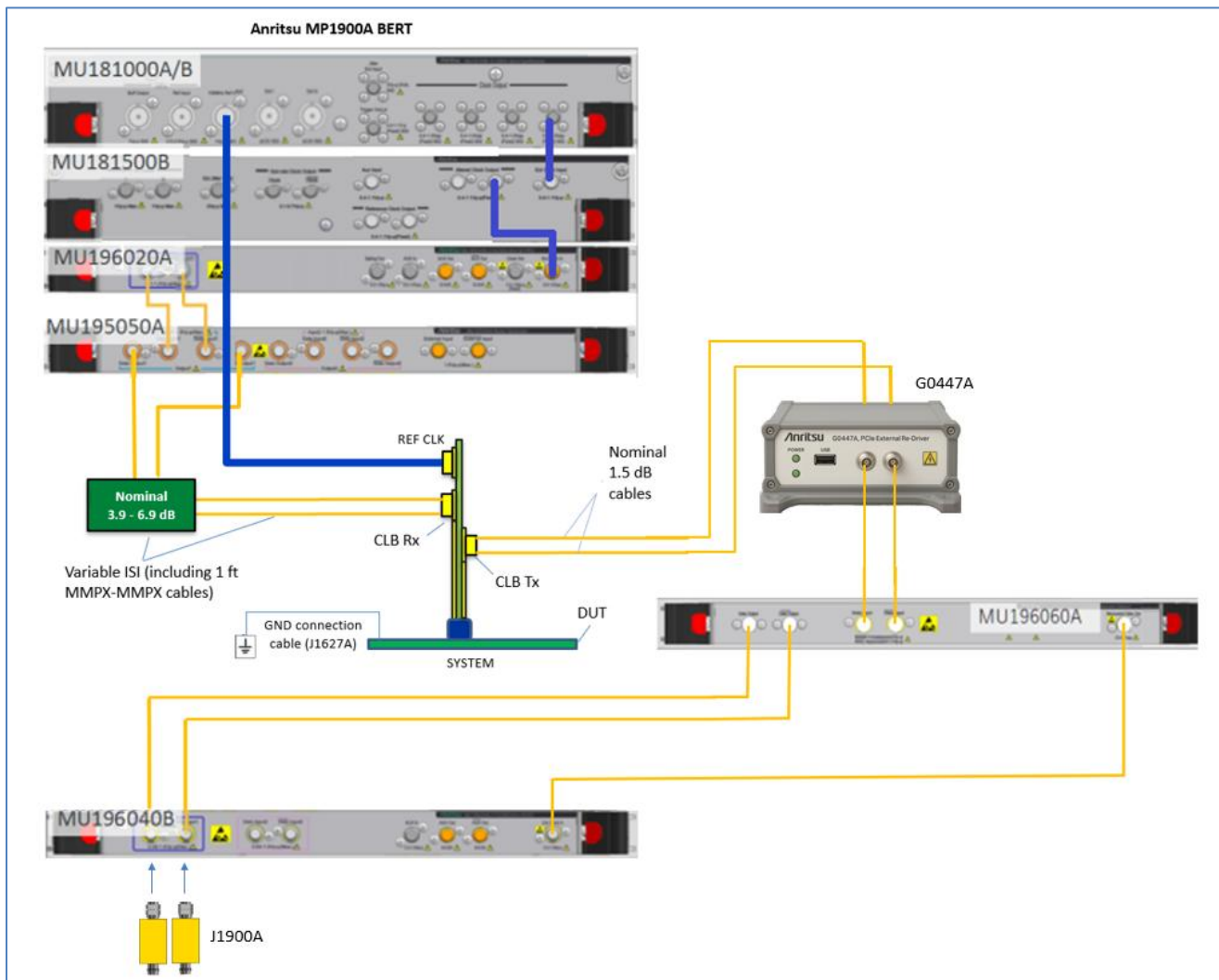


FIGURE 34. RECOMMENDED SETUP FOR DUT RX COMPLIANCE TESTING (PCIe GEN 6 SYSTEM BOARD)

1. Using the same setup from the system board link EQ test, remove all oscilloscope connections along with the pick-off tees.
2. Connect the MU195050A data outputs to the Variable ISI board (Nominal 3.9 – 6.9 dB trace).
3. Connect the Variable ISI board (including 1 ft MMPX-MMPX cables) to the CLB Rx Lane.
4. Using nominal 1.5 dB cables, connect the CLB Tx Lane to the G0447A external PCIe6 Re-Driver data inputs.
5. Using the J1789A coaxial cables, connect the G0447A data outputs to the MU196060A Re-Driver data inputs.
6. Connect the MU196060A Re-Driver data outputs to the MU196040B data inputs for loopback error detection.
7. Connect the J1900A passive low frequency equalizer to the MU196040B data inputs.
8. Connect the MU196060A Re-Driver clock output to the MU196040B Ext Clock in.

5.6.1.1 Independent Refclk Mode

The following Rx compliance test setup is similar to the above but uses an external Refclk source for testing in the IR Refclk mode.

Using back the same setup from Figure 34, remove the connection of the CLB's Ref Clk to the 100 MHz Ref Input on the MU181000A/B. The BERT will use its own internal Refclk which mimics an external Refclk source in this mode.

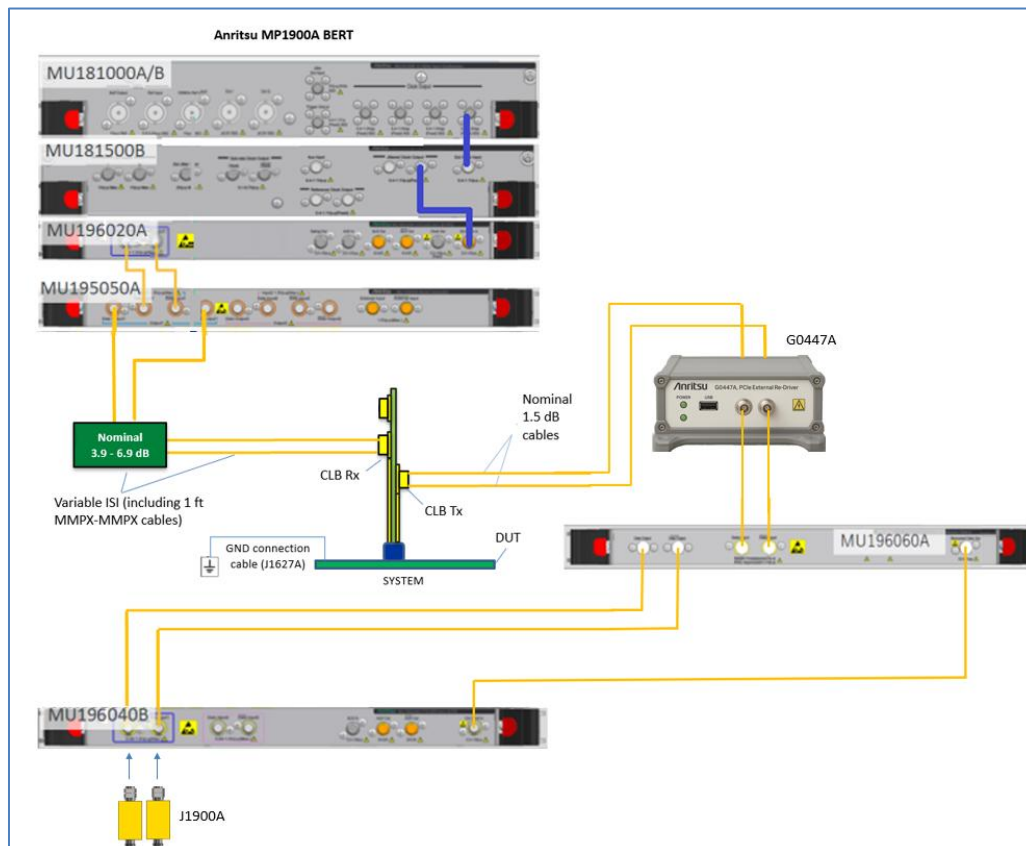


FIGURE 35. RECOMMENDED SETUP FOR DUT RX COMPLIANCE TESTING (PCIe GEN 6 SYSTEM BOARD) IN THE IR REFCLK MODE

5.6.2 Connect Equipment for Add-In Card Rx Compliance Testing

The following Rx compliance test setup uses a PCI-SIG compliance base board (CBB) test fixture for the PCIe Gen 6 Add-In Card DUT.

Note: Use logical Lane 0 for the following test setup.

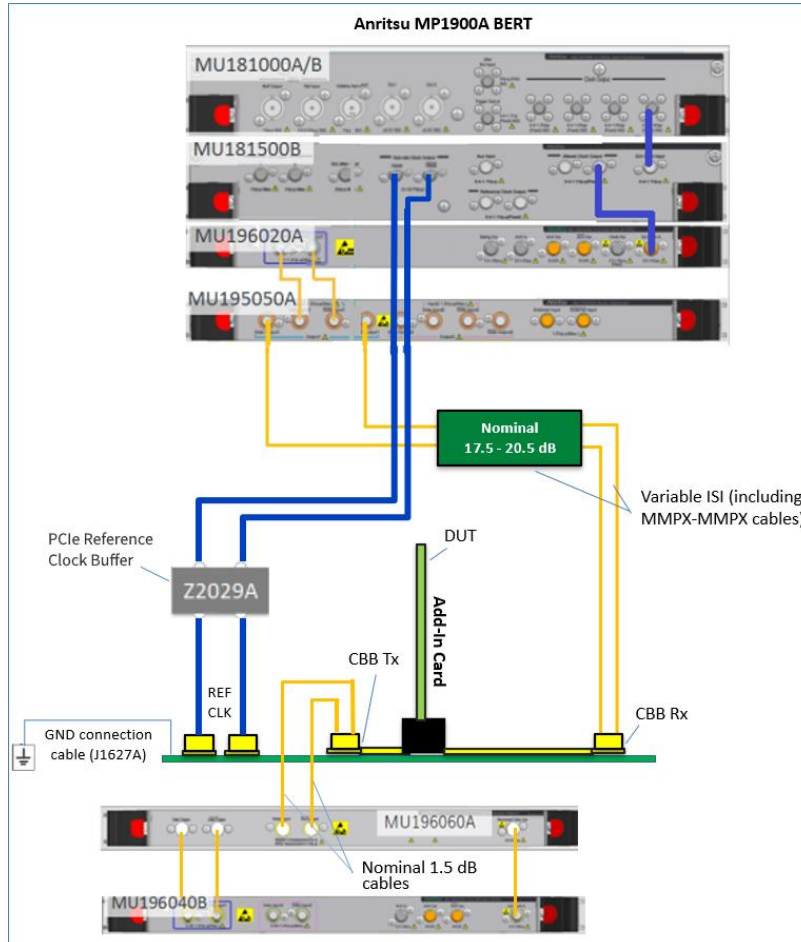


FIGURE 36. RECOMMENDED SETUP FOR DUT RX COMPLIANCE TESTING (PCIe GEN 6 ADD-IN CARD)

Note: Before starting the Add-In Card Rx Compliance Test, make sure to perform optimization of the Return Path (DUT Tx to BERT error detector).

1. Using the same setup from the add-in card link EQ test, remove all oscilloscope connections along with the pick-off tees.
2. Connect the MU195050A data outputs to the Variable ISI board (Nominal 17.5 – 20.5 dB trace).
3. Connect the Variable ISI board (including MMPX-MMPX cables) to the CBB Rx Lane.
4. Using Nominal 1.5 dB cables, connect the CBB Tx Lane to the MU196060A Re-Driver data inputs.
5. Connect the MU196060A Re-Driver data outputs to the MU196040B data inputs for loopback error detection.
6. Connect the MU196060A Re-Driver clock output to the MU196040B Ext Clock in.

5.6.2.1 Independent Refclk Mode

The following Rx compliance test setup is similar to the above but uses an external Refclk source for testing in the IR Refclk mode.

Using back the same setup from Figure 36, remove the connections of the MU181500B sub-rate clock outputs to the Ref Clk+/- of the CBB. The user can choose to connect an external Refclk source to the Ref Clk+/- of the CBB or use the Board Refclk source from the CBB.

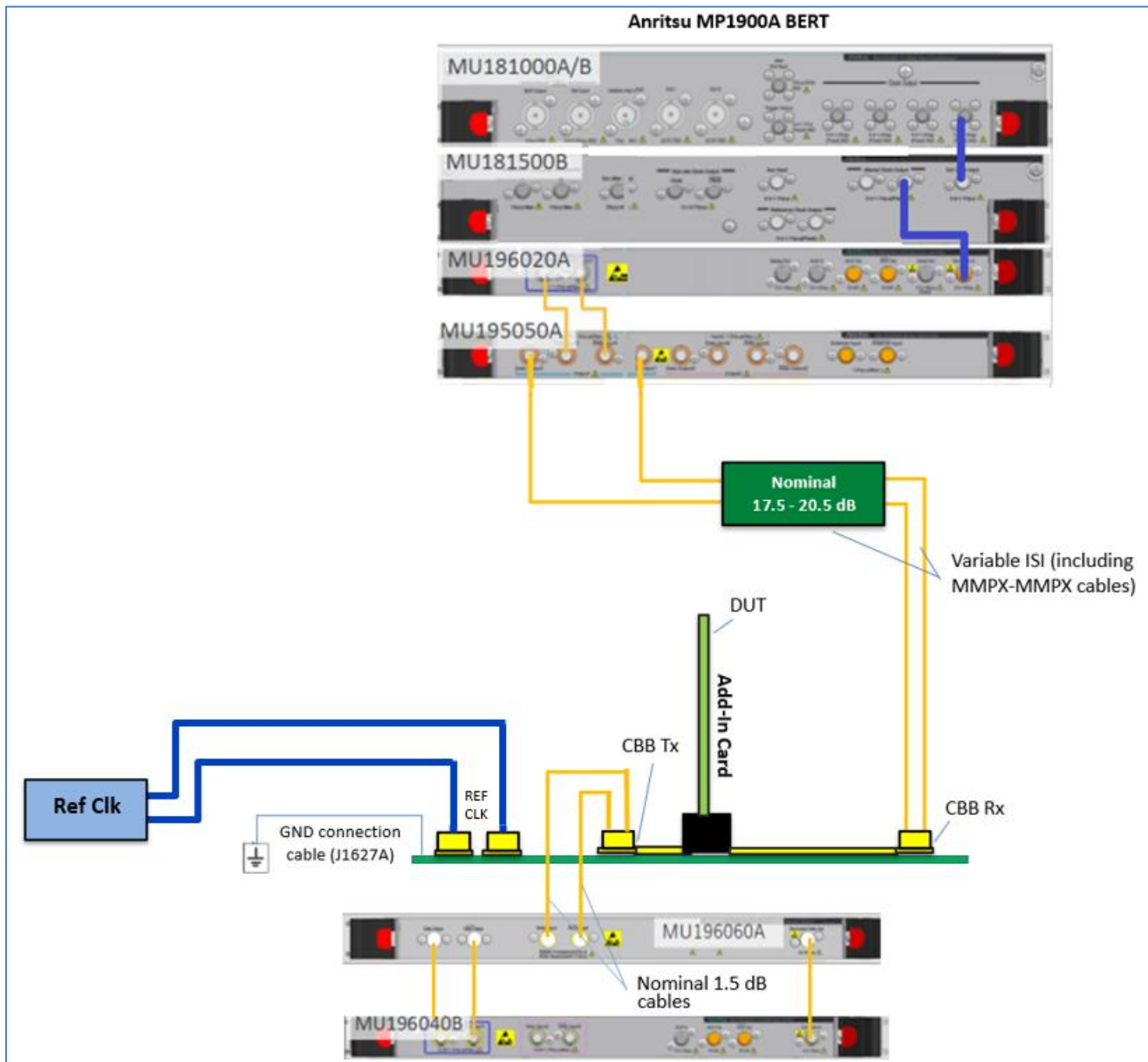


FIGURE 37. RECOMMENDED SETUP FOR DUT RX COMPLIANCE TESTING (PCIe GEN 6 ADD-IN CARD) IN THE IR REFCLK MODE

5.7 Set Up Test Requirements

After setting up the physical equipment, select  from the Anritsu_GRL PCIe CEM 6.0 Rx Test Application menu to access the Setup Configuration page.



FIGURE 38. SET UP TEST REQUIREMENTS

5.7.1 Setup Tab

Select to use a compliant PCIe System Board or Add-In Card as the DUT.

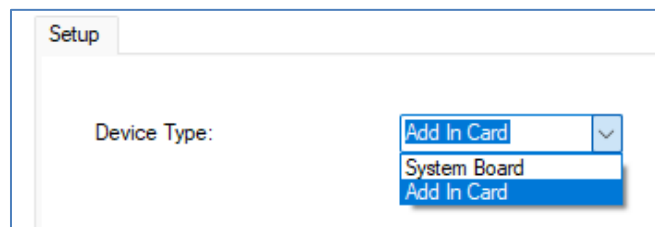


FIGURE 39. SELECT DUT TYPE

5.8 Select PCIe CEM 6.0 Rx Tests

After selecting the DUT type, access the **Select Tests** page on the left of the screen to select the available PCIe CEM 6.0 Rx tests to be run. Select the check box(s) for the required Rx tests.

Note: When running tests for the first time or changing anything in the setup, it is suggested to perform calibration first. If calibration is not completed, attempting to run the Rx tests will throw errors.

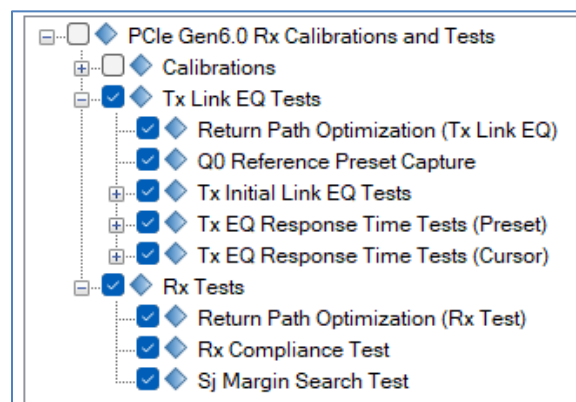


FIGURE 40. SELECT RX TESTS

5.8.1 Select to Run DUT Link Training and Rx Compliance Test

Select the 'Tx Link EQ Tests' group and 'Rx Compliance Test' to prepare and test the DUT for compliance with the PCIe CEM 6.0 Rx specifications. The Anritsu_GRL software will automatically run the link equalization test sequence when initiated. *Note that the 'Tx Initial Link EQ Tests' are only available when the Add-in Card is selected as the DUT in the Setup Configuration page.*

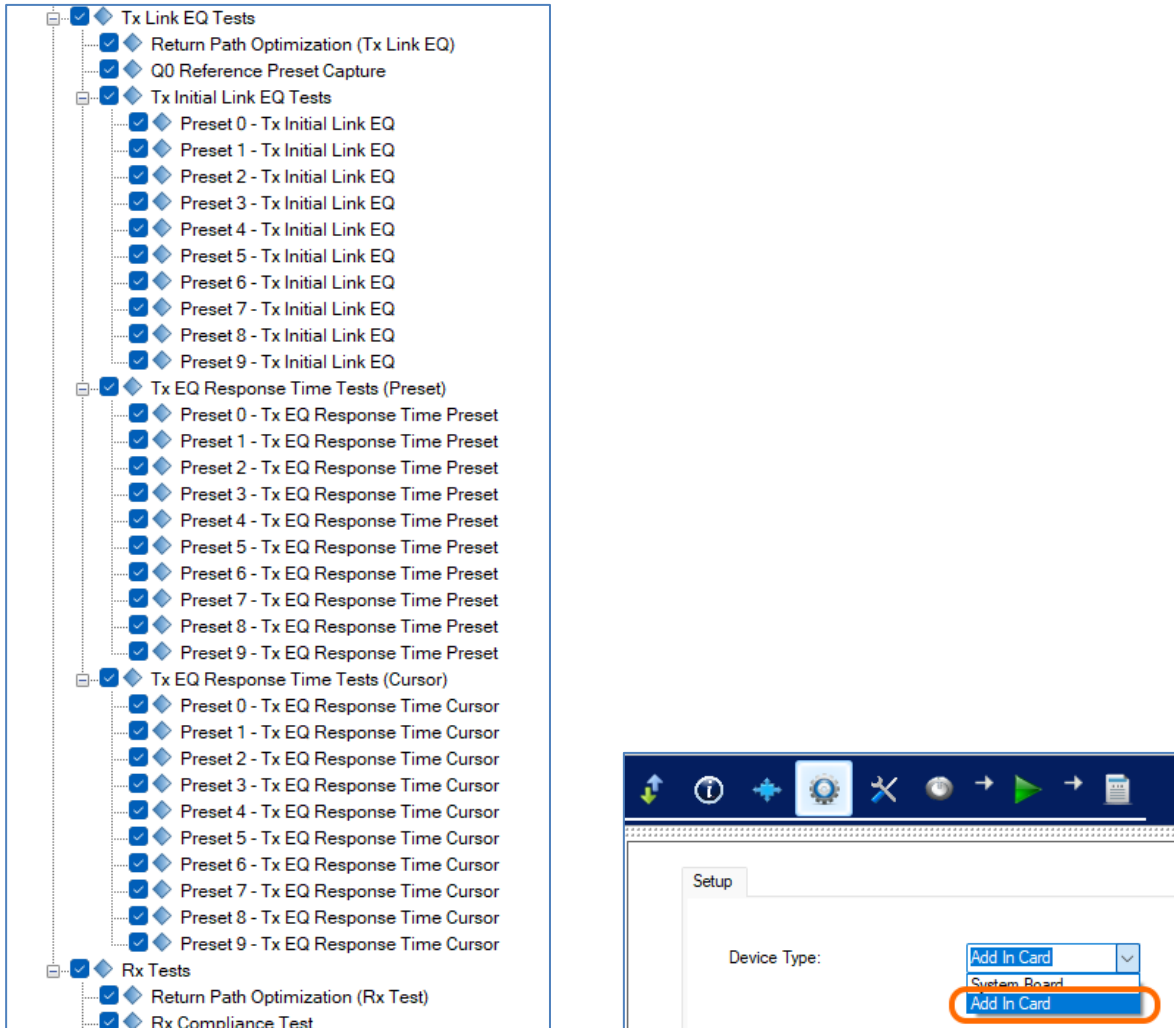


FIGURE 41. SELECT DUT TX LINK EQ AND RX COMPLIANCE TESTS

5.8.2 Select to Run SJ Margin Search Test

Select 'Sj Margin Search Test' to perform an optional test to conduct a SJ margin search for jitter tolerance. The Anritsu_GRL software will automatically run the selected test when initiated.

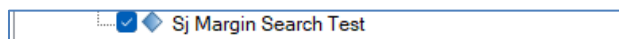
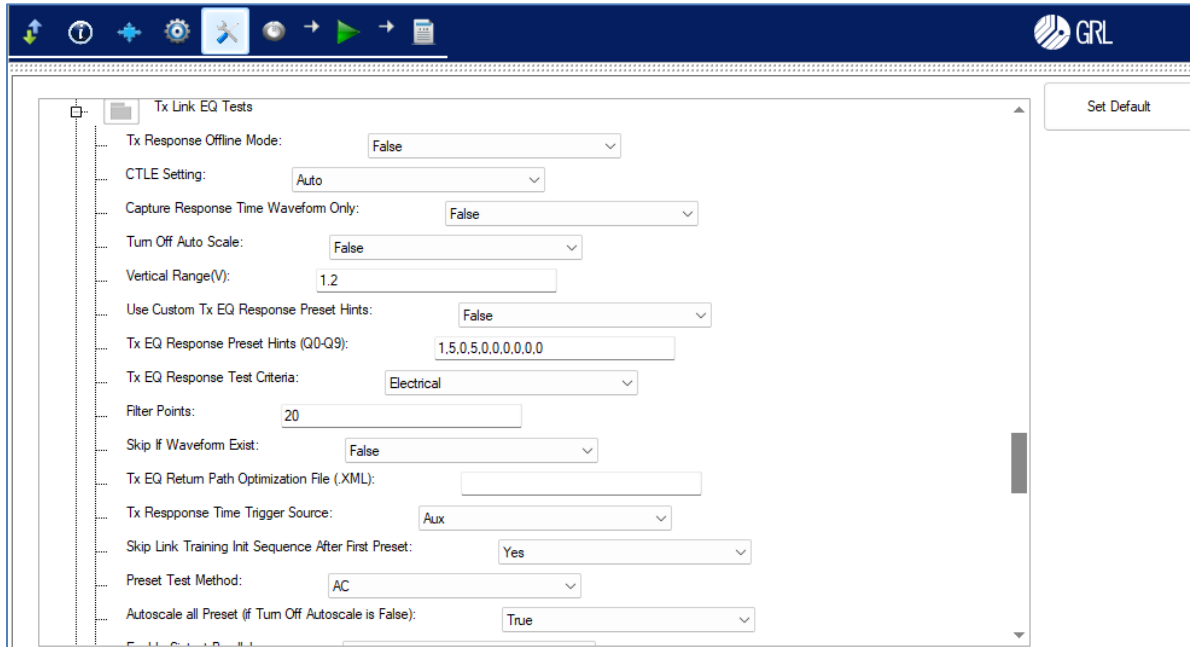


FIGURE 42. SELECT SJ MARGIN SEARCH TEST

5.9 Configure Test Parameters

After selecting the desired tests, select  from the menu to access the Configurations page. Set the required parameters for testing as described below.

To return all parameters to their default values, select the 'Set Default' button.



The screenshot shows the 'Tx Link EQ Tests' configuration page. The parameters and their current values are:

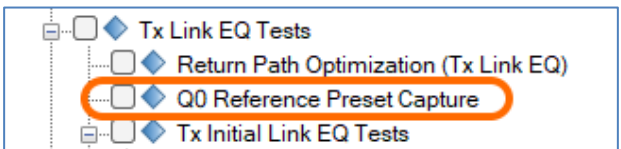
- Tx Response Offline Mode: False
- CTLE Setting: Auto
- Capture Response Time Waveform Only: False
- Turn Off Auto Scale: False
- Vertical Range(V): 1.2
- Use Custom Tx EQ Response Preset Hints: False
- Tx EQ Response Preset Hints (Q0-Q9): 1.5,0.5,0.0,0.0,0.0
- Tx EQ Response Test Criteria: Electrical
- Filter Points: 20
- Skip If Waveform Exist: False
- Tx EQ Return Path Optimization File (.XML):
- Tx Response Time Trigger Source: Aux
- Skip Link Training Init Sequence After First Preset: Yes
- Preset Test Method: AC
- Autoscale all Preset (if Turn Off Autoscale is False): True

A 'Set Default' button is located in the top right corner of the configuration area.

FIGURE 43. TEST PARAMETERS CONFIGURATION PAGE

TABLE 5. TEST PARAMETERS DESCRIPTION

Parameter	Description
Tx Response Offline Mode	Select 'True' to enable running Tx link equalization response tests in offline mode using appropriate offline PCIe compliant waveforms.
CTLE Setting	Select the CTLE method or gain setting index to be used when decoding PCIe compliant waveforms to verify Tx equalization change during link equalization response tests.
Capture Response Time Waveform Only	Select 'True' to enable capturing waveform data for time response verification only when running Tx link equalization response tests.
Turn Off Auto Scale	Select 'True' to disable auto scaling during Tx link equalization response tests.
Vertical Range (V)	Set the vertical range of the Scope to easily detect a change to the voltage level when running Tx link equalization response tests.
Use Custom Tx EQ Response Preset Hints	Select 'True' to enable custom preset hints to be used when running Tx link equalization response tests.

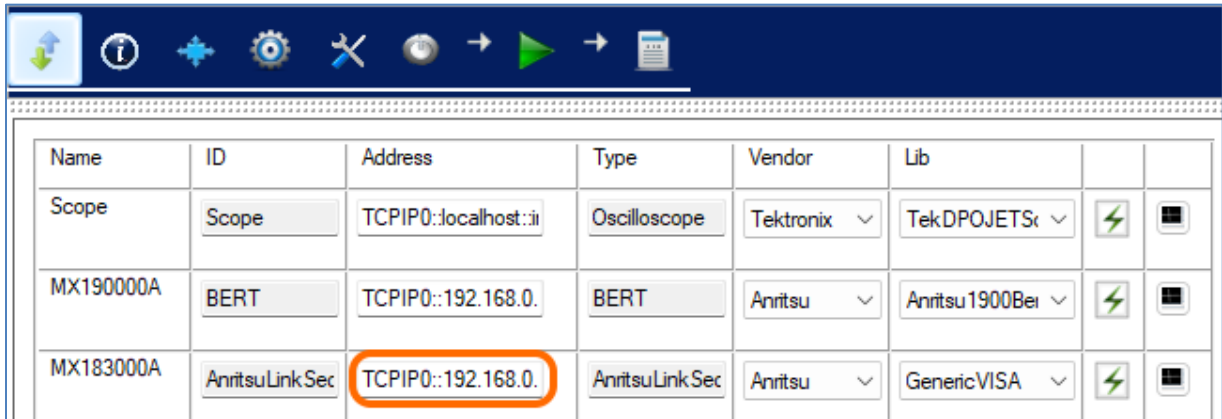
Tx EQ Response Preset Hints (Q0-Q9)	If 'True' is selected from the ' Use Custom Tx EQ Response Preset Hints ' field, specify the custom preset hints for Preset 0 to Preset 9.
Tx EQ Response Test Criteria	Select to enable the Tx link equalization response negotiation to occur in either the 'Electrical' level only or simultaneously in both the 'Electrical and Protocol' level.
Filter Points	Set the number of points that need to be captured.
Skip If Waveform Exist	Select 'True' to skip the Tx link equalization response tests if there are existing waveforms.
Tx EQ Return Path Optimization File (.XML)	Specify the path to recall the XML file saved by the Tx link equalization Return Path Optimization function.
Tx Response Time Trigger Source	Select to use the AUX channel or scope Channel 2 as the Tx Response Time Trigger source.
Skip Link Training Init Sequence After First Preset	Select 'Yes' to skip the link equalization process after the initial preset has been established.
Preset Test Method	Select to use the Link Function Preset Ratio ('LFPR') method during the link training and LTSSM recovery for add-in cards or 'AC' Fit method for Tx equalization preset test or skip the preset test.
Autoscale All Presets (if Turn Off Autoscale if False)	If auto scaling is enabled ('False' is selected from the ' Turn Off Autoscale ' field), select 'True' to enable auto scaling to be carried out for all presets.
Enable SigTest Parallel	Select 'True' to simultaneously run multiple threads of SigTest processing and plot the results.
Expected Tx Response Time Waveform Amplitude (mV)	Set the expected amplitude value of the Tx Response Time Waveform in mV.
Enable Remote SigTest	Select 'True' to enable and use the SigTest functionality remotely.
Preset Fail Action	If a failure occurs during the link equalization process, select to perform an AC power cycle and troubleshoot the link training process ('Test AC'). If not, select 'None'.
Q0 Manual Capture	Select 'True' to enable manual capture of Preset Q0 by forcing the link into Preset Q0 and manually triggering the scope. <i>Note: Selecting "True" will enable the "Q0 Reference Preset Capture" test option under the Tx Link EQ Tests group.</i> 

Q0 Waveform Method	Select the method to measure the Q0 waveform using either a controlled compliance/Manual mode with fixed settings or Link Training.
Clock Architecture	Select the Refclk mode for DUT testing: CC mode (common reference clock), SRIS mode (separate reference clock with independent SSC) or SNRS mode (separate reference clock without SSC).
Enable SSC	Select 'True' to enable Spread Spectrum Clock (SSC) capabilities for receiver testing (if supported by the DUT).
SSC Deviation	If 'True' is selected from the ' Enable SSC ' field, select the Deviation values for SSC.
Auto DUT Reset	Select which controller device connected with the Anritsu_GRL software to be used to perform auto reset for the DUT as required during test runs.
Power Reset Off Time (s)	Set the duration in seconds to reset the power for the system under test when internal power reset mechanism is used.
Power Cycle Off Time (s)	Set the duration in seconds to cycle the power for the system under test when internal power cycle mechanism is used.
Post Reset Wait Time (s)	Set the delay/buffer in seconds after power is reset for the system under test.
Link Training Wait Time (s)	Set the delay/buffer in seconds before initiation of each link training step.
Link Negotiation Wait Time	Set the delay/buffer in seconds during the training phase of a link negotiation.
Log Link Training	Select 'True' to enable logging for the link training steps.
BER Automation	Select 'PCIe Link Training' to run FBER automation tests using Anritsu PCIe Link Sequencer software loopback method, or select 'Manual' to run FBER automation tests manually.
Prompt Before Link EQ Training	Select 'True' to enable a prompt to come up prior to start running Rx link equalization tests.
Ignore Failed Link Training	Select 'True' to ignore tests that have failed when running the PCIe loopback link training sequence.
Compliance FBER Measurement Time (s)	Set the duration in seconds to complete the Rx compliance testing to measure First Bit Error Ratio (FBER).
Maximum FBER Error	Set the maximum error count for error checking during Rx compliance test runs.
Margin Test Measurement Time (s)	Set the duration in seconds to complete the Rx SJ margin search testing.
Margin Test Max Steps	Set the maximum number of steps for stepping through margins during the SJ margin search test.

Margin Test Step Size (%)	Set the step size in percentage for stepping through margins during the SJ margin search test.
Maximum Margin Test FBER Error	Set the maximum error count for error checking during the SJ margin search test.
Default Link Training Sequence	Select 'Yes' to enable the default sequence for link training to be used.
Retrain When SJ Frequency Changed	Select 'True' to re-send link training sequence when there is a change in the SJ frequency.
Margin Search Live Plot	Select 'True' to enable a graphical margin plot that updates as the margin test is performed to indicate progress of the test results.
Apply CM	Select 'Yes' to integrate the common mode component in a specific test.
PPG Start Preset	Select the preset co-efficient to be used at the start of link training.
DUT Initial Preset	Select the initial preset co-efficient for the DUT to be applied during Rx compliance test runs.
DUT Final Preset	Select the preset co-efficient for the DUT to be applied during the final FBER test.
Rx Test Return Path Optimization File (.XML)	Specify the path to recall the XML file saved by the Rx compliance test Return Path Optimization function.
Auto Search	Select to use either the automatic search mode or manual mode for CTLE or skip the search for CTLE.
Enable Channel ISI	Select 'True' to enable the ISI channel to be used during testing.

5.10 Enable Loopback FBER Test

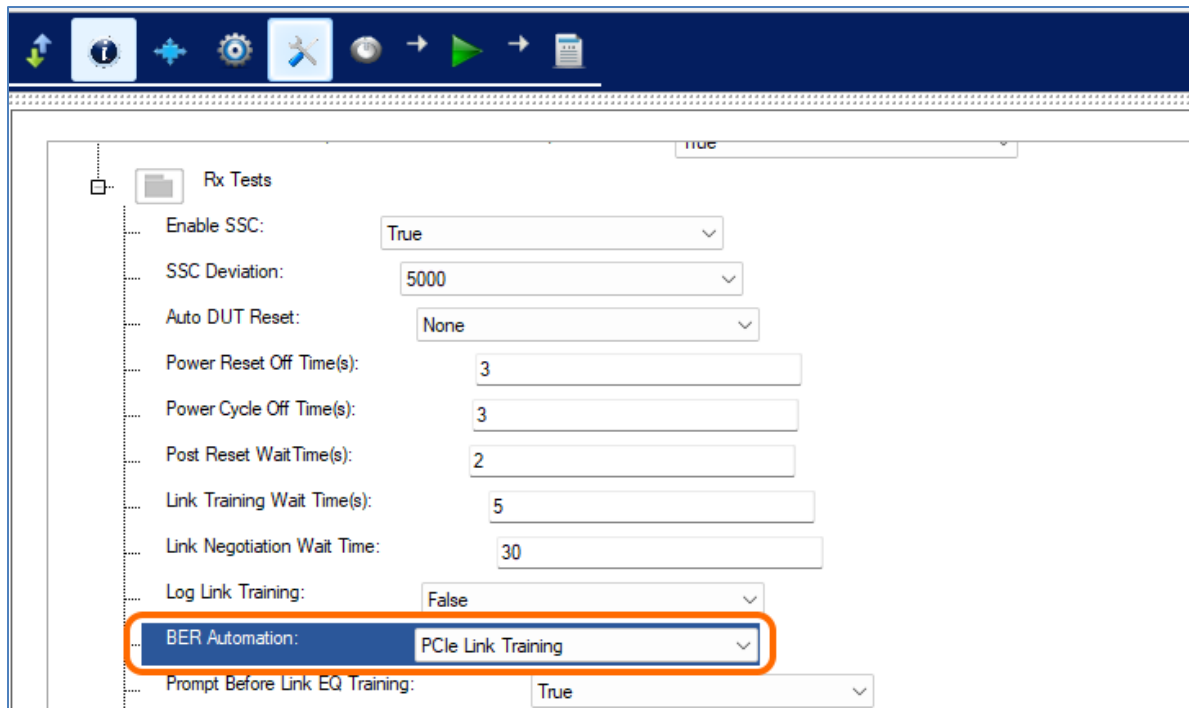
To set up the Anritsu_GRL software to automate loopback testing for error detection, go to the Equipment Setup  page and type in the VISA address that connects to the Anritsu MX183000A High-Speed Serial Data Test Software.



Name	ID	Address	Type	Vendor	Lib		
Scope	Scope	TCPIP0::localhost::i	Oscilloscope	Tektronix	TekDPOJETSc		
MX190000A	BERT	TCPIP0::192.168.0.	BERT	Anritsu	Anritsu1900Bei		
MX183000A	AnritsuLinkSec	TCPIP0::192.168.0.	AnritsuLinkSec	Anritsu	GenericVISA		

FIGURE 44. CONNECT EQUIPMENT FOR LOOPBACK FBER TEST

On the Configurations  page, select the FBER Automation test method as 'PCIe Link Training' to enable the Anritsu PCIe Link Sequencer software loopback mode. Additional configurations can also be made through this page.

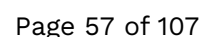
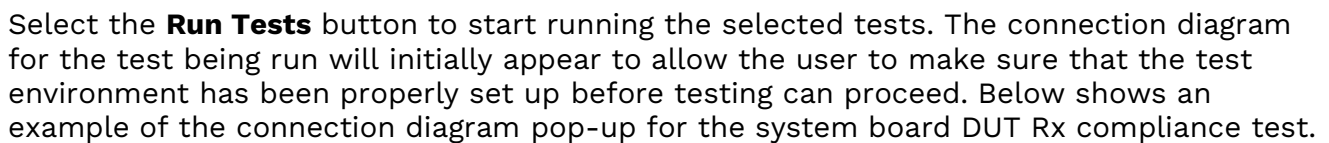


Rx Tests

- Enable SSC: True
- SSC Deviation: 5000
- Auto DUT Reset: None
- Power Reset Off Time(s): 3
- Power Cycle Off Time(s): 3
- Post Reset WaitTime(s): 2
- Link Training Wait Time(s): 5
- Link Negotiation Wait Time: 30
- Log Link Training: False
- BER Automation: PCIe Link Training**
- Prompt Before Link EQ Training: True

FIGURE 45. SELECT FBER LOOPBACK TEST METHOD

- **Skip Test if Result Exists** – If results from previous tests exist, the software will *skip* those tests.
- **Replace if Result Exists** – If results from previous tests exist, the software will *replace* those tests with new results.



6 Interpreting Anritsu_GRL-PXE6-CEM-RXA Test Report

When all calibration and test runs have completed from the previous section, the Anritsu_GRL-PXE6-CEM-RXA software will automatically display the results on the **Report** page.

Select  from the menu to access the Report page for a quick view of all results.

If some of the results are not desired, they can be individually deleted by selecting the **Delete** button.

For detailed test report, select the **Generate report** button to generate a PDF report. To have the calibration data plotted in the report, select the **Plot Calibration Data** checkbox.

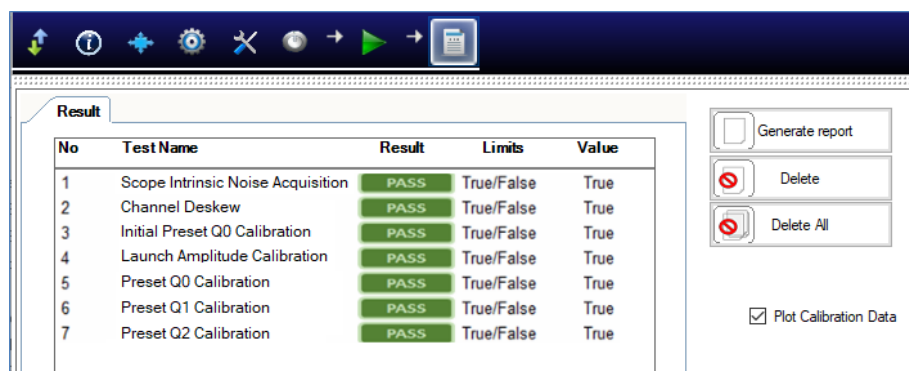


FIGURE 48. TEST REPORT PAGE

6.1 Understand Test Report Information

This section gives a general overview of the test report to help users familiarize themselves with the format. Select the **Generate report** button to generate the test report.

6.1.1 Test Session Information

This portion displays the information previously entered on the **Session Info** page.

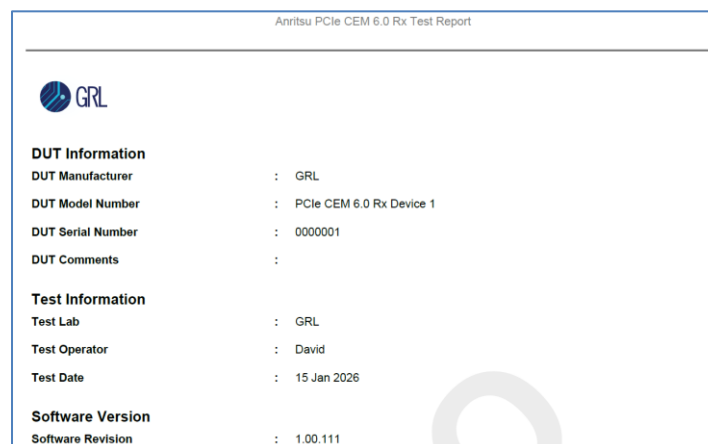


FIGURE 49. TEST SESSION INFORMATION EXAMPLE

6.1.2 Test Summary Table

This table provides an overall view of all the calibration and tests performed along with their conditions and results.

No	TestName	Limits	Value	Results	SJ Frequency
1	Scope Intrinsic Noise Acquisition	N/A	N/A	Pass	
2	Initial Preset Q0 Calibration	N/A	N/A	Pass	
3	Launch Amplitude Calibration	N/A	N/A	Pass	
4	Bert Intrinsic Jitter Measurement	N/A	N/A	Pass	
5	Preset Q0 Calibration	N/A	N/A	Pass	
6	Preset Q1 Calibration	N/A	N/A	Pass	
7	Preset Q2 Calibration	N/A	N/A	Pass	
8	Preset Q3 Calibration	N/A	N/A	Pass	
9	Preset Q4 Calibration	N/A	N/A	Pass	
10	Preset Q5 Calibration	N/A	N/A	Pass	
11	Preset Q6 Calibration	N/A	N/A	Pass	
12	Preset Q7 Calibration	N/A	N/A	Pass	
13	Preset Q8 Calibration	N/A	N/A	Pass	
14	Preset Q9 Calibration	N/A	N/A	Pass	
15	Rj Calibration	N/A	N/A	Pass	
16	Sj Calibration	N/A	N/A	Pass	SJ (100Mhz)
17	Preset EQ Optimization (Seasim)	N/A	N/A	Pass	
18	Final Eye Calibration (Seasim)	N/A	N/A	Pass	
19	CM Calibration	N/A	N/A	Pass	
20	DM Calibration	N/A	N/A	Pass	

Rx Compliance Test

Sj Frequency	SJ_100Mhz
Result	PASS(1)

*Note: In the example above, the number “(1)” next to “PASS” indicates the number of errors detected along with the pass/fail status.

FIGURE 50. TEST SUMMARY TABLE EXAMPLE

6.1.3 Test Results

This portion displays the results in detail along with supporting data points and screenshots for each calibration/test run.

16. Sj Calibration [SJ_100Mhz]

Pass/Fail Stats : Pass
Cal Parameter : SJ_Gen6_64G__SJ_100Mhz
Intrinsic Jitter : 116.8000 mUI
Settings : 64.0000 mUI(p-p)
Measured Value : 51.2000 mUI(p-p)
SigTest Version : 6.1.13
Test completed time : 27 October 2025 19:20:17 PM

Screen shots 1

Keysight Infiniium : Monday, October 27, 2025 4:17:30 AM

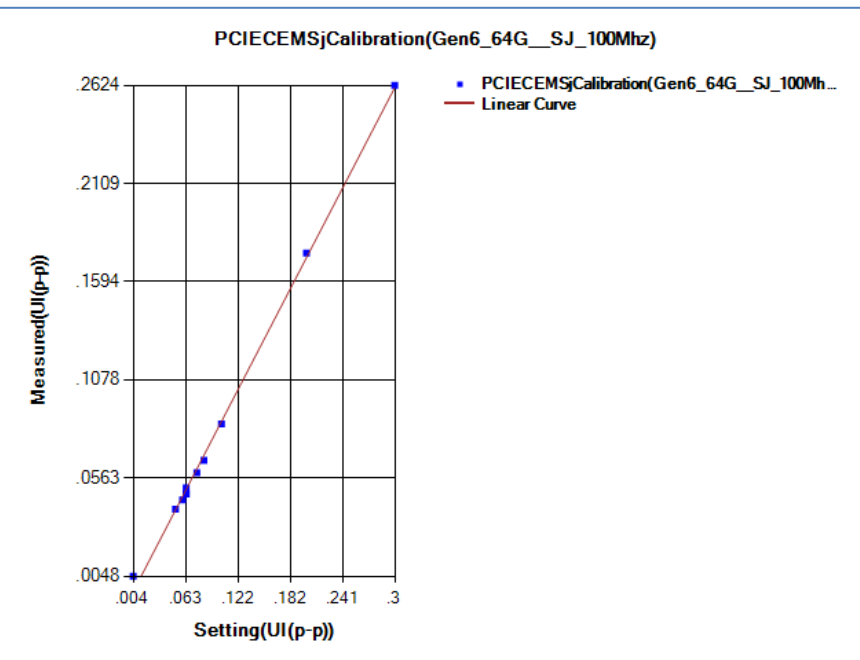


FIGURE 51. TEST RESULTS EXAMPLE

6.2 Delete Test Results

To individually delete any unwanted calibration/test results, select the corresponding result row and **Delete** button.

To entirely remove all existing calibration/test results, select the **Delete All** button.

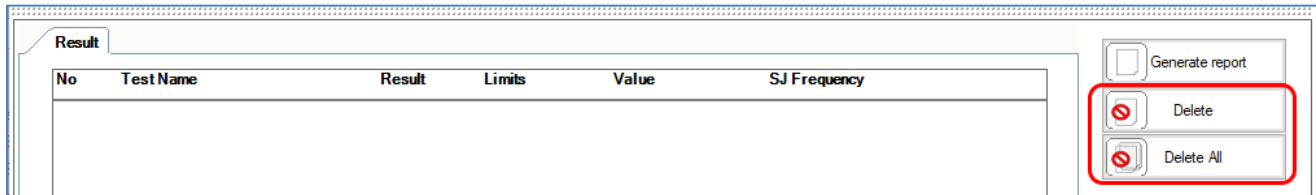


FIGURE 52. DELETE TEST RESULTS

7 Saving and Loading Anritsu_GRL-PXE6-CEM-RXA Test Sessions

The usage model for the Anritsu_GRL-PXE6-CEM-RXA software is that the test results are created and maintained as a 'Live Session' in the application. This allows the user to quit the application and return later to continue where the user left off.

Save and Load Sessions are used to save a test session that the user may want to recall later. The user can 'switch' between different sessions by saving and loading them when needed.

- To **save a test session**, with all of the test parameter information, test results, and any waveforms, select the Options drop-down menu and then select 'Save Session'.
- To **load a test session** back into the application, including the saved test parameter settings, select Options → 'Load Session'.
- To **create a new test session** and return the application back to the default configuration, select Options → 'New Session'.

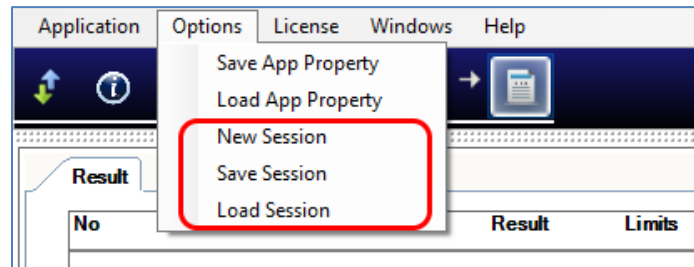


FIGURE 53. SAVE/LOAD/CREATE TEST SESSIONS

The test configuration and session results are saved in a file with the '.ses' extension, which is a compressed zip-style file, containing a variety of information.

8 Appendix A: Method of Implementation (MOI) for Manual PCIe CEM 6.0 Receiver Measurements

This section describes how to manually perform PCIe CEM 6.0 Rx calibration and DUT compliance testing based on Anritsu's recommended test procedure using the MP1900A BERT.

The following steps give a general overview for testing the PCIe CEM 6.0 receiver.

- i) Calibrate for the following components:
 - Channel Loss measurement with a vector network analyzer (VNA)
 - Initial Preset Q0, Launch Amplitude, Preset Q1-Q9, BERT Intrinsic Jitter, RJ and SJ measurements with MP1900A BERT and high-performance real-time oscilloscope
 - DM & CM Amplitude and Eye Height/Eye Width measurements with MP1900A BERT and high-performance real-time oscilloscope
- ii) Perform link training sequence for FBER loopback testing:
 - Enable DUT loopback mode for error detection with MP1900A BERT
 - Troubleshoot in the case of link training failure
- iii) Test for DUT Rx compliance to target specifications:
 - FBER compliance checking for $<1E-6$ with stressed eye
 - SJ marginal testing (optional)

Note: Existing PCI-SIG Compliance Load Boards (CLB's) and Compliance Base Boards (CBB's) will be used as test fixtures for system host and device DUT's respectively.

8.1 Perform Calibration

This section describes how to calibrate the stressed test signal before testing the receiver for compliance.

Calibration is initially performed for Channel Loss, followed by Initial Preset Q0, Launch Amplitude, Q1-Q9 Preset, BERT Intrinsic Jitter, and RJ & SJ. The final step is to determine the Eye Width (EW) & Eye Height (EH) and DM & CM.

The main equipment required for calibration consists of the MP1900A BERT, high performance real-time oscilloscope and vector network analyzer. The SigTest/Seasim application will also be used to ensure signal quality compliance.

8.1.1 Calibration Settings

Configure the following settings to be applied for PCIe Gen 6 based Rx calibration.

TABLE 6. CALIBRATION SETTINGS

Component	Setting	PCIe Gen 6
Variable ISI Board	Insertion Loss (dB)	30–33 ^[a]
Seasim	CTLE Gain (dB)	0–30 ^[b]
MP1900A BERT	Tx Emphasis Preset	Q0 to Q10
	Amplitude (mV)	550 (800 mVpp-diff at output of Noise Module)
	RJ (ps rms)	0.25
	SJ @100 MHz (mUIpp)	50
	DM-I (mVpp)	15
	CM-I (mVpp)	75

^[a] The insertion loss measures in between 30 to 33 dB for all configurations using different variable ISI pairs that provide the correct amount of insertion loss being measured.

^[b] The CTLE range from 0 dB to 30 dB in 1 dB step sizes is run for every waveform. (Note that this is a subset of allowed CTLE range. This subset is used to reduce calibration time.)

The following table shows the calibration targets to achieve:

TABLE 7. CALIBRATION TARGETS

Setting	PCIe Gen 6
Amplitude (mV)	800
RJ (ps rms)	0.25
SJ @100 MHz (mUIpp)	50 (at TP3)
DM-I (mVpp)	15 (at TP2)
CM-I (mVpp)	75
EH (mVpp)	$5.50 \leq EH \leq 6.50$
EW (UI)	$0.09 \leq EW \leq 0.11$

8.1.2 Channel Loss Calibration

The following connection diagram shows the channel loss calibration setup for PCIe Gen 6 using a 4-port (differential) vector network analyzer (VNA) and a compliant CLB/CBB test fixture for the add-in card and system board.

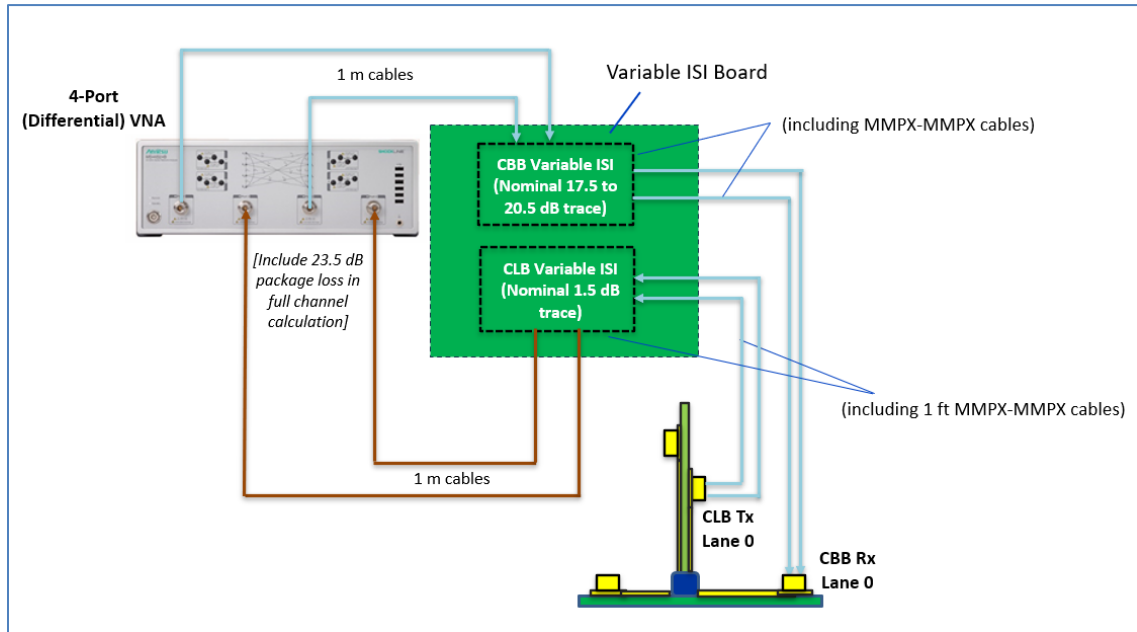


FIGURE 54. CONNECTION DIAGRAM FOR CHANNEL LOSS CALIBRATION (ADD-IN CARD)

Note: For the Add-In Card CEM Rx calibration, a -8.5 dB add-in card budget and -17.5 to -20.5 dB system budget shall be used in the intended 30 to 33 dB pad-to-pad loss range.

1. Connect the CBB Rx Lane 0 with CBB Variable ISI (Nominal 17.5 to 20.5 dB trace, including MMPX-MMPX cables) and CLB Tx Lane 0 with CLB Variable ISI (Nominal 1.5 dB trace, including 1 ft MMPX-MMPX cables).
2. Using 1 m cables, connect between both the VNA Ports 1 & 3 and the CBB Variable ISI and between both the CLB Variable ISI and the VNA Ports 2 & 4.

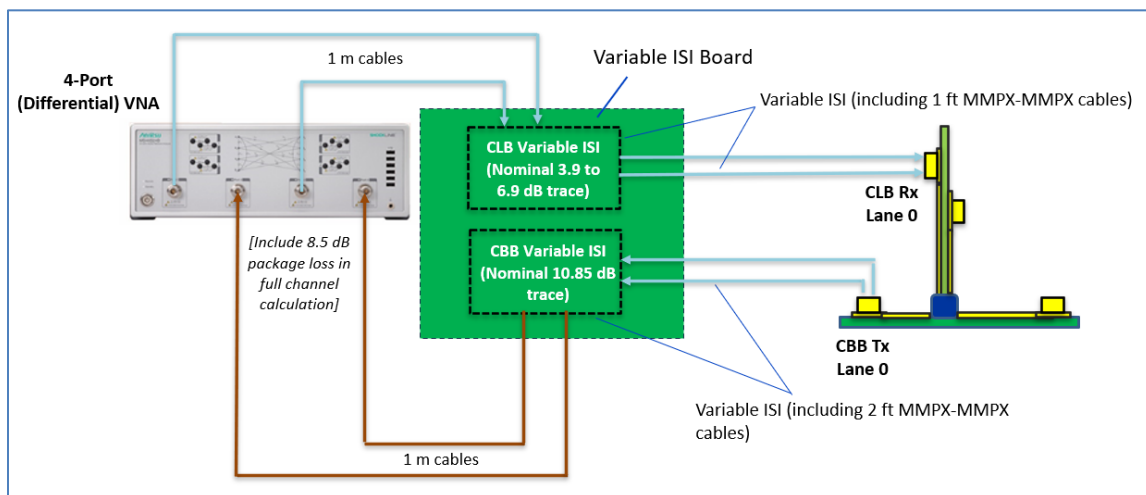


FIGURE 55. CONNECTION DIAGRAM FOR CHANNEL LOSS CALIBRATION (SYSTEM BOARD)

Note: For the System Board CEM Rx calibration, a -23.5 dB system budget (15.7 dB physical channel + 7.8 dB PKG) and -6.5 to -9.5 dB add-in card budget shall be used in the intended 30 to 33 dB pad-to-pad loss range.

1. Connect the CLB Rx Lane 0 with the CLB Variable ISI (Nominal 3.9 to 6.9 dB trace, including 1 ft MMPX-MMPX cables).
2. Connect the CBB Tx Lane 0 with the CBB Variable ISI (Nominal 10.85 dB trace, including 2 ft MMPX-MMPX cables).
3. Using 1 m cables, connect between both the VNA Ports 1 & 3 and the CLB Variable ISI and between both the CBB Variable ISI and the VNA Ports 2 & 4.

8.1.3 Amplitude, Preset, SJ and RJ Calibration Setup

The following connection diagram shows the calibration setup for amplitude, preset, SJ, and RJ at TP3 without any channel effect. The MP1900A BERT is directly connected to a digital oscilloscope supporting ≥ 50 GHz bandwidth and ≥ 192 GS/s sampling rate.

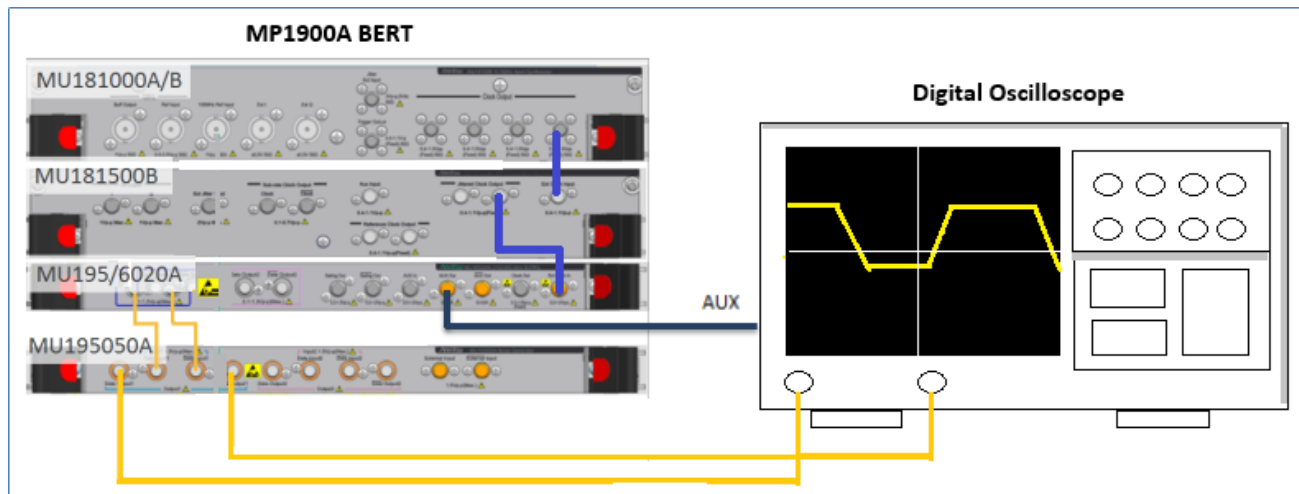


FIGURE 56. CONNECTION DIAGRAM FOR AMPLITUDE, PRESET, SJ AND RJ CALIBRATION

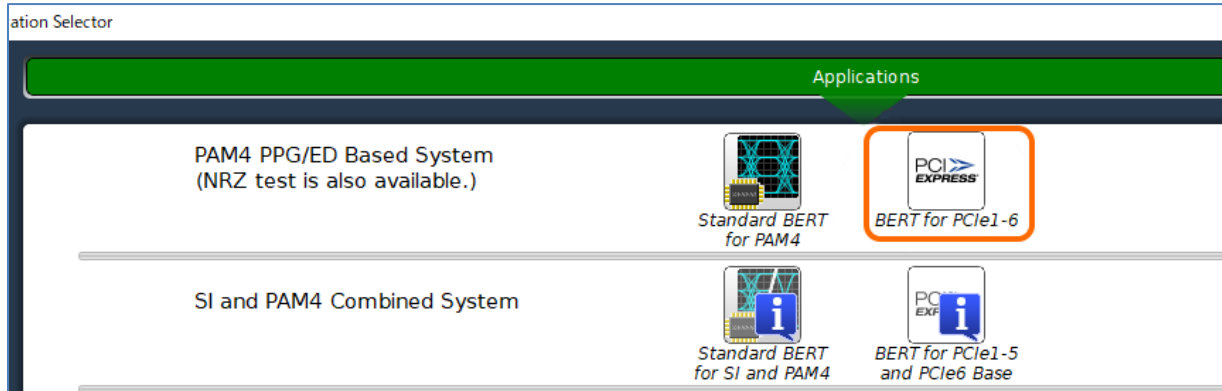
Note: If the oscilloscope does not support 192 GS/s sampling rate at minimum, it is required to use Sinx/x interpolation to achieve minimum 6 samples per UI.

1. Using a SMA-SMA short cable, connect the MU181000A/B clock output to the MU181500B Ext clock input.
2. Using a SMA-SMA short cable, connect the MU181500B jittered clock output to the MU195020A/MU196020A Ext clock input.
3. Using coaxial cables, connect the MU195020A/MU196020A data outputs to the MU195050A data inputs.
4. Using coaxial cables, connect the MU195050A data outputs to the digital Scope channels.
5. Using a SMA cable, connect the MU195020A/MU196020A Aux output to the digital Scope for pattern sync triggering.

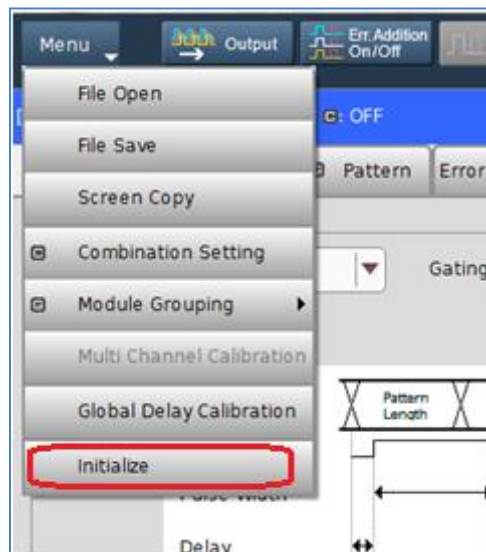
8.1.4 Anritsu Standard BERT Device Test Application (MX190000A) Startup

To adjust the calibration parameters when measuring on the Scope, use the MX190000A Standard test application on the MP1900A BERT.

1. On the BERT's Applications screen, select the "BERT for PCIe1-6" application.



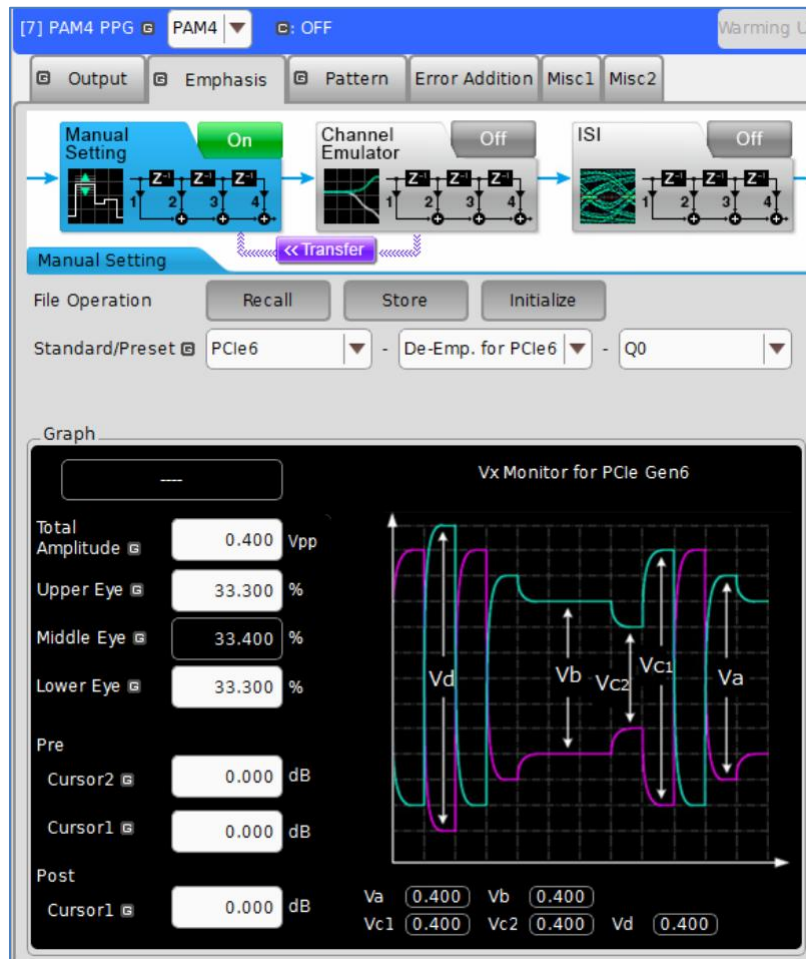
2. In the drop-down Menu, select 'Initialize' to start using the application.



8.1.5 Initial Preset Q0 Calibration

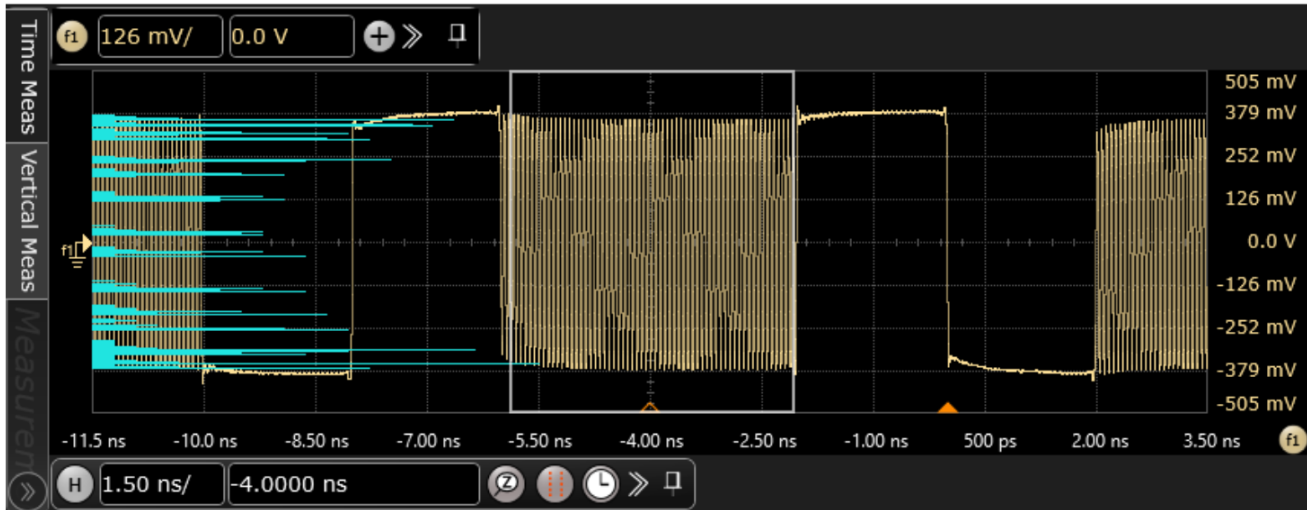
Adjust the Pre Cursor1, Pre Cursor2 and Post Cursor1 of Preset Q0 to 0 ± 0.3 dB with Scope markers using the following configuration:

- a) BERT Settings:
 - General Output: ON
 - Select PAM4-PPG and Emphasis tab- Emphasis Function: ON



- Select the Pattern tab- Test Pattern: Using Preset Q0, with 64x0, 64x10, 64x1
 - Select the Misc1 tab- Aux Output: Pattern Sync
- b) Scope Settings:
- Averaging: 256 points
 - Horizontal Scale: 1 ns/div
 - Bandwidth: 50 GHz
 - Sampling Rate: ≥ 192 GS/s
- c) Preshoot-1, Preshoot-2 and De-emphasis Calibration:
- Set 500 mV (p-p) initial amplitude on BERT, with Preset Q0.
 - On the scope, trigger on the LF and HF of the transmitted signal at the center of the screen. Scale the differential amplitude to cover 80% of the screen.
 - Measure the transmitted signal on the scope using markers/histogram/equivalent for Preshoot-1, Preshoot-2 and De-emphasis.
 - Note the adjusted Tx equalization settings on the BERT. Adjust the Tx equalization to Q0 on the scope.

- Subtract the measured value on the scope with the setup value and save it as an Error value.
- Measure the amplitude of HF and LF and HF/LF ratio.
- Set the Error value to Preset and measure again. Repeat until the measured Preshoot-1, Preshoot-2 and De-emphasis values are obtained at 0 ± 0.3 dB and the HF/LF ratio at 0.9 to 1.1.



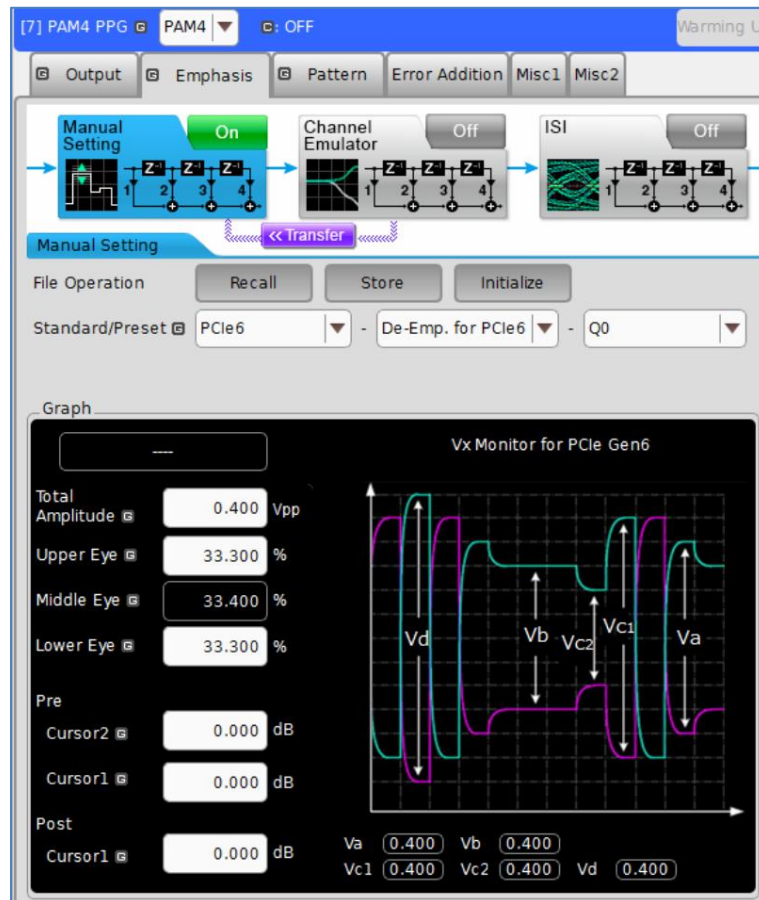
- Save the calibrated Preset Q0 value.

8.1.6 Launch Amplitude Calibration

Adjust the Amplitude with Scope markers to between 790 - 800 mVpp (diff) using the following configuration:

a) BERT Settings:

- General Output: ON
- Select PAM4-PPG and Emphasis tab: Select PCIe6 – De-Emphasis for PCIe6 – Preset Q0



- Select the Pattern tab- Test Pattern: Using Preset Q0, with 64x0, 64x10, 64x1
- Select the Misc1 tab- Aux Output: Pattern Sync

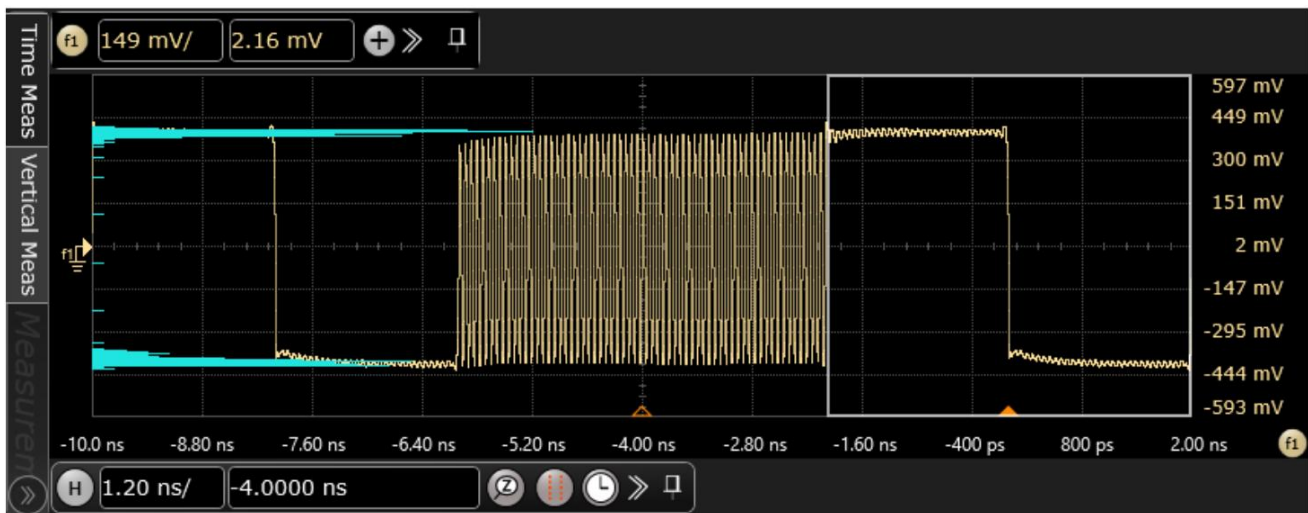
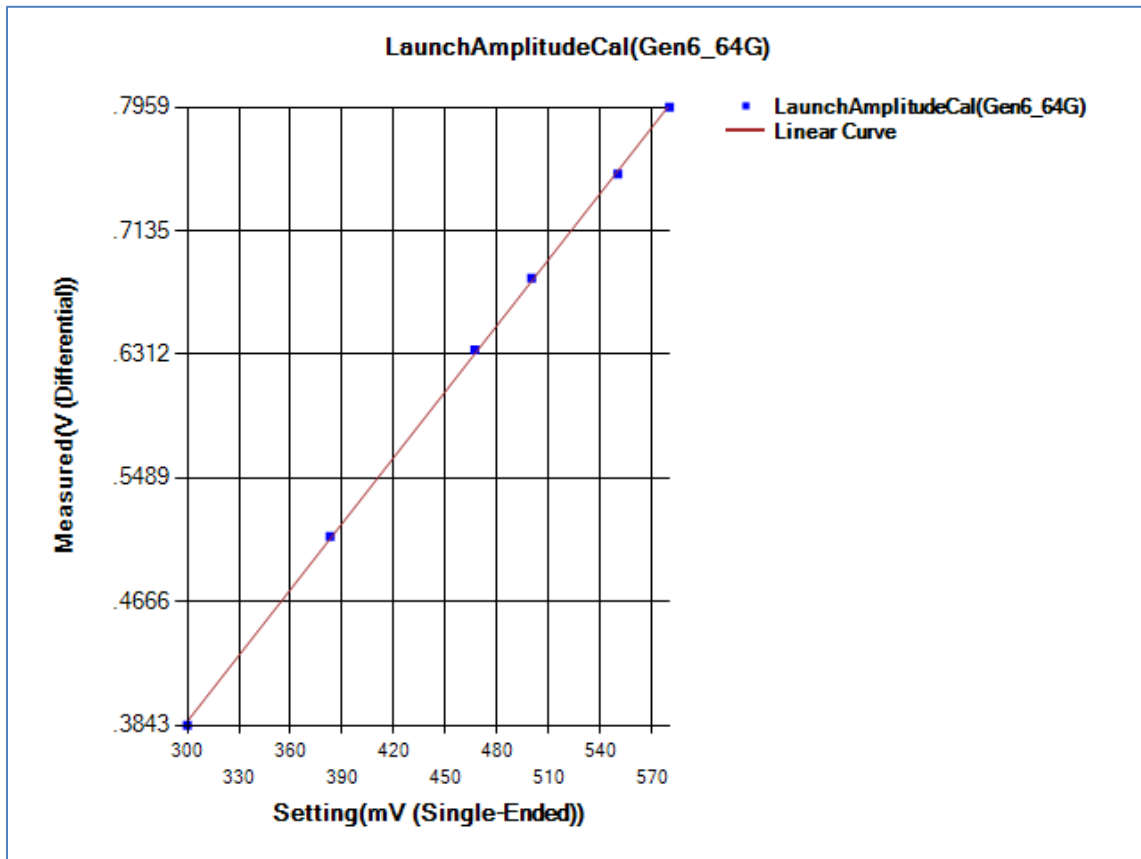
b) Scope Settings:

- Averaging: 256 points
- Horizontal Scale: 100 ns/div
- Bandwidth: 50 GHz
- Sampling Rate: ≥ 192 GS/s

c) Amplitude Calibration:

- Set 500 mV (p-p) initial amplitude on BERT, with the calibrated Preset Q0 saved from the Initial Preset Q0 calibration.
- On the scope, trigger on the LF and HF of the transmitted signal at the center of the screen. Scale the differential amplitude to cover 80% of the screen.
- Measure the transmitted signal on the scope using markers/histogram/equivalent for the LF amplitude.
- Plot a Caltable graph for the measured value versus the setup value.

- Increase the amplitude setting and measure again. Repeat until the measured amplitude is obtained at between 790 to 800 mVpp (diff).



- Save the calibrated amplitude value.

8.1.7 Preset Q1 to Q9 Calibration

Adjust the Pre Cursor1, Pre Cursor2 and Post Cursor1 of Preset Q1 - Q9 with Scope markers to within ± 0.3 dB tolerance using the following configuration:

a) BERT Settings:

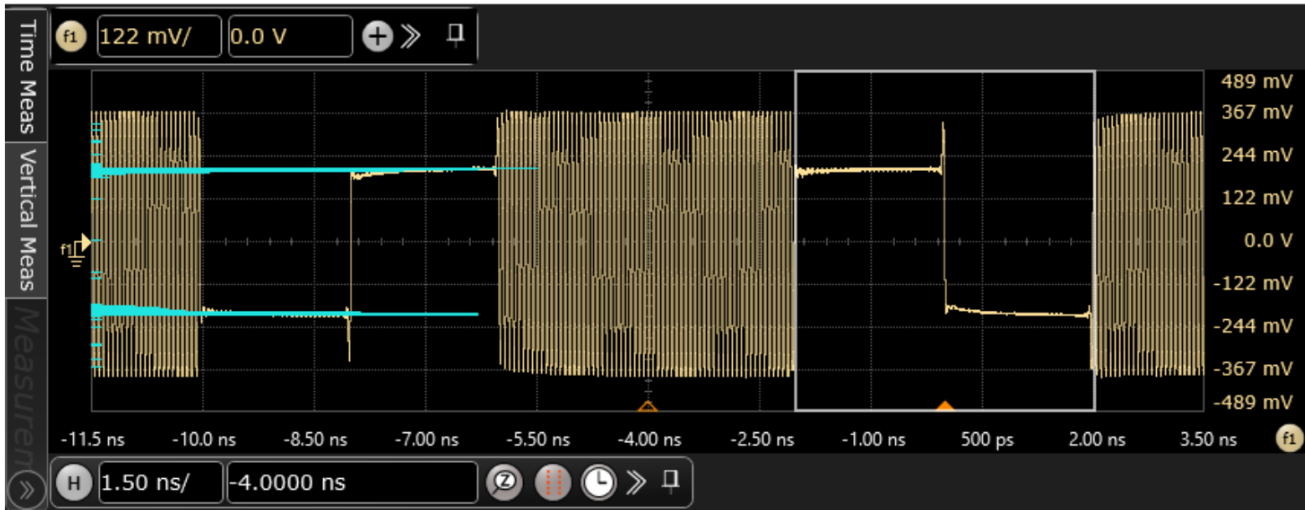
- General Output: ON
- Select PAM4-PPG and Emphasis tab- Emphasis Function: ON
- Select the Pattern tab- Test Pattern: Using Preset Q# with 64x0, 64x10, 64x1
- Select the Misc1 tab- Aux Output: Pattern Sync

b) Scope Settings:

- Averaging: 256 points
- Horizontal Scale: 1 ns/div
- Bandwidth: 50 GHz
- Sampling Rate: ≥ 192 GS/s

c) Preshoot-1, Preshoot-2 and De-emphasis Calibration:

- Set 500 mV (p-p) initial amplitude on BERT, with Preset Q#.
- On the scope, trigger on the LF and HF of the transmitted signal at the center of the screen. Scale the differential amplitude to cover 80% of the screen.
- Measure the transmitted signal on the scope using markers/histogram/equivalent for Preshoot-1, Preshoot-2 and De-emphasis.
- Note the adjusted Tx equalization settings on the BERT. Adjust the Tx equalization to Q# on the scope.
- Subtract the measured value on the scope with the setup value and save it as an Error value.
- Measure the amplitude of HF and obtain the Error value HF versus 0.8 V.
- Set the Error value to Preset and error of amplitude and measure again. Repeat until the measured Preshoot-1, Preshoot-2 and De-emphasis values are obtained within ± 0.3 dB and the HF/0.8 ratio at 5% for Preset Q1 to Q9.
- For example, passing criteria for Preset Q5 is to obtain measured Preshoot-1 at 4.7 ± 0.3 dB, measured Preshoot-2 at -1.3 ± 0.3 dB and measured De-emphasis at 0.0 ± 0.3 dB.



- Save the calibrated Preset Q1 to Q9 values.

8.1.8 BERT Intrinsic Pulse Width Jitter (PWJ) Calibration

Capture data and noise waveforms on the scope and measure PWJ RJ and PWJ DDJ using SigTest. Set up the following parameters.

a) BERT Settings:

- General Output: ON
- Select the Pattern tab- Test Pattern: [Clk] 0303
- Set the Amplitude (based on calibrated value from the Launch Amplitude calibration)
- Set Preset Q0 (based on the calibrated value from the Initial Preset Q0 calibration)
- Set All Stresses to 0 ps/0 mV

b) Scope Settings:

- Averaging: OFF
- Bandwidth: 50 GHz
- Sampling Rate: ≥ 192 GS/s

c) PWJ Calibration:

- On the scope, scale the differential amplitude to cover 80% of the screen.
- Enable 4th order Bessel-Thomson filter with roll-off from DC value by 3 dB at 33 GHz on the scope.
- Capture 3.0 million UI data ($3.0 \times 10^6 \times 31.25$ ps = 93.75 μ s) simultaneously and save the captured waveform.
- Using the same scope settings/scale, terminate the scope Channel 1/Channel 3 with 50 Ω and capture the noise waveform.

- Run SigTest on both the captured data and noise waveforms using the 64.0 GT/s Optimize_CTLE template file (*PCIe* → *6_0* → *Base_TX_w_ClockPattn*).
- Passing criteria is to obtain measured PWJ RJ and PWJ DDJ ($T_{TX-UPW-DJDD}$) at $1e-6$.
- Using the Seasim config file, *CEM_6_0_Seasim_2_0_103f_Config_June18_2025_RX_LEQ.inc*, set the *jit_pwddj* parameter to $T_{TX-UPW-DJDD}$ and the *jit_pwrj* parameter to PW RJ.

8.1.9 RJ Calibration

Capture the waveform on the Scope and measure RJ using SigTest and the Caltable method. Set up the following parameters.

a) BERT Settings:

- General Output: ON
- Select PAM4-PPG and Emphasis tab- Emphasis Function: OFF
- Select the Pattern tab- Test Pattern: [Clk] 3030
- Select Jitter Modulation Source- RJ: ON
- Set the Amplitude (based on calibrated value from the Launch Amplitude calibration)
- Set Preset Q0 (based on the calibrated value from the Initial Preset Q0 calibration)
- Set All Stresses to 0 ps/0 mV

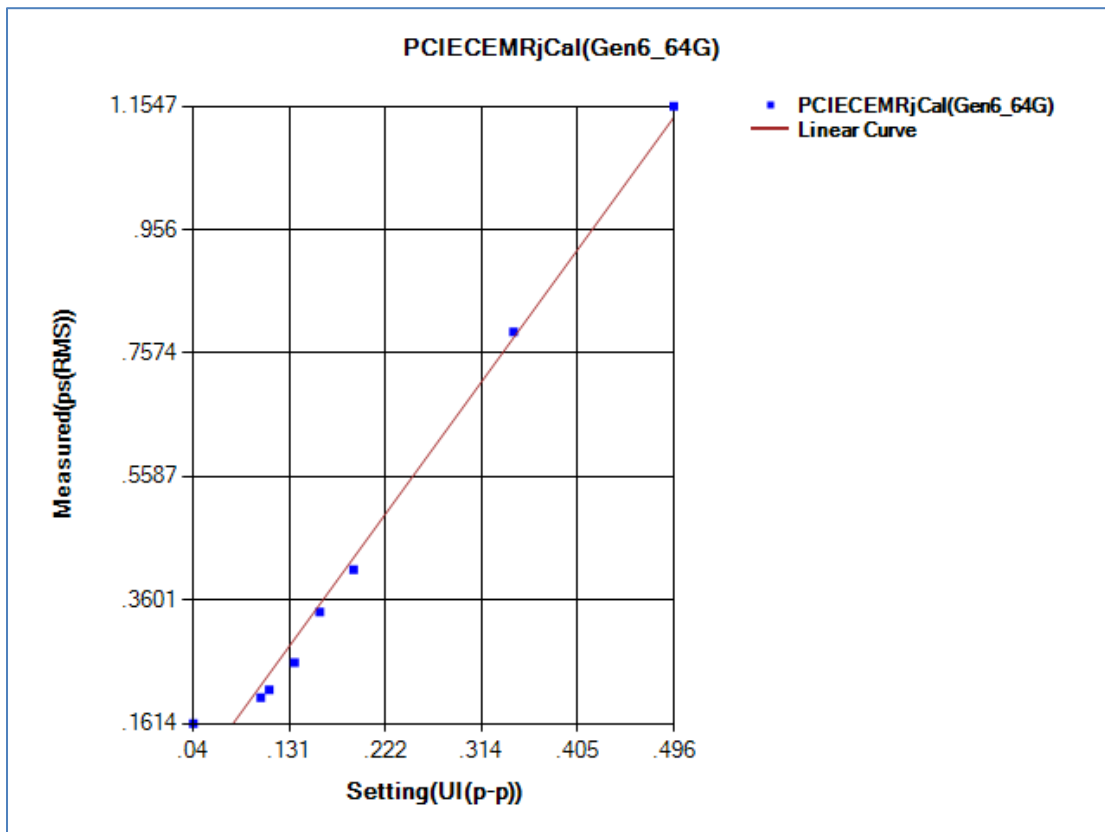
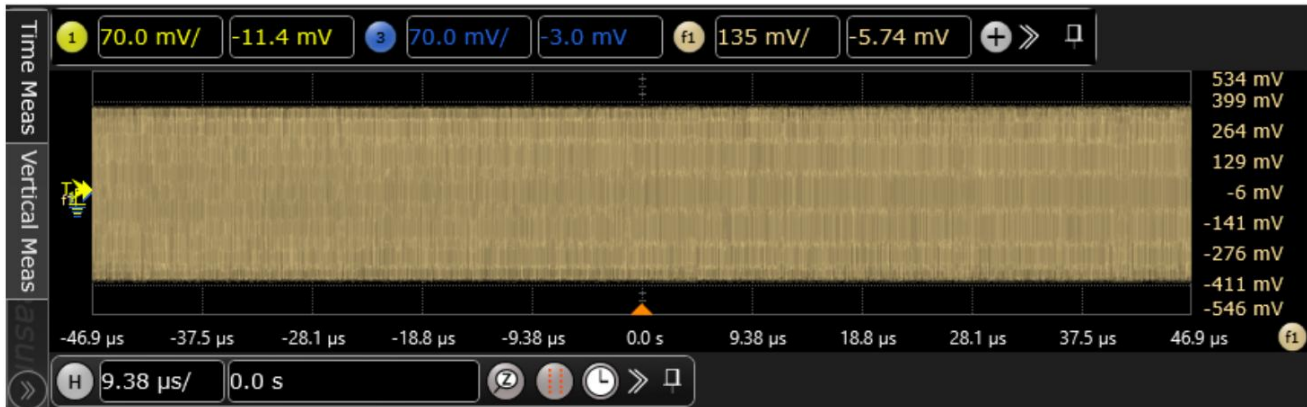
b) Scope Settings:

- Averaging: OFF
- Horizontal Scale: 10 μ s/div
- Bandwidth: 50 GHz
- Sampling Rate: ≥ 192 GS/s

c) Caltable Method:

- On the scope, scale the differential amplitude to cover 80% of the screen.
- Enable 4th order Bessel-Thomson filter with roll-off from DC value by 3 dB at 33 GHz on the scope.
- Adjust the RJ to target ~ 0.25 ps RMS.
- Capture 3.0 million UI data ($3.0 \times 10^6 \times 31.25$ ps = 93.75 μ s) and save the captured waveform.
- Using the same scope settings/scale, terminate the scope Channel 1/Channel 3 with 50 Ω and capture the noise waveform.
- Run SigTest on both the captured data and noise waveforms using the *PCIe* → *6_0* → *CEM_RjCal* template.
- Plot a Caltable graph for the measured value versus setup value.

- Increase the RJ amplitude on each iteration, recapture the waveforms, measure RJ from the scope and plot the Caltable graph, until the measured RJ meets $0.25 + 0.025 / - 0$ ps RMS.



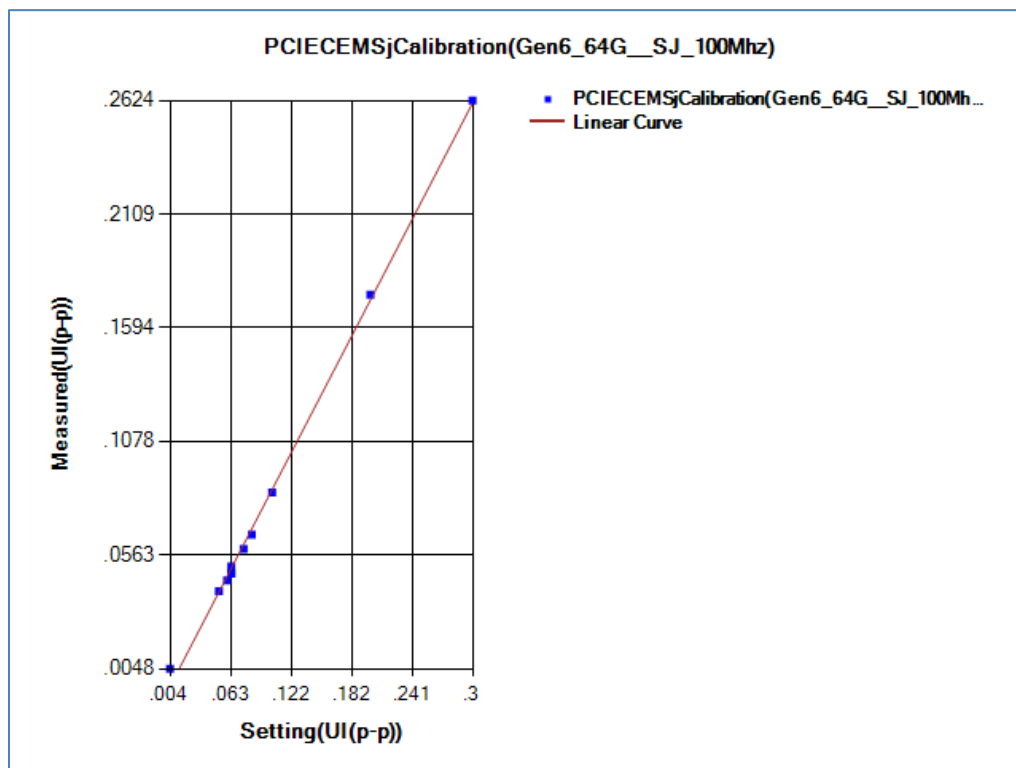
8.1.10 SJ Calibration

Capture three waveforms for both TJ(Base) and TJ(Jittered) and measure SJ using SigTest and the Caltable method. Set up the following parameters.

a) BERT Settings:

- General Output: ON
- Select PAM4-PPG and Emphasis tab- Emphasis Function: OFF

- Select the Pattern tab- Test Pattern: Compliance
 - Set the Amplitude (based on calibrated value from the Launch Amplitude calibration)
 - Set Preset Q0 (based on the calibrated value from the Initial Preset Q0 calibration)
 - Select Jitter Modulation Source- SJ1: ON
 - SJ1 Frequency and Amplitude: 100 MHz, 0.000 UIpp, Measure Total Jitter as TJ(Base)
 - SJ1 Frequency and Amplitude: 100 MHz, 0.050 UIpp, Measure Total Jitter as TJ(Jittered)
 - Set All Stresses to 0 ps/0 mV
- b) Scope Settings:
- Averaging: OFF
 - Horizontal Scale: 10 μ s/div
 - Bandwidth: 50 GHz
 - Sampling Rate: $\geq$ 192 GS/s
- c) Caltable Method:
- On the scope, scale the differential amplitude to cover 80% of the screen.
 - Enable 4th order Bessel-Thomson filter with roll-off from DC value by 3 dB at 33 GHz on the scope.
 - Capture three waveforms with 3.0 million UI data ($3.0 \times 10^6 \times 31.25$ ps = 93.75 μ s) and save the captured waveforms.
 - Run SigTest on the captured waveforms using the *PCIe* $\rightarrow$ 6_0 $\rightarrow$ CEM_SjCal template and check the average Max Peak to Peak Jitter (ps).
 - Adjust the 100 MHz SJ to target $\sim$ 1.5625 ps.
 - Plot a Caltable graph for the measured value versus setup value.
 - Increase the SJ amplitude on each iteration, recapture the waveforms, measure SJ from the scope and plot the Caltable graph. Subtract the average Max Peak to Peak Jitter (ps) from each SigTest analysis until the measured SJ meets $1.5625 + 0.15 / - 0$ ps. Repeat for each SJ frequency using a maximum 0.25 ps step size between 1 ps and 3 ps.
 - Adjust SJ until SJ is between 1 - 3 ps.
 - Disable all jitter and noise sources.



8.1.11 Eye Height/Eye Width and DM & CM Amplitude Calibration Setup

The following connection diagrams show the calibration setups at TP2 for Eye Height (EH)/Eye Width (EW), DM amplitude (DM-I) and CM amplitude (CM-I) for PCIe Gen 6. The CLB/CBB test fixture is connected in between the MP1900A BERT and a digital oscilloscope.

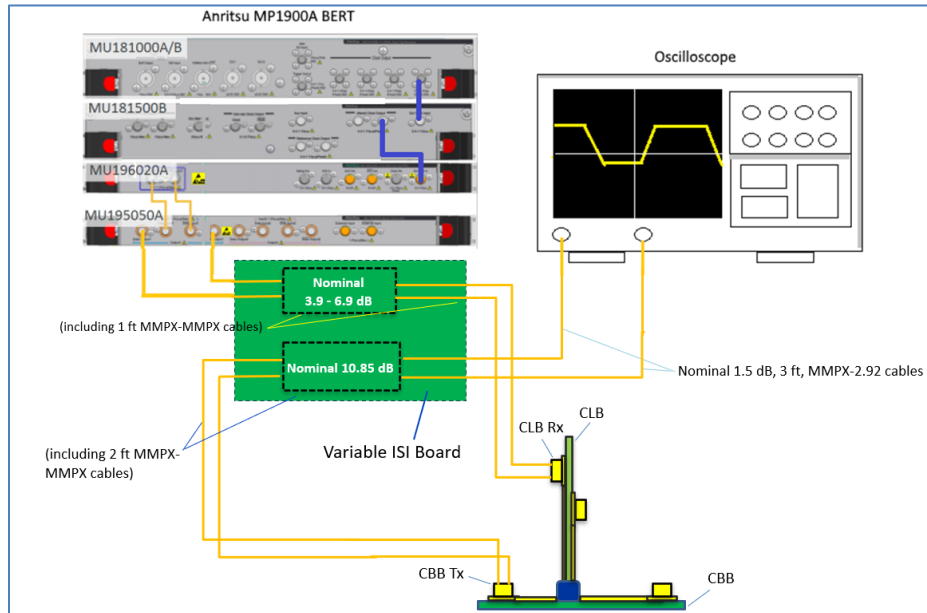


FIGURE 57. CONNECTION DIAGRAM FOR PCIe GEN 6 EH/EW, DM-I AND CM-I TP2 CALIBRATION (FOR SYSTEM BOARD)

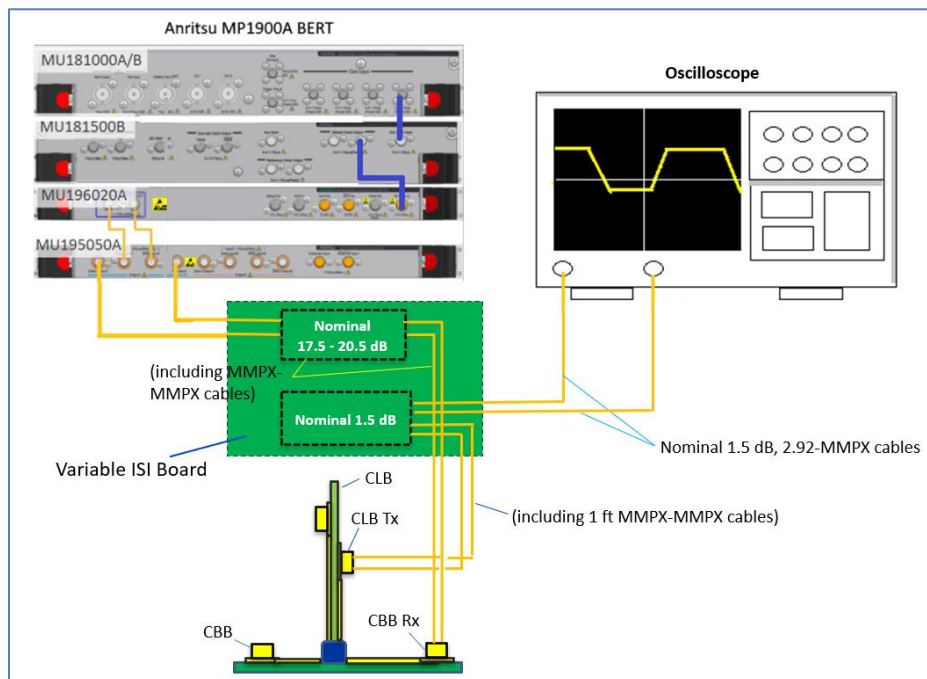


FIGURE 58. CONNECTION DIAGRAM FOR PCIe GEN 6 EH/EW, DM-I AND CM-I TP2 CALIBRATION (FOR ADD-IN CARD)

1. Using a SMA-SMA short cable, connect the MU181000A/B clock output to the MU181500B Ext clock input.
2. Using a SMA-SMA short cable, connect the MU181500B jittered clock output to the MU196020A Ext clock input.
3. Using coaxial cables, connect the MU196020A data outputs to the MU195050A data inputs.
4. For System Board calibration:
 - a) Using coaxial cables, connect the MU195050A data outputs to the Variable ISI (Nominal 3.9 – 6.9 dB trace) of the CLB.
 - b) Connect between both the CLB Rx Lane 0 and CLB Variable ISI (including 1 ft MMPX-MMPX cables) and between both the CBB Tx Lane 0 and CBB Variable ISI (Nominal 10.85 dB trace, including 2 ft MMPX-MMPX cables).
5. For Add-In Card calibration:
 - a) Using coaxial cables, connect the MU195050A data outputs to the Variable ISI (Nominal 17.5 – 20.5 dB trace) of the CBB.
 - b) Connect between both the CBB Rx Lane 0 and CBB Variable ISI (including MMPX-MMPX cables) and between both the CLB Tx Lane 0 and CLB Variable ISI (Nominal 1.5 dB trace, including 1 ft MMPX-MMPX cables).

[Note: DM-I and CM-I should be calibrated with no reference package embedding applied.]

6. Connect the CLB Variable ISI (for add-in card) to the digital Scope channels using Nominal 1.5 dB, 2.92-MMPX cables.
7. Connect the CBB Variable ISI (for system board) to the digital Scope channels using Nominal 1.5 dB, 3 ft, MMPX-2.92 cables.

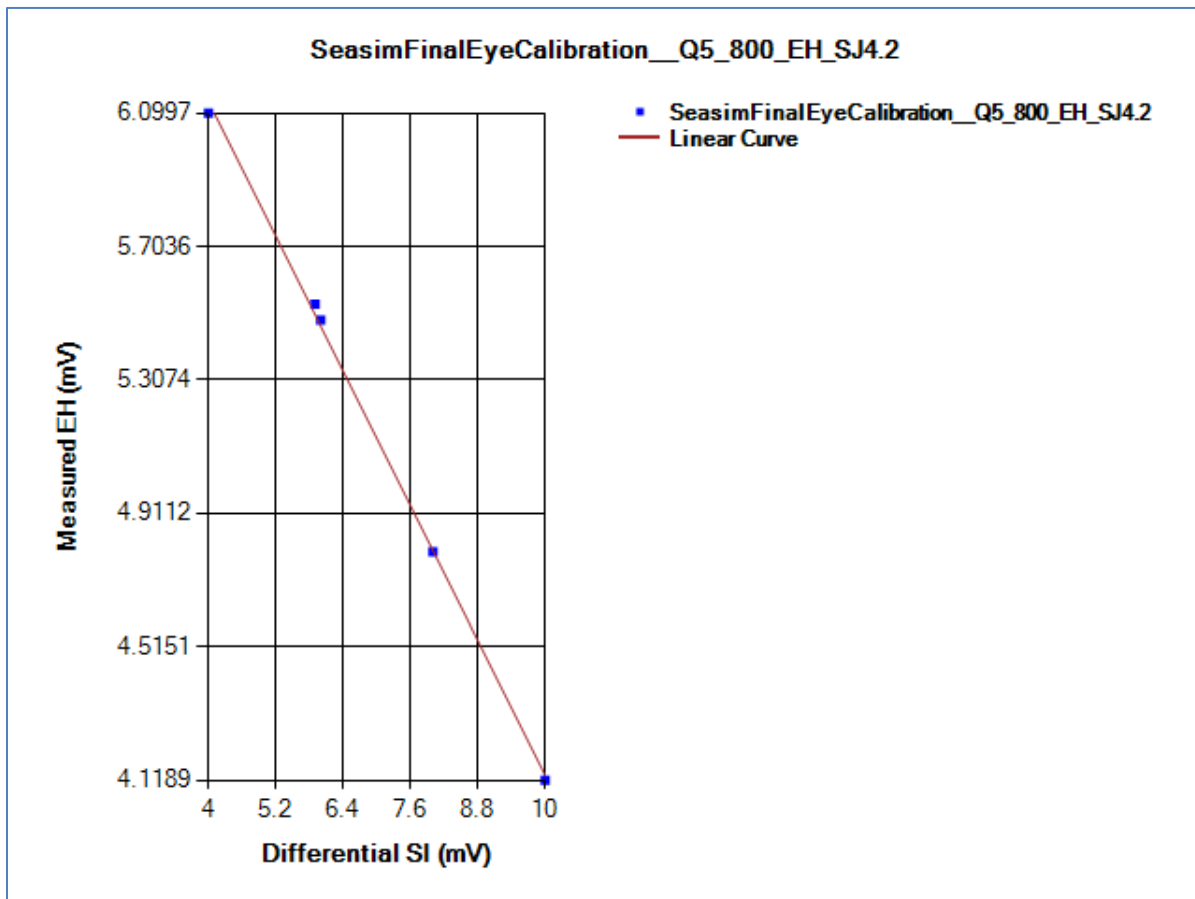
8.1.12 EH/EW Calibration

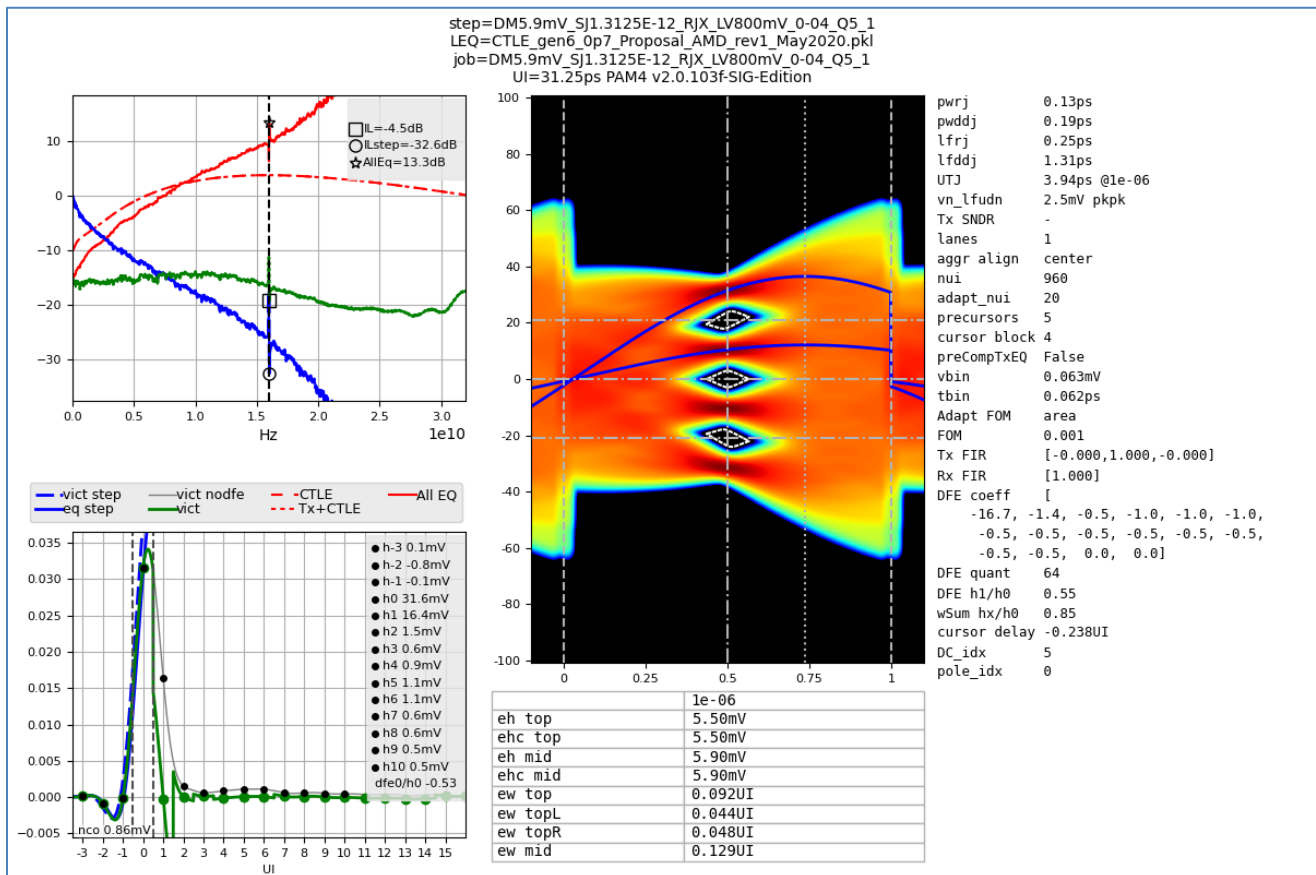
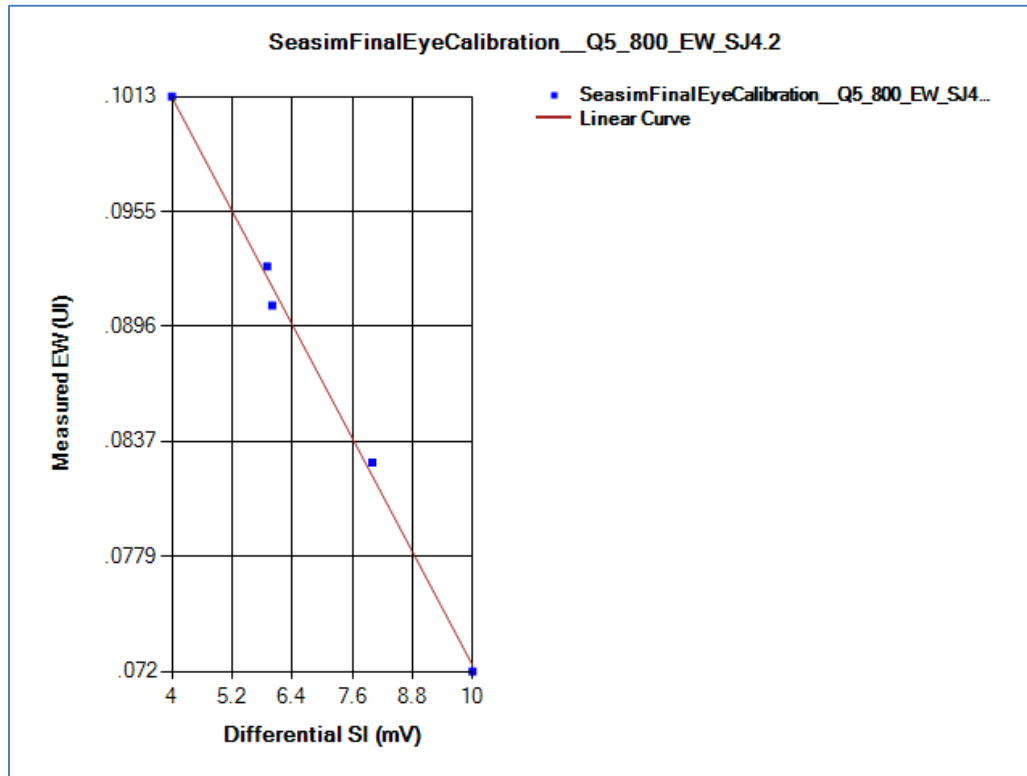
This calibration is to ensure that the waveform achieves the calibrated eye width and eye height.

- a) BERT Settings:
 - General Output: ON
 - Select PAM4-PPG and Emphasis tab- Emphasis Function: OFF
 - Select the Pattern tab- Test Pattern: Clk/1024 Pattern
 - Set the Amplitude (based on calibrated value from the Launch Amplitude calibration)
 - Set Preset Q5 (based on the calibrated value from the Preset Q1 to Q9 calibration)
 - SJ Frequency and Amplitude: 100 MHz, 0 ps
 - RJ Amplitude: 0 ps
 - DM-I & CM-I Amplitude: 0 mV
- b) Scope Settings:
 - Bandwidth: 50 GHz

- Sampling Rate: ≥ 192 GS/s
 - Averaging: 10000
- c) Caltable Method:
- Start with ISI traces of 33 dB.
 - Disable the Bessel-Thomson filter on the scope.
 - On the scope Channel 1 and Channel 3, set autoscale to 80% of screen. Set the horizontal scale to display the Step Response waveform on the screen.
 - Capture the step response/step rising edge (32 ns step) waveform on the scope. Set the rising edge within the first graticule, to the far left of the scope screen and capture 20UI's before the rising edge. Adjust the vertical scale so that the step amplitude is maximized without clipping.
 - Save the step and capture at least five repetitions for Preset Q5.
 - Run Seasim ver 2.0.103f with the *CEM_6_0_Seasim_2_0_103f_Config_June18_2025_RX_LEQ.inc* config file (from the BERT Intrinsic Pulse Width Jitter (PWJ) calibration) and step response:
 - with initial modified DM at TP2P for 5 mV
 - SJ = 0.1 UI
 - with CTLE range of 9 dB to 15 dB
 - PWJ DDJ and PWJ RJ
 - RJ = Specs value
 - Read and save the eye height (EH) and eye width (EW).
 - Change the Preset on the BERT to Preset Q6 (based on the calibrated value from the Preset Q1 to Q9 calibration), run Seasim again, obtain and save the EH and EW.
 - Change the Preset on the BERT to Preset Q9 (based on the calibrated value from the Preset Q1 to Q9 calibration), run Seasim again, obtain and save the EH and EW.
 - Identify the preset with the largest eye area (EH * EW) (optimal preset) and record the corresponding CTLE.
 - Set the optimal preset on the BERT.
 - Capture the step response waveform on the scope.
 - Run Seasim with the *CEM_6_0_Seasim_2_0_103f_Config_June18_2025_RX_LEQ.inc* config file and step response:
 - with initial modified DM at TP2P for 10 mV
 - SJ = 0.1 UI
 - with CTLE range of 9 dB to 15 dB
 - PWJ DDJ and PWJ RJ

- RJ = Specs value
- Sweep the DM of 2 mV resolution (min DM is 5 mV), and SJ of 0.08 UI resolution.
- Plot the Caltable graph and repeat method to obtain EH and EW by adjusting DM/SJ.
- If EH and EW do not fall within 6 mV (top eye height: 6 mV $\pm$ 0.5 mV) and 0.1 UI (top eye width: 3.125 ps $\pm$ 0.3 ps) respectively after DM/SJ adjustments, reduce ISI by 0.5 dB up to 30 dB and repeat the above steps.
- If EH and EW still do not fall within specifications, return to the starting ISI trace of 33 dB while adjusting Amplitude and reducing ISI if necessary.
- Repeat until EH and EW fall within specifications.
- Record the measured Amplitude, SJ and DM values.





8.1.13 DM-I Calibration Adjustment

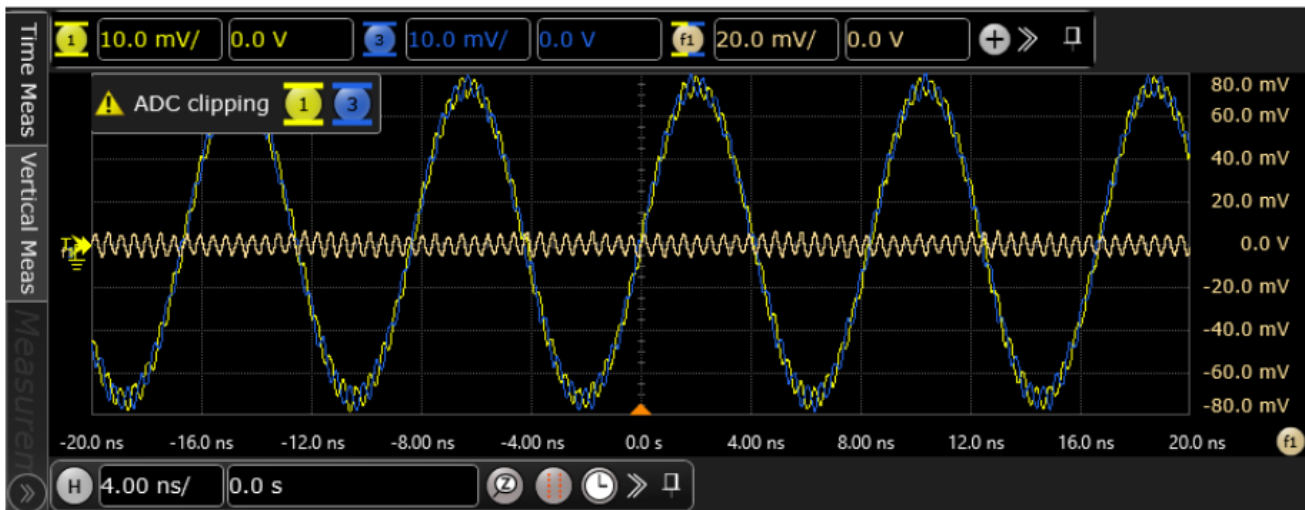
Adjust the DM Amplitude using the Scope RMS function with the following configuration. Compute $V_{\text{Diff}} = (\text{RMS} * 2)/0.707$.

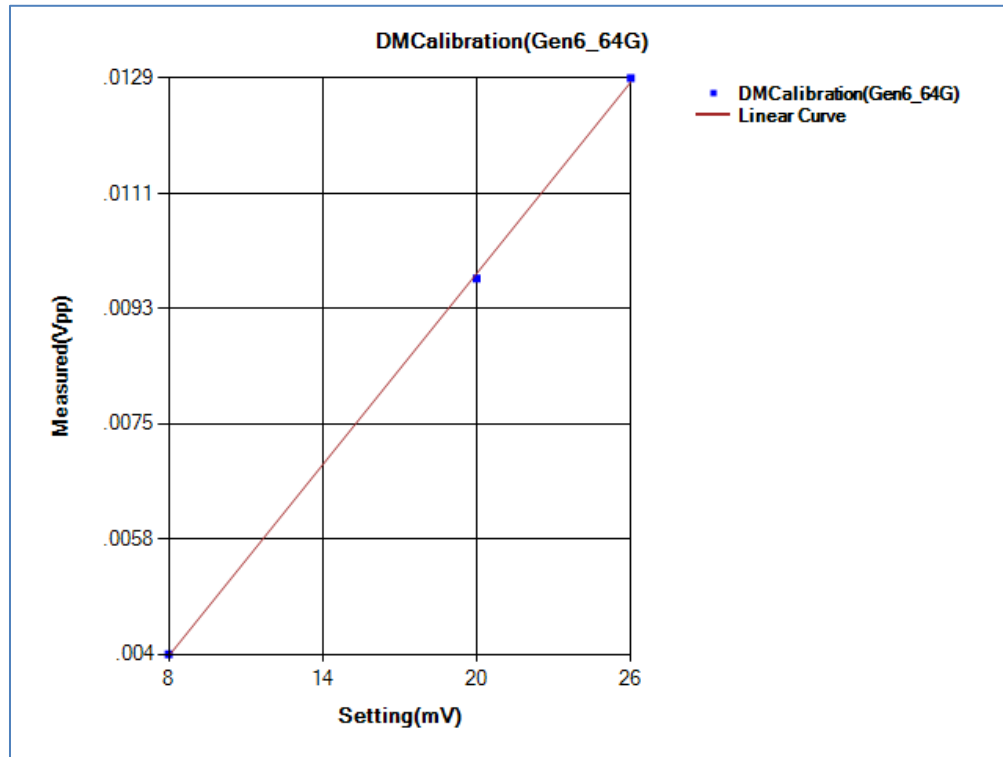
a) BERT Settings:

- Loss Channel
- General Output: ON
- Select PAM4-PPG and Emphasis tab
- PPG Data Output: OFF
- Select Noise Generator- DM: ON
- Differential mode noise Amplitude and Frequency: 0 mV and 2.1 GHz
- Set the Amplitude (based on calibrated value from the Launch Amplitude calibration)
- Set Preset Q0 (based on the calibrated value from the Initial Preset Q0 calibration)
- SJ & RJ: 0 ps

b) Scope Settings:

- Averaging: OFF
- Bandwidth: 50 GHz



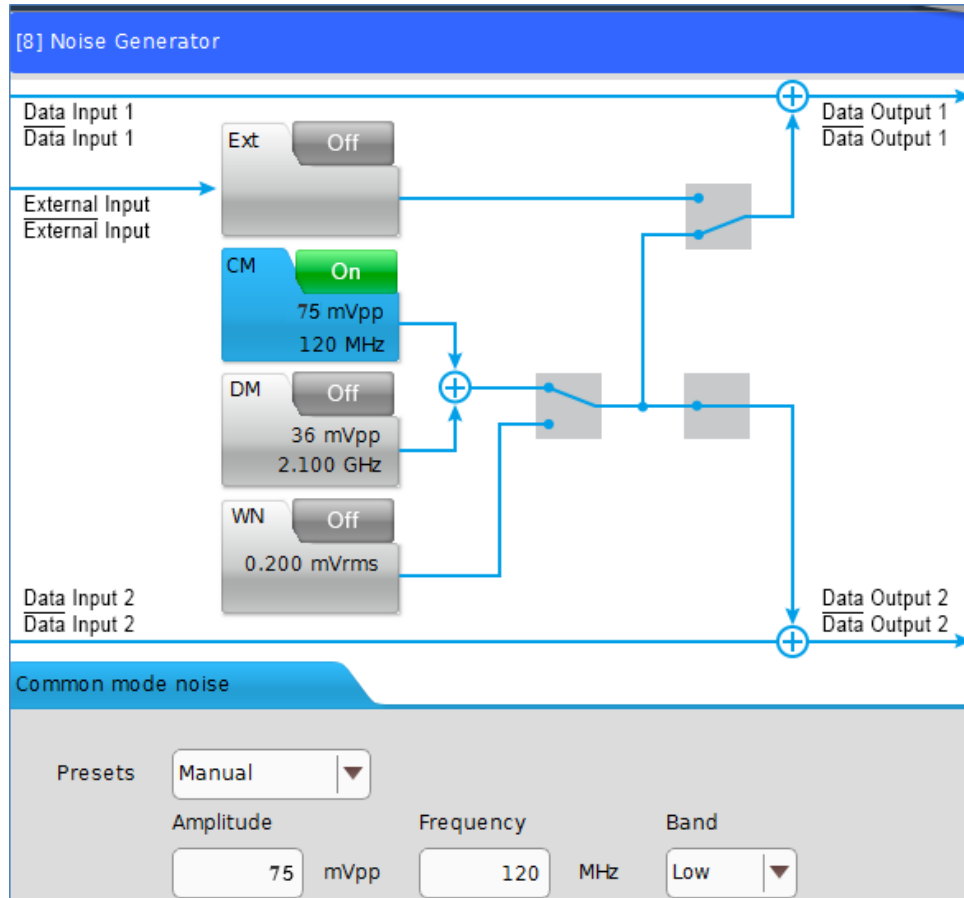


8.1.14 CM-I Calibration Adjustment

Adjust the CM Amplitude using the Scope RMS function with the following configuration. Compute $V_{pp} = \text{RMS}/0.707$.

a) BERT Settings:

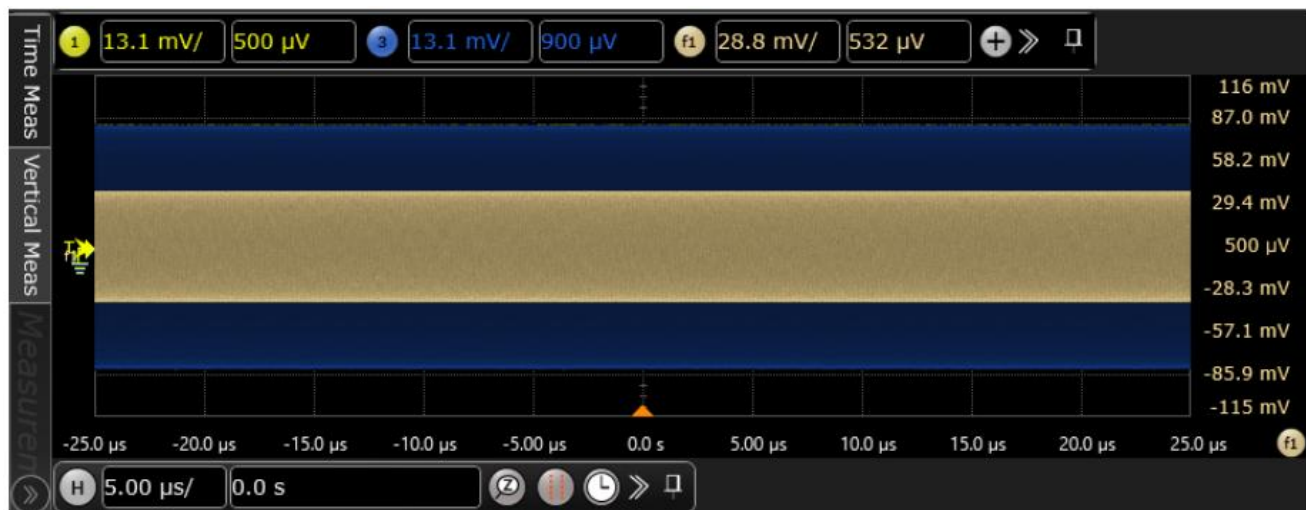
- Loss Channel
- General Output: ON
- Select PAM4-PPG and Emphasis tab
- PPG Data Output: OFF
- Select Noise Generator- CM: ON
- Common mode noise Amplitude and Frequency: 75 mVpp and 120 MHz
- Set the Amplitude (based on calibrated value from the Launch Amplitude calibration)
- Set Preset Q0 (based on the calibrated value from the Initial Preset Q0 calibration)
- SJ & RJ: 0 ps

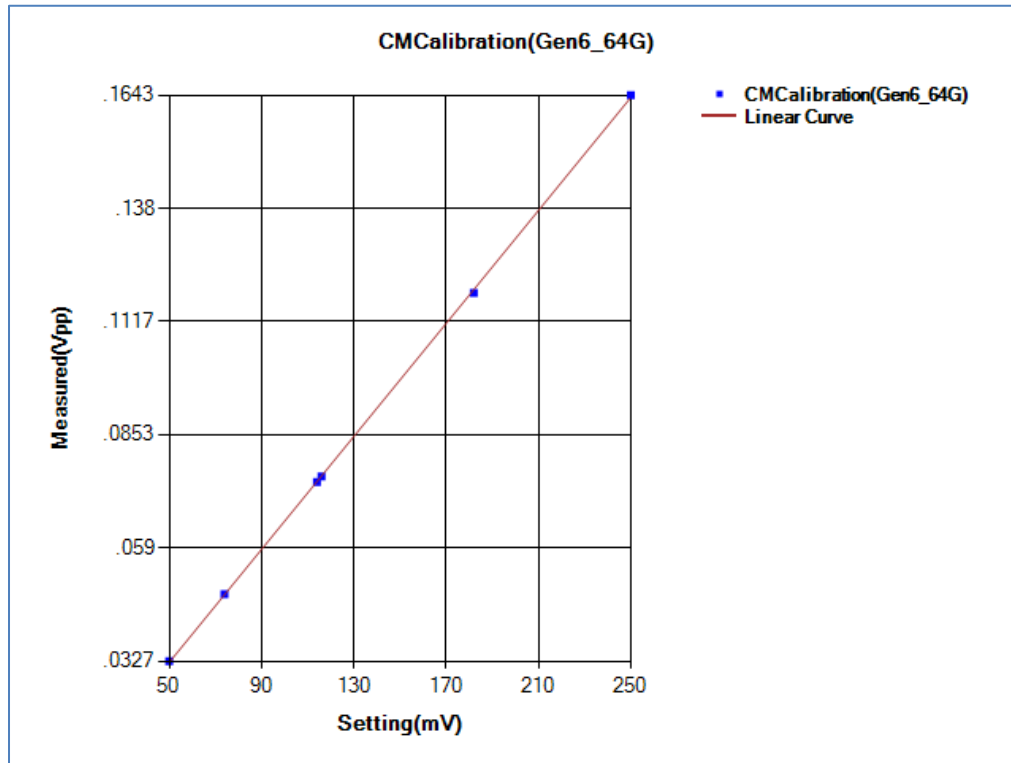


b) Scope Settings:

- Averaging: OFF
- Bandwidth: 50 GHz

Measure RMS on (CH1+CH3)/2 and calculate $V_{pp} = \text{RMS} / 0.707$.





8.2 Perform Initial Tx Equalization & Tx Link Equalization Response Tests

This section describes how to set up the DUT to perform initial Tx equalization (EQ) testing (for the add-in card only) and Tx link EQ response testing (for both the system board and add-in card). This is to ensure that the DUT will be able to apply the correct Tx EQ preset as required during the test.

To perform the initial Tx EQ & Tx link EQ response tests, the DUT attached to a test fixture will basically receive data signals from a stress signal generator which is also connected to a reference clock with the DUT fixture. After data is processed, the signals will be separated to flow through two different directions— one part of the signal will be sent back through the test fixture to the stress signal generator for error detection while the other part will be sent to the oscilloscope for waveforms to be captured and analyzed for target EQ values.

Note: Refer to Sections 5.2 and 5.3 for more details on the test setup requirements for the DUT.

8.2.1 Equipment Setup for Add-in Card DUT Initial Tx EQ / Tx Link EQ Response Test

The following connection diagram shows the physical setup to perform initial Tx EQ / Tx link EQ response test for the PCIe Gen 6 add-in card DUT. The setup requires the Anritsu MP1900A BERT (including the MU196040B PAM4 Error Detector), MU196060A Re-Driver, oscilloscope and a compliant CBB test fixture for the DUT.

Note: Use logical Lane 0 for the following test setup.

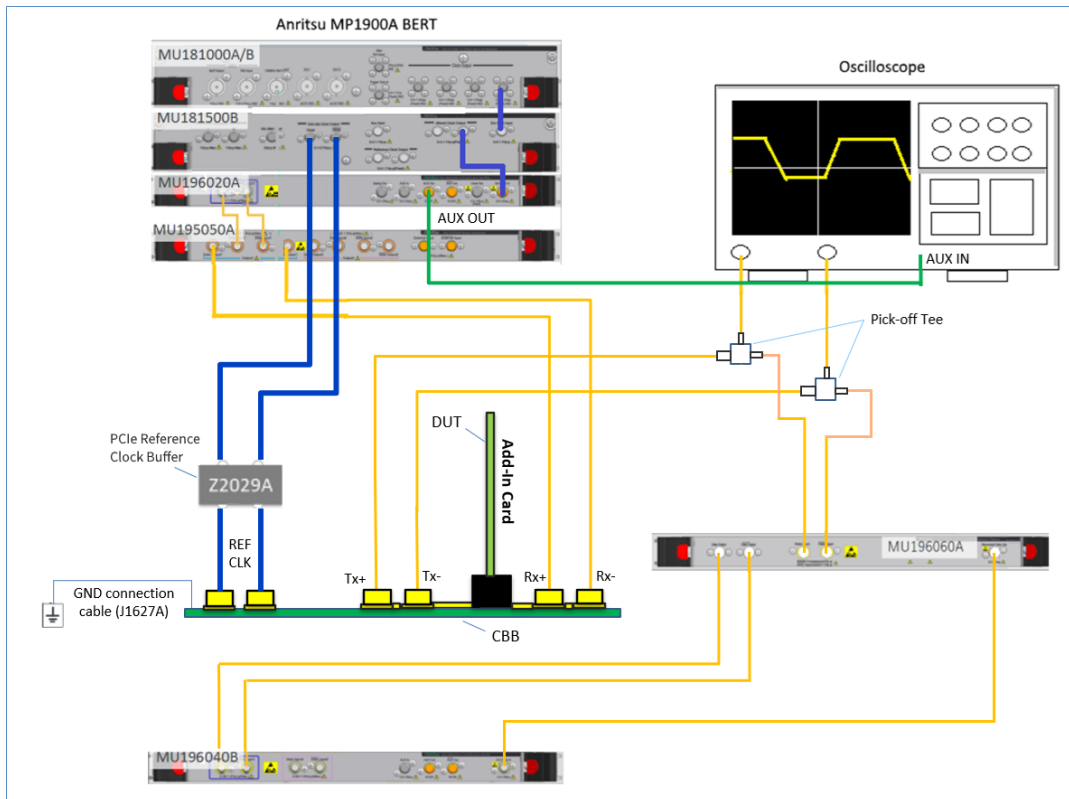


FIGURE 59. CONNECTION DIAGRAM FOR PCIe GEN 6 ADD-IN CARD DUT INITIAL TX EQ / TX LINK EQ RESPONSE TEST

Note: Before starting the add-in card initial Tx EQ / Tx link EQ response test, make sure to perform optimization of the Return Path (DUT Tx to BERT error detector). Refer to Section 9, Appendix B: Return Path Optimization Using Anritsu MU196060A Re-Driver for more details.

1. Using back the same BERT connections from the Long Channel add-in card calibration (Figure 58), remove all Variable ISI channels.
2. Using coaxial cables, connect the MU181500B sub-rate clock outputs to the Ref Clk+/- of the CBB through a Z2029A PCIe reference clock buffer.
3. Using a SMA cable, connect a MU196020A Aux Out connector to an Aux input on the oscilloscope. *Note the other unused MU196020A Aux Out connector must be terminated with the J1632A coaxial terminator due to differential signal output (not shown in above setup).*
4. Using phase matched cables, connect the oscilloscope channels to the pick-off tee PICK OFF ports.
5. Using coaxial cables, connect the CBB Tx Lanes to the pick-off tee IN ports.
6. Using coaxial cables, connect the pick-off tee OUT ports to the MU196060A Re-Driver data inputs.
7. Connect the MU196060A Re-Driver data outputs to the MU196040B data inputs for loopback error detection.
8. Connect the MU196060A Re-Driver clock output to the MU196040B Ext Clock in.

9. Using the J1627A GND connection cable, connect the CBB to ground.

8.2.2 Equipment Setup for System Board DUT Tx Link EQ Response Test

The following connection diagram shows the physical setup to perform Tx link EQ response test for the PCIe Gen 6 system board DUT. The setup requires the Anritsu MP1900A BERT (including the MU196040B PAM4 Error Detector), MU196060A Re-Driver, oscilloscope and a compliant CLB test fixture for the DUT.

Note: Before starting the System Board TxRx Link EQ Test, make sure to perform optimization of the Return Path (DUT Tx to BERT error detector). Refer to Section 9, Appendix B: Return Path Optimization Using Anritsu MU196060A Re-Driver for more details.

Note: A Re-Driver may be required for System DUT testing. The return path of the Re-Driver needs to be optimized. The procedure for optimizing the Re-Driver return path is described in the manual at the link below:

<https://dl.cdn-anritsu.com/en-en/test-measurement/files/Application-Notes/Application-Note/mp1900a-pcie6-ef1500.pdf>

Note: Use logical Lane 0 for the following test setup.

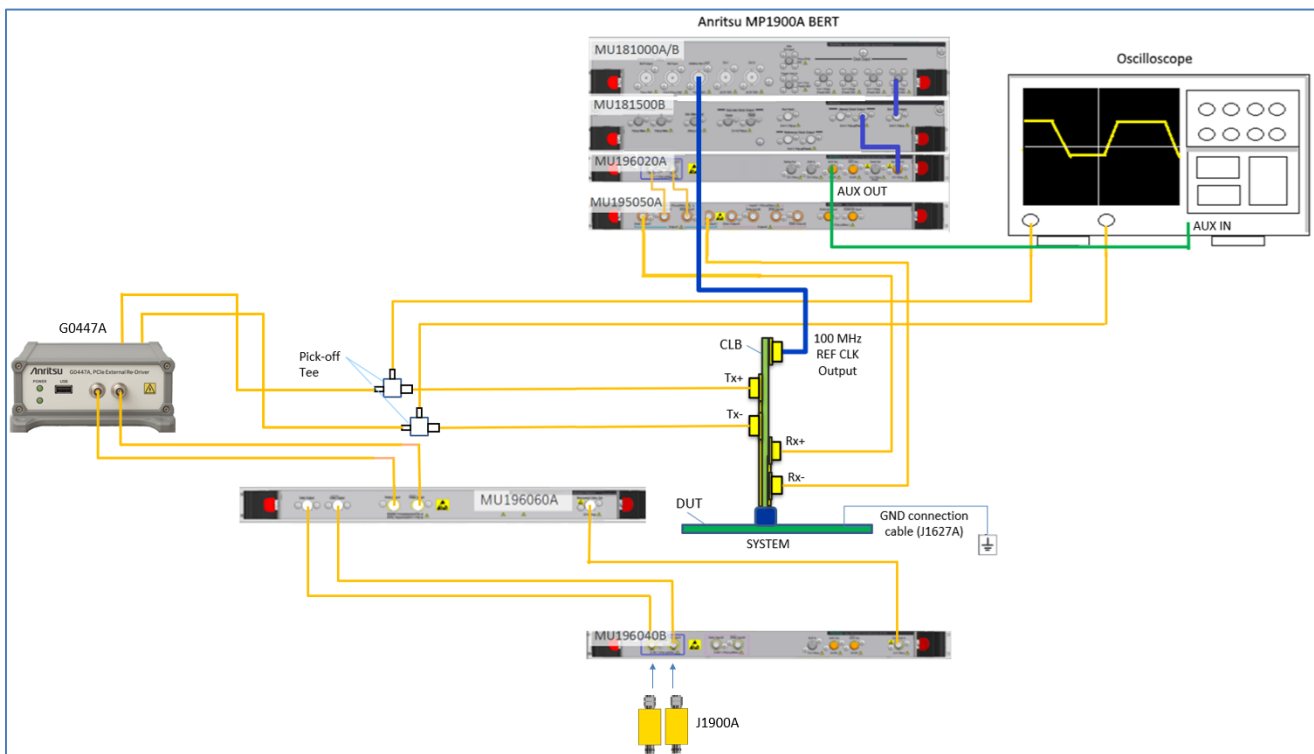


FIGURE 60. CONNECTION DIAGRAM FOR PCIe GEN 6 SYSTEM BOARD DUT TX LINK EQ RESPONSE TEST

1. Using back the same BERT connections from the Long Channel system board calibration (Figure 57), remove all Variable ISI channels and connect the Ref Clk of the CLB to the 100 MHz Ref Input on the MU181000A/B with a BNC cable.
2. Using a SMA cable, connect a MU196020A Aux Out connector to an Aux input on the oscilloscope. *Note the other unused MU196020A Aux Out connector must be terminated*

with the J1632A coaxial terminator due to differential signal output (not shown in above setup).

3. Using coaxial cables, connect the CLB Tx Lanes to the pick-off tee IN ports.
4. Using phase matched cables, connect the oscilloscope channels to the pick-off tee PICK OFF ports.
5. Using coaxial cables, connect the pick-off tee OUT ports to the G0447A external PCIe6 Re-Driver data inputs.
6. Using the J1789A coaxial cables, connect the G0447A data outputs to the MU196060A Re-Driver data inputs.
7. Connect the MU196060A Re-Driver data outputs to the MU196040B data inputs for loopback error detection.
8. Connect the J1900A passive low frequency equalizer to the MU196040B data inputs.
9. Connect the MU196060A Re-Driver clock output to the MU196040B Ext Clock in.
10. Using the J1627A GND connection cable, connect the CLB to ground.

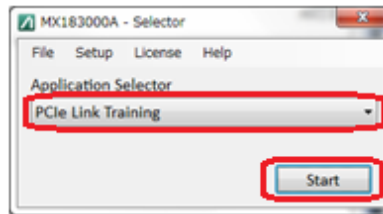
8.2.3 Initial Tx EQ Startup and Testing

The Anritsu MX183000A High-Speed Serial Data test software is used with the MX190000A test application on the MP1900A BERT to perform the initial Tx EQ test. The oscilloscope will also be used to capture waveforms for post processing analysis.

1. Configure the oscilloscope as follows:
 - Averaging: OFF
 - Horizontal Scale: 6.25 μ s/div (2M UI)
 - Bandwidth: 50 GHz
 - Sampling Rate: $\geq$ 192 GS/s
 - Trigger: 0 V, Channel 1
2. Set Preset Q0 on the BERT.
3. On the BERT's Applications screen, select the MX183000A Utility application.



4. In the MX183000A – Selector pop-up, select 'PCIe Link Training' and then 'Start'.



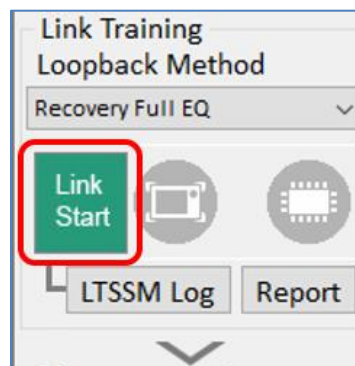
5. In the next window, select the network address of the MX190000A BERT application followed by 'Connect' to link up with the MX190000A.



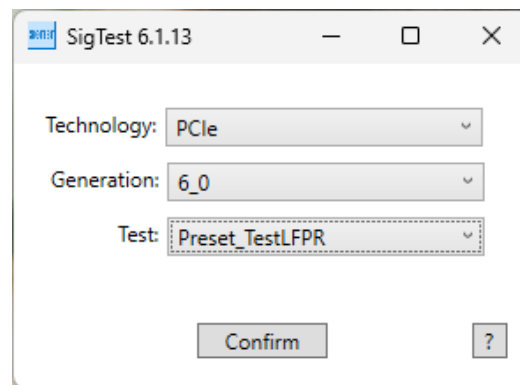
6. In the MX183000A – PCIe Link Training window, select the 'Link Training' tab.
7. In the LEQ Test pane, select the 'Initial TX LEQ' tab. Set the "DUT Initial Preset (Preset Hint Tx)" to Preset 0 (Q0). Then select "Apply".
8. Press the Power Reset button on the CBB test fixture to reset the DUT.



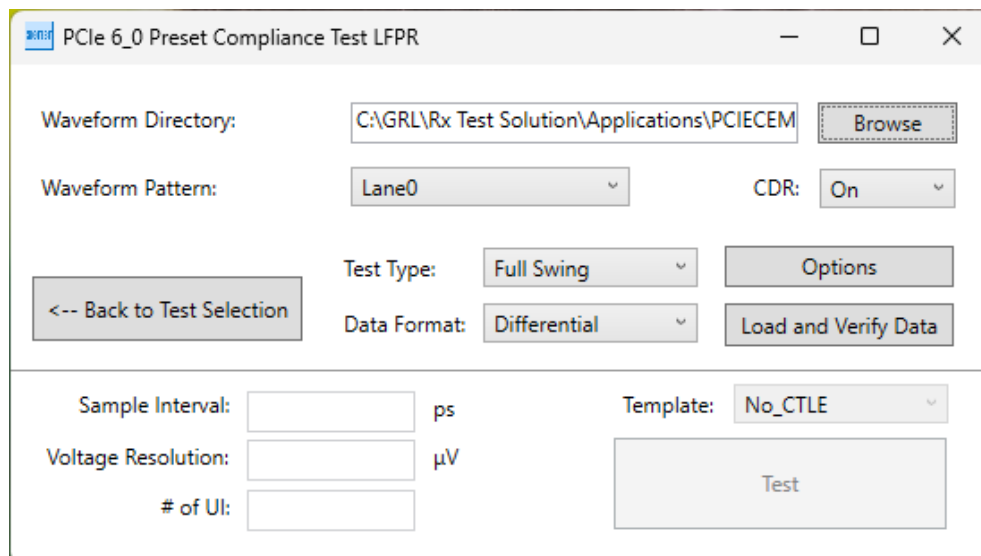
9. In the MX183000A – PCIe Link Training window, select "Link Start" under 'Link Training'.



10. On the Scope, capture the Preset Q0 waveforms and save to a file labeled as either “Add In Card_Ln00_TXResponse_Q0X_d_acq000” (for the add-in card where Q0X represents the Preset Number) or “System Board_TXResponse_Q0_d_acq000” (for the system board). For example, if using an add-in card DUT, the Preset 0 waveform should be saved as “Add In Card_Ln00_TXResponse_Q00_d_acq000”. If using a system board DUT, the Preset 0 waveform should be saved as “System Board_TXResponse_Q0_d_acq000”.
11. Repeat steps 1 to 9 to capture all waveforms for all Presets (up to Preset Q9). All waveforms must be saved to the same file directory.
12. Launch SigTest and select the “PCIe Gen6 Preset Test” (PCIe -> 6_0 -> Preset_TestLFPR).



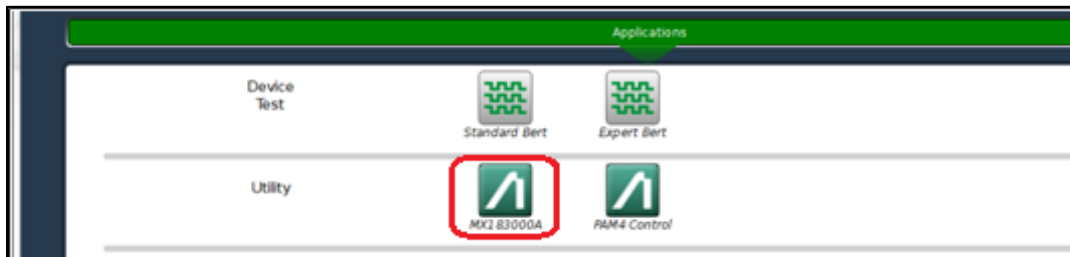
13. Browse to select the directory of the saved waveform file to be tested and select “No_CTLE” at the Template drop-down field. Then select the “Test” button at the bottom to start the test run. All preset numbers must turn green once the test is completed to indicate a Pass.



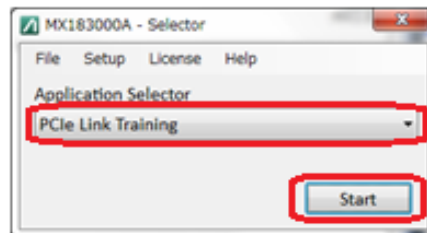
8.2.4 Tx Link EQ Time Response (with Presets/Cursors) Startup and Testing

The Anritsu MX183000A High-Speed Serial Data test software is used with the MX190000A test application on the MP1900A BERT to perform the Tx link EQ time response test with presets or cursors. The oscilloscope will also be used to capture waveforms for post processing analysis.

1. Configure the oscilloscope as follows:
 - Averaging: OFF
 - Horizontal Scale: 6.25 μ s/div (2M UI)
 - Bandwidth: 50 GHz
 - Sampling Rate: $\geq$ 192 GS/s
 - Trigger: -350 mV, Anritsu AUX channel
2. Set Preset 0 on the BERT.
3. On the BERT's Applications screen, select the MX183000A Utility application.



4. In the MX183000A – Selector pop-up, select 'PCIe Link Training' and then 'Start'.



4. In the next window, select the network address of the MX190000A BERT application followed by 'Connect' to link up with the MX190000A.



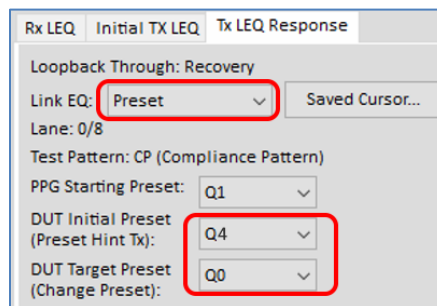
5. In the MX183000A – PCIe Link Training window, select the 'Link Training' tab.

- In the LEQ Test pane, select the 'Tx LEQ Response' tab. Set 'DUT Initial Preset (Preset Hint Tx)' to 'Preset 4 (Q4)' and the "DUT Target Preset (Change Preset)" to Q0.

Note: Use the following "DUT Initial Preset (Preset Hint Tx)" and "DUT Target Preset (Change Preset)" combinations for this step:

Preset # to be Tested	DUT Initial Preset (Preset Hint Tx)	DUT Target Preset (Change Preset)
Q0	Q4	Q0
Q1	Q4	Q1
Q2	Q4	Q2
Q3	Q7	Q3
Q4	Q7	Q4
Q5	Q7	Q5
Q6	Q7	Q6
Q7	Q4	Q7
Q8	Q4	Q8
Q9	Q7	Q9

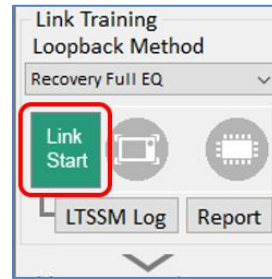
Set Link EQ to "Preset" if testing for Tx Response Preset or "Cursor" if testing for Tx Response Cursor.



- Press the Power Reset button on the CBB test fixture to reset the DUT.



- In the MX183000A – PCIe Link Training window, select "Link Start" under Link Training.



9. On the Scope, capture the Preset Q0 waveforms and save to a file labeled as either “Add In Card_Ln00_TXResponse_Q0X_d_acq000” (for the add-in card where Q0X represents the Preset Number) or “System Board_TXResponse_Q0_d_acq000” (for the system board). For example, if using an add-in card DUT, the Preset 0 waveform should be saved as “Add In Card_Ln00_TXResponse_Q00_d_acq000”. If using a system board DUT, the Preset 0 waveform should be saved as “System Board_TXResponse_Q0_d_acq000”.
10. Repeat steps 1 to 8 for each Preset change.
11. Repeat steps 1 to 9 for each Cursor change.
12. Perform post processing analysis for each waveform to locate the transition time between the preset/cursor change.
13. Verify that the Electrical transition time is < 1 μ s to pass the test.

8.3 Perform Rx Link EQ Test

This section describes how to set up the DUT for loopback testing to measure the First Bit Error Rate (FBER) using the link equalization test method.

To perform link training loopback tests, the DUT attached to a test fixture will basically receive data signals from a stress signal generator which is also connected to a reference clock with the DUT fixture. After the data is processed, the signals will be sent back through the test fixture to the stress signal generator for error detection. To enable this loopback mode, the error detector on the stress signal generator will run link training procedure on the DUT. When the DUT enters the loopback state, the error detector will proceed to measure FBER of the loopback signals.

Note: Refer to Section 5.5 to set up the DUT for link equalization testing to verify initially that the DUT is ready for link training and loopback.

8.3.1 Equipment Setup for Add-in Card DUT Loopback Test

The following connection diagram shows the physical setup to enable loopback to perform link training for the PCIe Gen 6 add-in card DUT. This setup is using the MP1900A BERT that includes the MU196040B PAM4 Error Detector module, MU196060A Re-Driver and a compliant CBB test fixture for the DUT.

Note: Use logical Lane 0 for the following test setup.

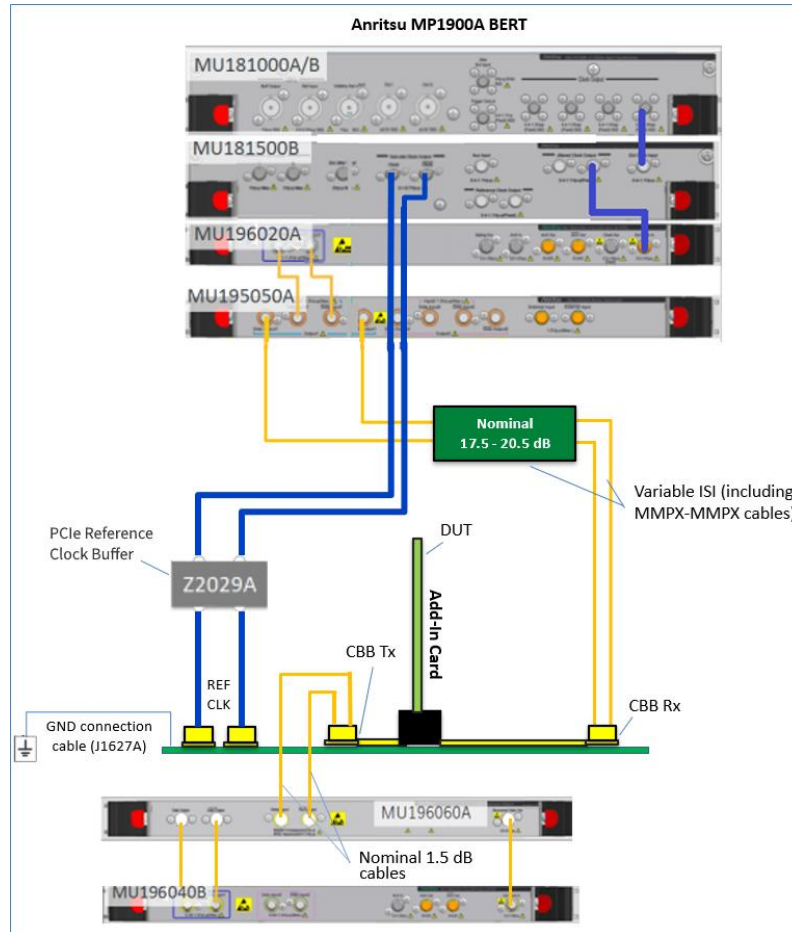


FIGURE 61. CONNECTION DIAGRAM FOR PCIe GEN 6 ADD-IN CARD DUT LOOPBACK TEST

1. Using the same setup from the add-in card link EQ test (Figure 59), remove all oscilloscope connections along with the pick-off tees.
2. Connect the MU195050A data outputs to the Variable ISI board (Nominal 17.5 – 20.5 dB trace).
3. Connect the Variable ISI board (including MMPX-MMPX cables) to the CBB Rx Lane.
4. Using Nominal 1.5 dB cables, connect the CBB Tx Lane to the MU196060A Re-Driver data inputs.
5. Connect the MU196060A Re-Driver data outputs to the MU196040B data inputs for loopback error detection.
6. Connect the MU196060A Re-Driver clock output to the MU196040B Ext Clock in.

8.3.2 Equipment Setup for System Board DUT Loopback Test

The following connection diagram shows the physical setup to enable loopback to perform link training for the PCIe Gen 6 system board DUT. This setup is using the MP1900A BERT that includes the MU196040B PAM4 Error Detector module, MU196060A Re-Driver and a compliant CLB test fixture for the DUT.

Note: Before starting the System Board Rx Compliance Test, make sure to perform optimization of the Return Path (DUT Tx to BERT error detector).

Note: A Re-Driver may be required for System DUT testing. The return path of the Re-Driver needs to be optimized. The procedure for optimizing the Re-Driver return path is described in the manual at the link below:

<https://dl.cdn-anritsu.com/en-en/test-measurement/files/Application-Notes/Application-Note/mp1900a-pcie6-ef1500.pdf>

Note: Use logical Lane 0 for the following test setup.

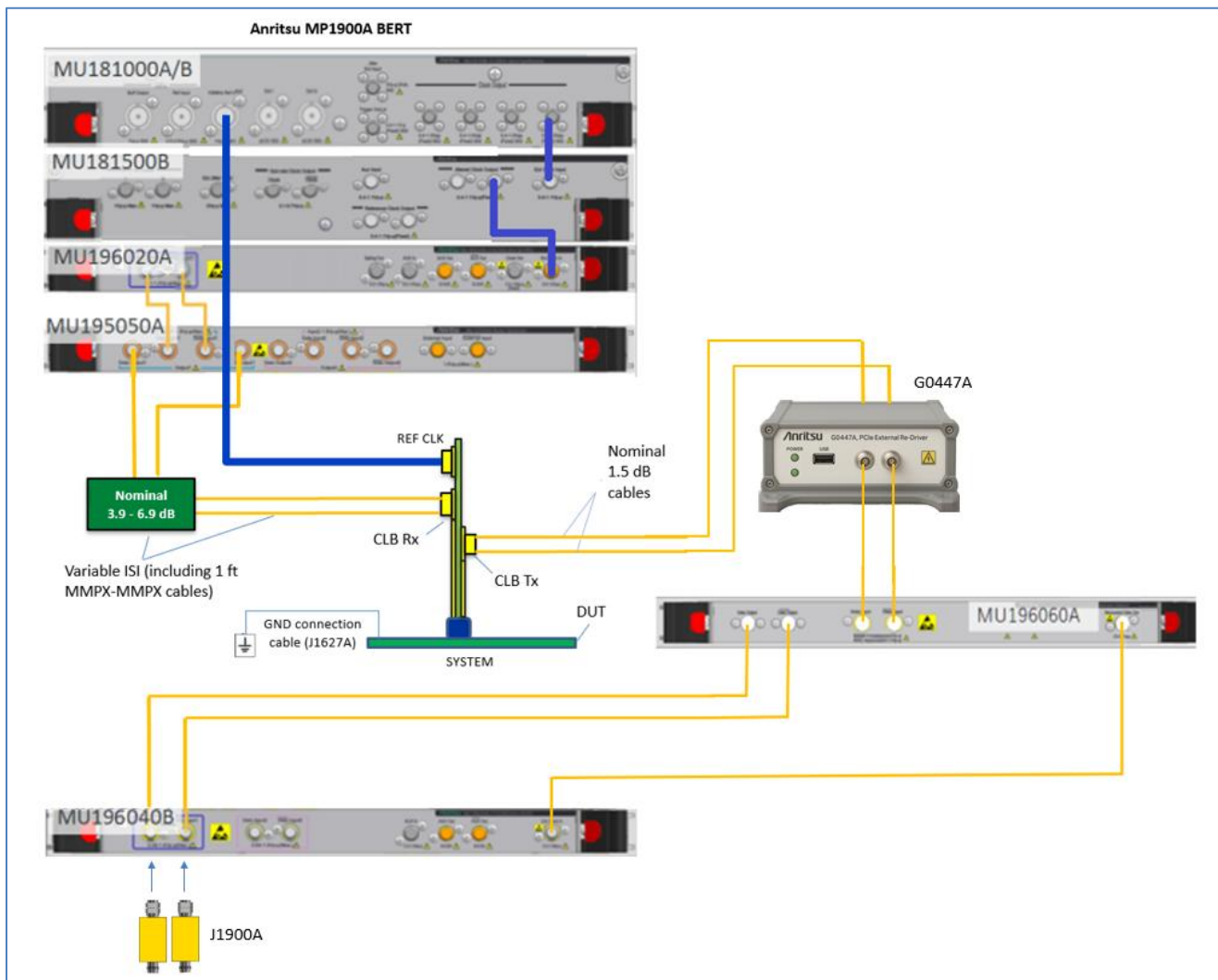


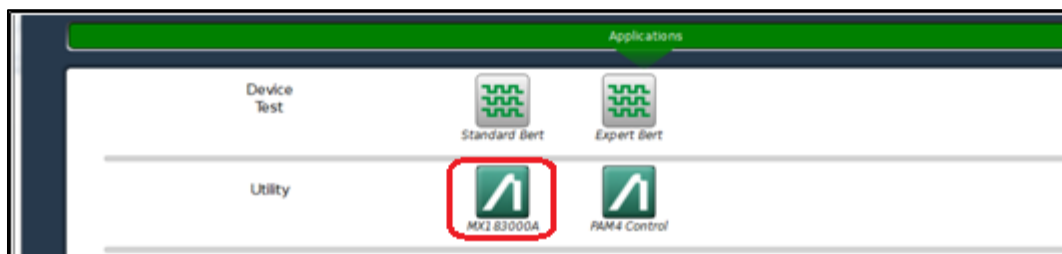
FIGURE 62. CONNECTION DIAGRAM FOR PCIe GEN 6 SYSTEM BOARD DUT LOOPBACK TEST

1. Using the same setup from the system board link EQ test (Figure 60), remove all oscilloscope connections along with the pick-off tees.
2. Connect the MU195050A data outputs to Variable ISI board (Nominal 3.9 – 6.9 dB trace).
3. Connect between both the Variable ISI board (including 1 ft MMPX-MMPX cables) and CLB Rx Lane.
4. Using nominal 1.5 dB cables, connect the CLB Tx Lane to the G0447A external PCIe6 Re-Driver data inputs.
5. Using the J1789A coaxial cables, connect the G0447A data outputs to the MU196060A Re-Driver data inputs.
6. Connect the MU196060A Re-Driver data outputs to the MU196040B data inputs for loopback error detection.
7. Connect the J1900A passive low frequency equalizer to the MU196040B data inputs.
8. Connect the MU196060A Re-Driver clock output to the MU196040B Ext Clock in.

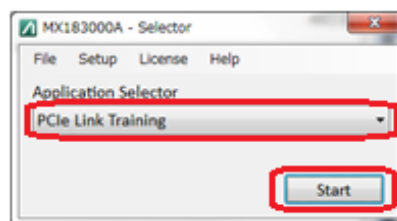
8.3.3 Link Training Initialization and Testing

The Anritsu MX183000A High-Speed Serial Data test software is used with the MX190000A test application on the MP1900A BERT to perform link training.

1. Enable all calibrated stresses on the BERT.
2. On the BERT's Applications screen, select the MX183000A Utility application.



3. In the MX183000A – Selector pop-up, select 'PCIe Link Training' and then 'Start'.



4. In the next window, select the network address of the MX190000A BERT application followed by 'Connect' to link up with the MX190000A.

☒ No.1
TCPIP0::127.0.0.1::5001::SOCKET

☐ No.2
TCPIP0::192.168.2.100::5001::SOCKET

☐ No.3
TCPIP0::192.168.2.100::5001::SOCKET

Search Start
Connect

- In the MX183000A – PCIe Link Training window, select the ‘Link Training’ tab. Select “Recovery Full EQ” under the Loopback Method drop-down field. The Recovery mode is a recommended setting for the DUT loopback state.

MX183000A - PCIe Link Training
×

Operate MP1900A

File Setup Help

Electrical Idle

Equipment Setup
Link Training
Run Test Graph Report

Link Training Setting

Specification
6.0(64.0 GT/s)

DUT
Root Complex (System)

☐ More results

LTSSM State

Linkup Speed

8b10b	Received	Transmitted
SKP Count		
Symbol Err		
Current RD Err		
Symbol Lock		

128b130b	Received	Transmitted
SKP Count		
TS1/TS2 Symbol14-15 DC Balance		
Sync Header Err		
TS1 OS Parity Err		
Block Lock		
EIEOS Counter		

1b1b	Received	Transmitted
Control SKP Count		
TS0/TS1/TS2 Symbol 7,15 DC Balance		
TS0/1/2 OS Parity Err		
Block Lock		
EIEOS Counter		
Idle Flit		
Count		
Err Count		

Received
Use Preset

PPG Final Preset

PPG Final Cursor
2nd Pre-Cursor(C-2)
Pre-Cursor(C-1)
Cursor(C0)
Post-Cursor(C+1)

Full Swing, Low Frequency

Recovery.EQ

	Phase0 (Root)	Phase1	Phase2	Phase3
PCIe 3				
PCIe 4				
PCIe 5				
PCIe 6				

LEQ Test Tx LEQ Response Apply
Rx LEQ Initial TX LEQ Tx LEQ Response
Loopback Through: Recovery
Link EQ: Preset Saved Cursor...
Lane: 0/8
Test Pattern: CP (Compliance Pattern)
PPG Starting Preset: Q1
DUT Initial Preset (Preset Hint Tx): Q1
DUT Target Preset (Change Preset): Q0

Option

Timeout

Return Path Optim.

File Name
AutoSave_202601160903.xml
File Open Clear

Optimization

Test Pattern
Compliance
CP
SRIS OFF

Link Training Loopback Method

Recovery Full EQ

Link Start

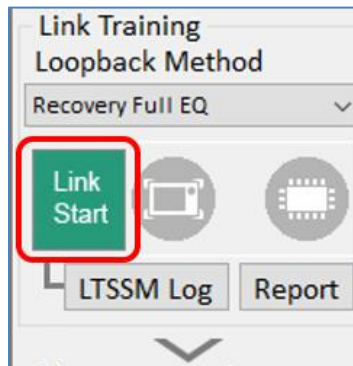
LTSSM Log Report

Measurement Item
☐ Configure
BER Measurement
Matrix Scan

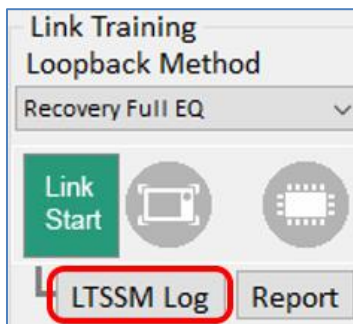
6. Press the Power Reset button on the CBB test fixture to reset the DUT.



7. In the MX183000A – PCIe Link Training window, select “Link Start” under Link Training.



8. If the LTSSM (Link Training and Status State Machine) State shows ‘Loopback.Active.Master’, it means link training is successful.
If ‘Detect.Quiet’ is shown instead, it means link training has failed.
9. Select “LTSSM Log” to generate a log of the link training results.



If the link training is successful, the log will show the DUT enter a Loopback Active state.

If the link training has failed, the log will show the Detect and Polling states.

8.3.4 Link Training Failure Troubleshooting

If the link training has been unsuccessful, perform troubleshooting for any of the following cases that may have been encountered during testing.

- a) The LTSSM state for link training is repeated at 2.5 GT/s:
 - Check that the instruments and fixtures have been properly connected.

- Ensure sufficient power supply to the DUT.
 - Press the Power Reset button on the CBB or reboot the DUT.
 - Connect the MU195050A noise generator data outputs directly to the MU196040B PAM4 Error Detector data inputs, and try to run link training by selecting “Configuration” under the ‘Loopback Through’ field in the Link Training tab.
- b) The DUT enters the 64 GT/s LTSSM state, but the Loopback Active state is not shown.
- Set all Jitter and Noise to OFF on the BERT.
 - Remove the ISI channel and connect data signals to the DUT directly.
 - Press the Power Reset button on the CBB or reboot the DUT.
 - Ensure the PPG Output setting is ON.
 - Change to other Preset values, for example:
 - Q5, Q6, Q8 and Q9 are recommended for PCIe Gen 6.
 - Ensure the correct EIEOS pattern revision of the DUT is being used.

If link training still fails, restart both the MX190000A and MX183000A applications.

8.4 Perform DUT Rx Compliance Testing

This section describes how to test the DUT to meet the PCIe CEM 6.0 Rx electrical compliance specs. The Rx path is tested with the worst case stressed eye to ensure a FBER of less than 1E-6 can be achieved. An optional jitter tolerance test is also described here.

The Rx compliance test can be performed once the DUT has passed the link training loopback tests (as described in the previous section).

1. Enable all calibrated stresses on the BERT.
2. In the same link training window from the previous test, the LTSSM State will show ‘Loopback.Active.Master’ to indicate link training has been successful. From there, select ‘BER Measurement’ to start the error detection process for the DUT.
3. Run the test for 15 seconds for the PCIe Gen 6 DUT.

Note: Any # of bit errors (1 or 2) in the PAM4 symbol is considered a symbol error. Any number of consecutive PAM 4 symbol errors up to length of 8 count as 1 error towards FBER calculation.

8.4.1 Jitter Tolerance Testing (Optional)

The DUT can be additionally tested for jitter tolerance after it has passed Rx compliance testing. The optional jitter tolerance test is basically carried out to search for SJ margins and measure the FBER.

1. Continuing from the same Rx compliance test window, select the Run Test tab. Select ‘Run Test’ to start running measurements for jitter tolerance.
2. When completed, select the Graph tab to view a data plot from the measurement results.

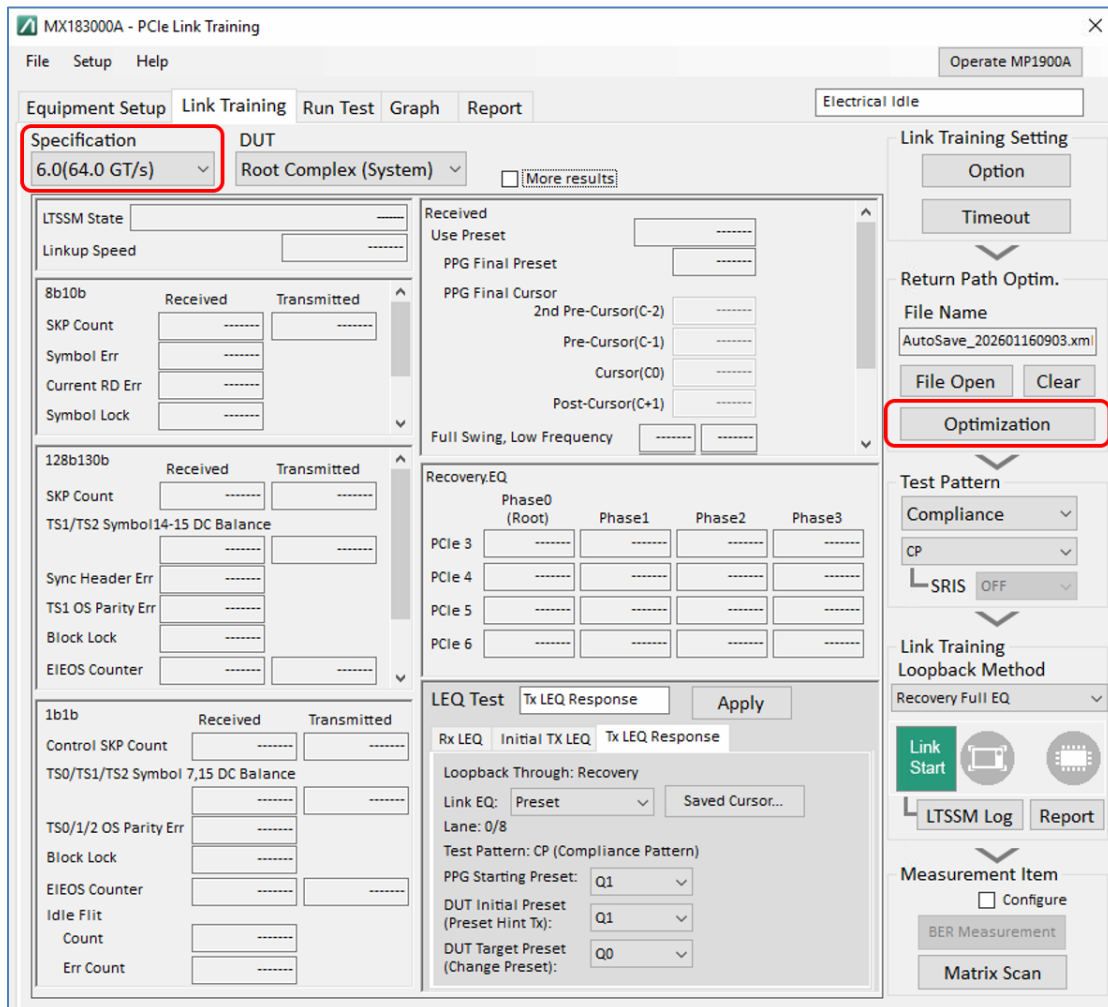
9 Appendix B: Return Path Optimization Using Anritsu MU196060A Re-Driver

It is important to optimize the Return Path (DUT Tx to BERT Error Detector) when testing for Receiver Link Equalization and Rx Compliance with PCIe Gen6 (64 GT/s), as described below.

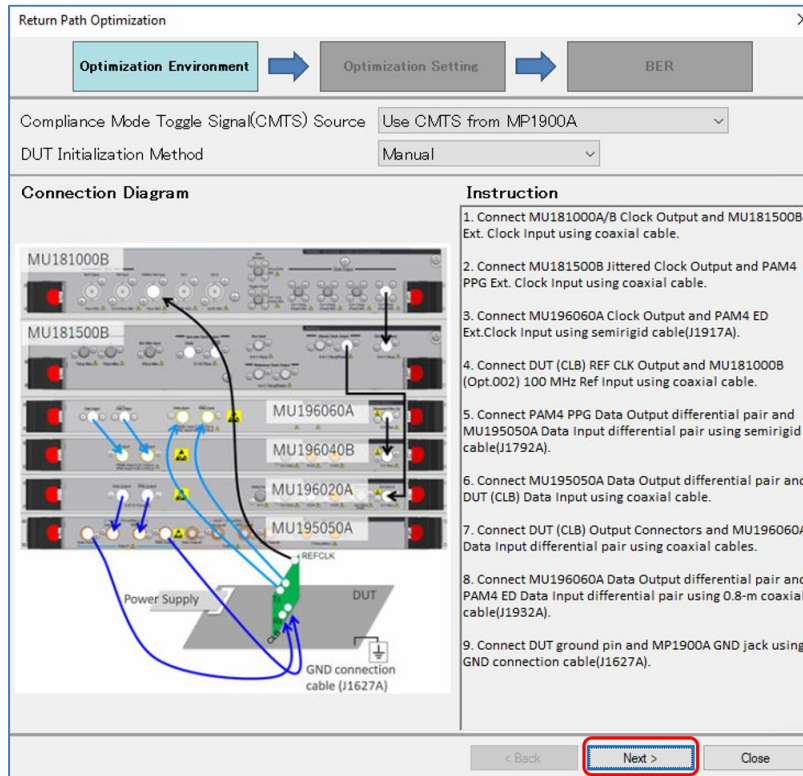
9.1 Return Path Optimization Procedure

Follow the steps below to optimize the Return Path.

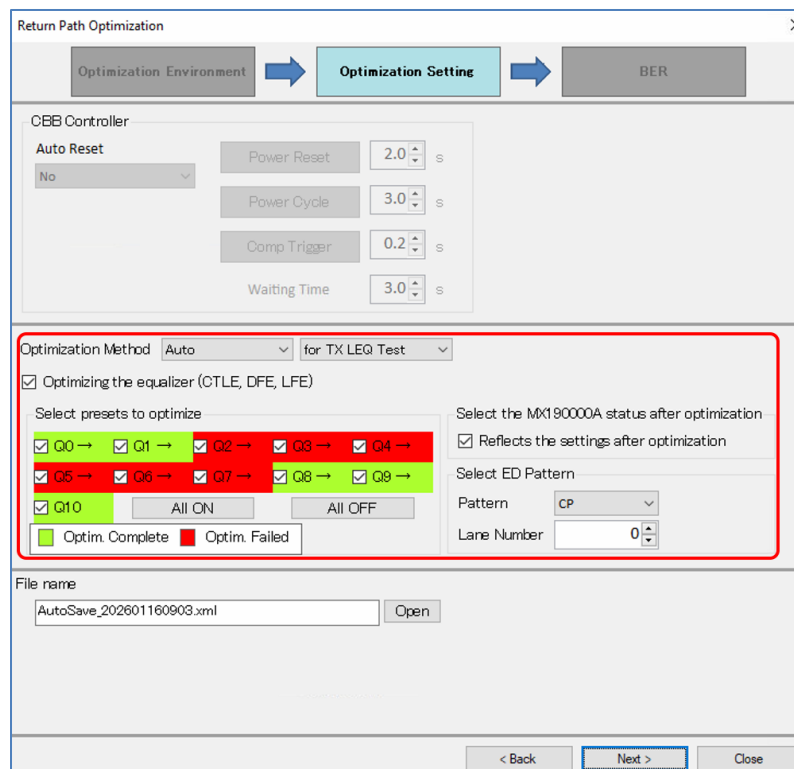
1. Connect the equipment as shown in the DUT TxRx Link EQ Test setups in Section 5.5.1 & 5.5.2 and DUT Rx Compliance Test setups in Section 5.6.1 & 5.6.2 respectively.
2. Start the MX183000A, set the 'Specification' to 'Gen6'. In the 'Return Path Optim.' section, click on the Optimization button as follows:



3. In the following 'Optimization Environment' screen, make sure that all equipment connections are set up correctly and then click 'Next' to proceed.



4. In the following 'Optimization Setting' screen, configure the required parameters (e.g. presets to optimize, error detector pattern, lane number). Then click 'Next' to proceed.



5. In the following 'BER' optimization screen, click on the **Start Optimization** button to measure BER with the preset and other settings specified in step 4. This will find the setting that gives the optimal BER.
 - a) Wait until the optimization process is completed and then check BER.
 - b) Increase the preset file number of the re-driver by 1 or 2 at a time and then check the BER again. If the optimal preset BER numbers are detected in succession, repeat until you find the preset number at which the BER deteriorates. If an error-free condition is achieved with multiple preset file numbers, use the preset file with the middle number of a series of preset file numbers as the optimum setting.
 - c) Click on the **Start Optimization** button and check the BER again.
6. When an error-free condition is achieved with the steps so far, then optimization of Return Path is completed successfully.

10 Appendix C: Connecting Keysight Oscilloscope to PC

If using a Keysight oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Keysight Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Keysight IO Libraries Suite software from the Keysight website and install on the PC.
2. When installed successfully, the IO icon () will appear in the taskbar notification area of the PC.
3. Select the IO icon to launch the **Keysight Connection Expert**.
4. Click Rescan.

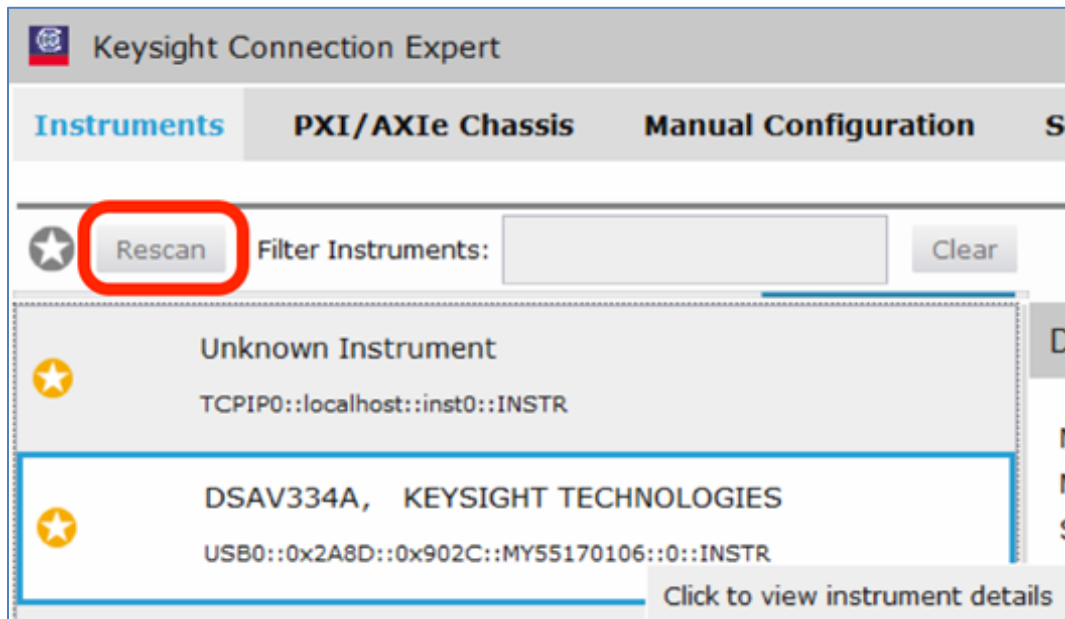


FIGURE 63. KEYSIGHT CONNECTION EXPERT

5. Refresh the system. The Keysight Scope is shown on the left pane and the VISA address is shown on the right pane.

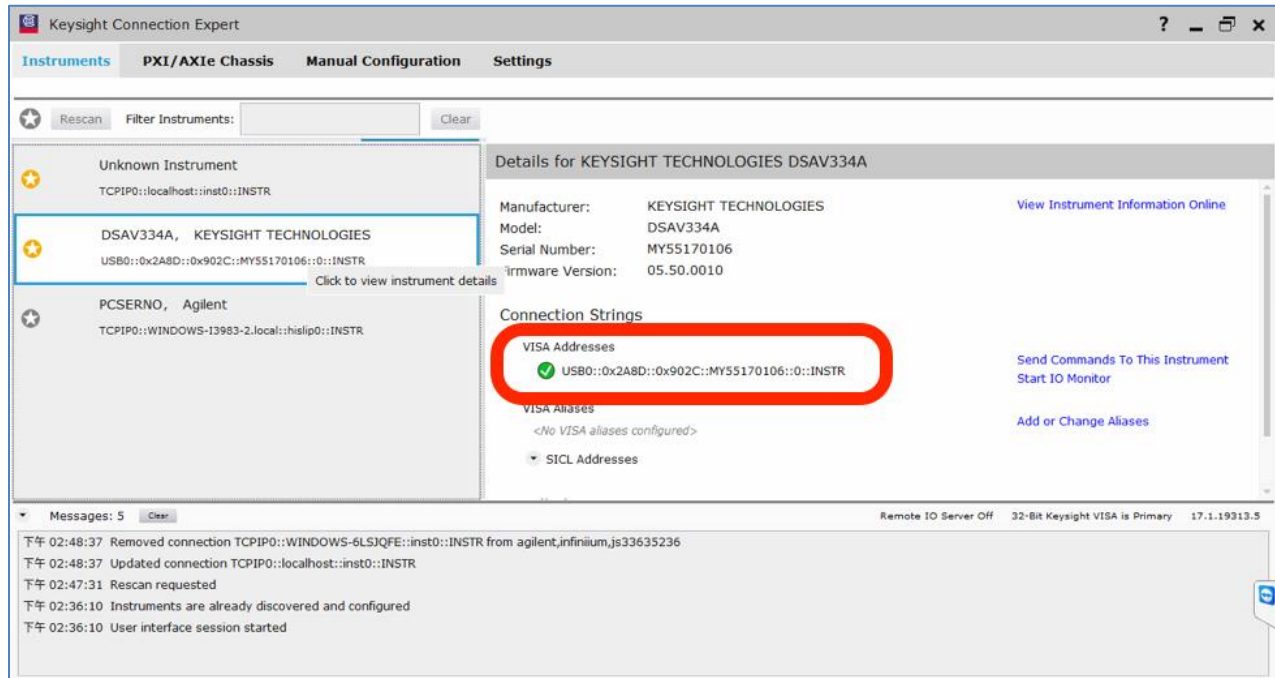


FIGURE 64. OSCILLOSCOPE'S VISA ADDRESS

6. When connecting the Keysight Scope to the PC through GPIB/USB, type in the VISA address into the 'Address' field on the Equipment Setup page of the Anritsu_GRL PCIe CEM 6.0 Rx Test Application. If connected via LAN, type in the Scope IP address, for example "TCPIP0::192.168.0.110::inst0::INSTR". Note to **omit** the Port number from the address.

If there is error in connection, type in the Scope IP address as "TCPIP0::192.168.0.4::5025::SOCKET".

11 Appendix D: Connecting Tektronix Oscilloscope to PC

If using a Tektronix DPOJET Series oscilloscope, refer to the following procedure on how to connect the Scope to be used with a PC. The Tektronix Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Tektronix TekVISA software from the Tektronix website and install it on the PC.
2. When installed successfully, open the OpenChoice Instrument Manager application.

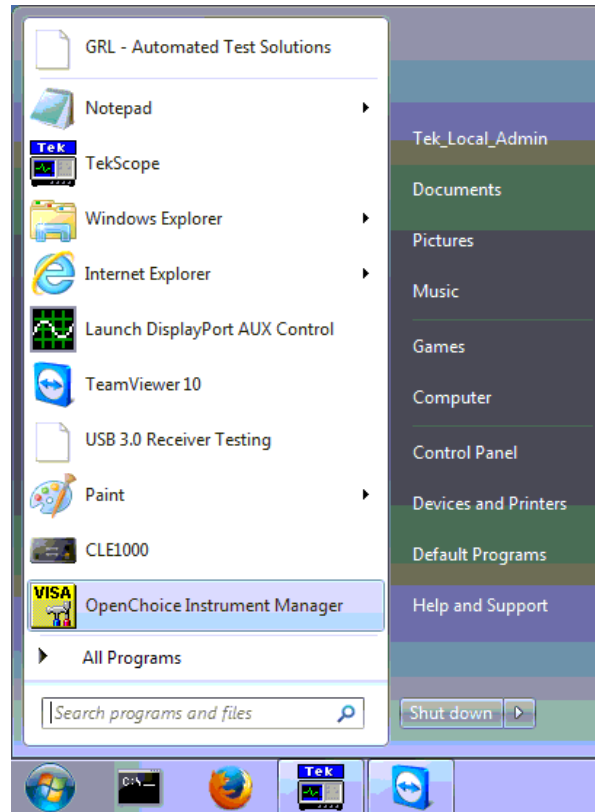


FIGURE 65. OPENCHOICE INSTRUMENT MANAGER IN START MENU

3. The left “Instruments” panel on the OpenChoice Instrument Manager will display all connected instruments. The functional buttons below the “Instruments” panel – “Instrument List Update”, “Search Criteria”, “Instrument Identify” and “Properties” can be used to detect the Scope in case it does not initially appear under “Instruments”.
 - a) “Instrument List Update”: Select to refresh the instrument list and locate new instruments connected to the PC.
 - b) “Search Criteria”: Select to configure the instrument search function.
 - c) “Instrument Identify”: Select to use a supported programming language to send a query to identify the selected instrument.
 - d) “Properties”: Select to display and view the selected instrument properties.

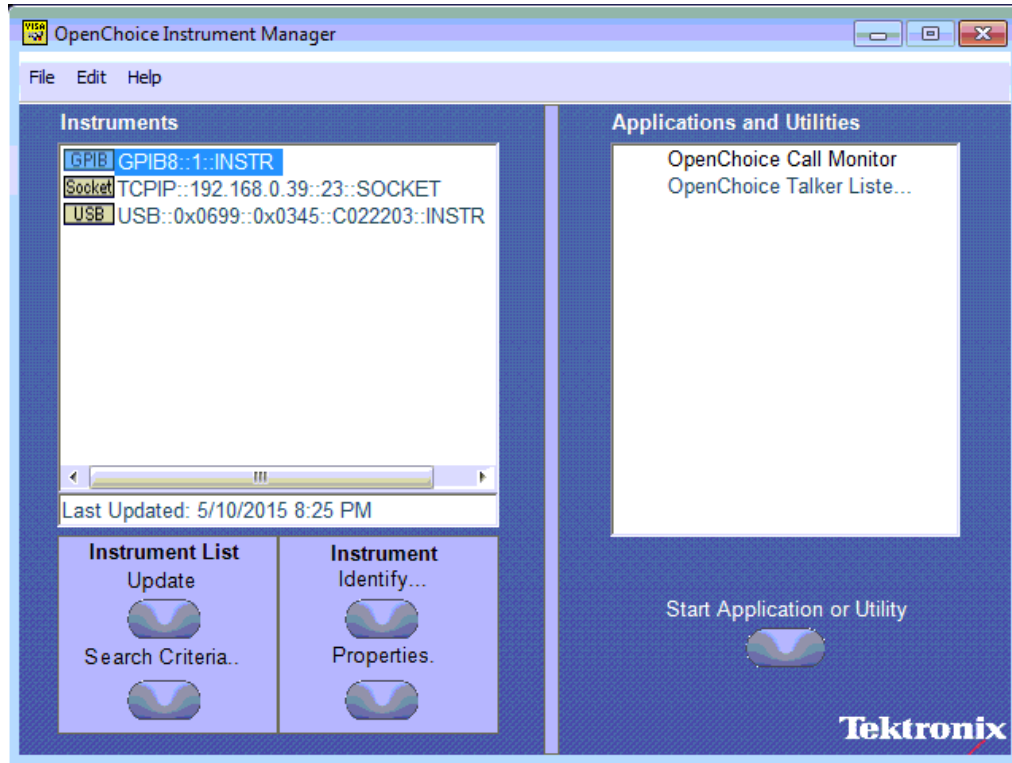


FIGURE 66. OPENCHOICE INSTRUMENT MANAGER MENU

4. If connecting the Tektronix Scope to the PC via USB, select the “Search Criteria” function to ensure that USB connection is enabled, and then select the “Instrument List Update” function. When the Scope appears on the “Instruments” panel, select it and then go to the “Instrument Identify” function. This will display the model and serial number of the Scope once detected. Select the “Properties” function to view the Scope address.
5. If connecting the Tektronix Scope to the PC via LAN, the Scope IP address must be pre-determined beforehand. Then select the “Search Criteria” function to ensure that LAN connection is enabled and type in the Scope IP address. When the Scope shows up in the list, select it followed by “Search”. The Scope should then appear on the “Instruments” panel. Select it and access the “Instrument Identify” function to view the Scope model and serial number as well as the “Properties” function to view the Scope address.
6. On the Equipment Setup page of the Anritsu_GRL PCIe CEM 6.0 Rx Test Application, type in the Scope address into the ‘Address’ field. If the Anritsu_GRL PCIe CEM 6.0 Rx Test Application is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example “GPIB8::1::INSTR”. If the Anritsu_GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example “TCPIP0::192.168.0.110::inst0::INSTR”. Note to **omit** the Port number from the address.

END_OF_DOCUMENT