



GRL Platform Solutions

**USB4® Version 2.0 Receiver Test Method of
Implementation (MOI)
Using Anritsu MP1900A BERT,
High Performance Real-time Oscilloscope,
and GRL-USB4-V2-RXA Calibration and Test Automation
Software**

Published on 31 July 2026

DISCLAIMER

This document is provided “as is” with no warranties whatsoever, including any warranty of merchantability, no infringement, fitness for any particular purpose, or any warranty otherwise arising out of any proposal, specification, or sample. The GRL Platform Solutions disclaims all liability for infringement of proprietary rights, relating to use of information in this specification. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted herein.

All product names are trademarks, registered trademarks, or service marks of their respective owners.



Copyright © 2026 GRL Platform Solutions. All rights reserved.

TABLE OF CONTENTS

1	INTRODUCTION	10
2	RESOURCE REQUIREMENTS	11
2.1	EQUIPMENT REQUIREMENTS	11
2.2	SOFTWARE REQUIREMENTS.....	14
3	INSTALLING AND SETTING UP GRL-USB4-V2-RXA SOFTWARE	15
3.1	DOWNLOAD AND SET UP GRL-USB4-V2-RXA SOFTWARE.....	15
3.1.1	Download and Install USB4 V2 Electrical Test Tools (ETT)	17
3.1.2	Launch and Set Up GRL-USB4-V2-RXA Software.....	18
3.1.3	Set Up Remote File Server	19
4	RECEIVER CALIBRATION SETUPS	21
4.1	CONNECTION SETUP FOR SCOPE INTRINSIC NOISE MEASUREMENT.....	21
4.2	GENERAL CALIBRATION CONNECTION SETUP.....	22
4.3	CONNECTION SETUP FOR CASE 2 LINK OPERATING MARGIN EVALUATION (RX & TX) CALIBRATION	23
5	CALIBRATING USING GRL-USB4-V2-RXA SOFTWARE	27
5.1	ENTER CALIBRATION/TEST SESSION INFORMATION	27
5.2	SET UP CONDITIONS FOR CALIBRATION/TESTING	27
5.3	SELECT CALIBRATION.....	30
5.4	SET UP SIGTEST ENVIRONMENT.....	31
5.5	PERFORM DE-EMBEDDING OF TEST RECEPTACLE FIXTURE	32
5.6	CONFIGURE CALIBRATION PARAMETERS	33
5.7	CONFIGURE CALIBRATION TARGET VALUES	35
5.8	RUN CALIBRATION.....	35
6	COMPLIANCE TESTING USING GRL-USB4-V2-RXA SOFTWARE	37
6.1	CONNECTION SETUPS FOR RECEIVER TER TESTING	37
6.1.1	MP1900A BERT Standard Modes.....	37
6.1.2	TER Test Setup for Case 1.....	42
6.1.3	TER Test Setup for Case 2	45
6.2	RECEIVER LFPS TEST SETUPS.....	48
6.2.1	Standard BERT for PAM4 with MU195050A Mode	48
6.2.2	Standard BERT for PAM4 with MU196050A Mode	49
6.2.3	Standard BERT for SI Mode.....	50
6.3	SELECT DUT RX COMPLIANCE, AGGRESSOR SIGNAL MONITORING, FREQUENCY VARIATION, MARGIN SEARCH, LFPS AND LRD TESTS	51
6.4	SELECT TEST MODE.....	52

6.5	SET UP USB4 ETT ENVIRONMENT.....	52
6.6	SET UP LRD TEST ENVIRONMENT.....	53
6.7	CONFIGURE MARGIN SEARCH TEST VALUES.....	54
6.8	CONFIGURE TEST PARAMETERS.....	54
6.9	RUN DUT RX TESTS.....	57
7	TEST RESULTS AND REPORTS USING GRL-USB4-V2-RXA SOFTWARE	58
7.1.1	DUT Information.....	58
7.1.2	Results Summary Table.....	59
7.1.3	Calibration & Test Result Details.....	60
7.2	DELETE TEST RESULTS.....	61
8	SAVING AND LOADING GRL-USB4-V2-RXA TEST SESSIONS	62
9	APPENDIX A: MANUAL CALIBRATION & TEST METHODOLOGIES	63
9.1	INITIALIZE SETTING OF BERT AND SCOPE FOR RECEIVER STRESSED EYE CALIBRATION FOR CASE 1.....	63
9.1.1	Set up the MP1900A BERT as follows:.....	63
9.1.2	Set Up Oscilloscope.....	73
9.2	VOLTAGE SWING CALIBRATION FOR CASE 1.....	75
9.3	LEVEL MISMATCH CALIBRATION FOR CASE 1.....	77
9.4	RJ CALIBRATION FOR CASE 1.....	80
9.5	SNDR CALIBRATION FOR CASE 1.....	83
9.6	ACCM CALIBRATION FOR CASE 1.....	86
9.7	PJ CALIBRATION FOR CASE 1.....	89
9.8	INITIALIZE SETTING OF BERT AND SCOPE FOR CALIBRATE RECEIVER STRESSED EYE FOR CASE 2.....	93
9.8.1	Set up the MP1900A BERT as follows:.....	93
9.8.2	Set Up Oscilloscope.....	103
9.9	VOLTAGE SWING CALIBRATION FOR CASE 2.....	105
9.10	LEVEL MISMATCH CALIBRATION FOR CASE 2.....	107
9.11	RJ CALIBRATION FOR CASE 2.....	110
9.12	SNDR CALIBRATION FOR CASE 2.....	113
9.13	ACCM CALIBRATION FOR CASE 2.....	116
9.14	PJ CALIBRATION FOR CASE 2.....	119
9.15	BERT MODEL EXTRACTION FOR CASE 2.....	122
9.15.1	Differential Return Loss Measurement at BERT Assembly Output.....	122
9.15.2	BERT Assembly Step Response Extraction.....	124
9.15.3	Differential Insertion Loss of the BERT Assembly Extraction.....	125
9.15.4	Test Channel Measurement.....	125

9.15.5	Link operating margin evaluation.....	126
9.16	USB4 GEN 4 TER TEST CASE 1	127
9.17	USB4 GEN 4 TER TEST CASE 2.....	129
9.18	RECEIVER FREQUENCY VARIATION CALIBRATION FOR CASE 1.....	131
9.19	RECEIVER FREQUENCY VARIATION CALIBRATION FOR CASE 2	134
9.20	RECEIVER FREQUENCY VARIATION TEST CASE 1	137
9.21	RECEIVER FREQUENCY VARIATION TEST CASE 2.....	138
10	APPENDIX B: RECEIVER STRESSED EYE CALIBRATION USING SIGTEST	139
10.1	INSTALL AND RUN SigTest.....	139
10.2	SET UP SCOPE FOR SAVING WAVEFORMS	139
11	APPENDIX C: CONNECTING KEYSIGHT OSCILLOSCOPE TO PC	140
12	APPENDIX D: CONNECTING TEKTRONIX OSCILLOSCOPE TO PC	142

List of Figures

Figure 1. Launching GRL Platform Solutions Software Framework.....	15
Figure 2. Launching Anritsu USB4 V2 Rx Test Application.....	16
Figure 3. License Details.....	16
Figure 4. Check License for Installed Application	16
Figure 5. GRL Platform Solutions Software Instrument Connection Setup	19
Figure 6. Installed GRLRemoteProxyServer.exe File Directory	19
Figure 7. Verify Proxy Server Connection for Controller PC and Scope	20
Figure 8. Configure Remote Proxy Server Network Settings on GRL Platform Solutions Software.....	20
Figure 9. Setup for Scope Intrinsic Noise Measurement.....	22
Figure 10. General Setup for USB4 Gen 4 Calibration.....	22
Figure 11. Setup for Link Operating Margin Evaluation for RX0	24
Figure 12. Setup for Link Operating Margin Evaluation for RX1 (Optional)	24
Figure 13. Setup for Link Operating Margin Evaluation for TX0.....	25
Figure 14. Setup for Link Operating Margin Evaluation for TX1 (Optional)	25
Figure 15. Enter Calibration/Test Session Information	27
Figure 16. Select Test Points for Calibration and Testing	28
Figure 17. Select USB4 Symmetric Link or Asymmetric Link.....	28
Figure 18. Select High Speed Test Lanes for Symmetric or Asymmetric Link	28
Figure 19. Select PJ Frequency	29
Figure 20. Select LFPS Test Lanes for Symmetric or Asymmetric Link.....	29
Figure 21. Select LRD Test Lanes for Symmetric or Asymmetric Link	29
Figure 22. Select Calibration.....	30
Figure 23. Configure SigTest	31
Figure 24. Set Up De-embedding of Test Receptacle Fixture.....	32
Figure 25. Configure Calibration Parameters	33
Figure 26. Calibration Target Overwrite Page	35
Figure 27. Run Calibration	35
Figure 28. Connection Setup Diagram Dialog Example.....	36
Figure 29. Standard BERT for PAM4 with MU196050A Setup	38
Figure 30. Standard BERT for PAM4 with MU195050A Setup	39
Figure 31. Standard BERT for SI	41
Figure 32. Rx TER Test Setup for Case 1 Using PAM4 Standard BERT Mode With MU195050A	42
Figure 33. Rx TER Test Setup for Case 1 Using PAM4 Standard BERT Mode With MU196050A	43
Figure 34. Rx TER Test Setup for Case 1 Using SI Standard BERT Mode	44
Figure 35. Rx TER Test Setup for Case 2 Using PAM4 Standard BERT Mode With MU195050A	45

Figure 36. Rx TER Test Setup for Case 2 Using PAM4 Standard BERT Mode With MU196050A	46
Figure 37. Rx TER Test Setup for Case 2 Using SI Standard BERT Mode.....	47
Figure 38. Rx LFPS Test Setup Using PAM4 Standard BERT Mode With MU195050A	48
Figure 39. Rx LFPS Test Setup Using PAM4 Standard BERT Mode With MU196050A	49
Figure 40. Rx LFPS Test Setup Using SI Standard BERT Mode	50
Figure 41. Select DUT Rx Compliance, Aggressor Signal Check, Frequency Variation and Margin Search Tests to be Run	51
Figure 42. Select Test Mode	52
Figure 43. Setup for ETT Environment.....	52
Figure 44. Setup for LRD Test Environment.....	53
Figure 45. Configure PJ Margin Search Test Values	54
Figure 46. Configure Test Parameters	54
Figure 47. Run Tests.....	57
Figure 48. Report Results Page	58
Figure 49. DUT Information.....	58
Figure 50. Results Summary Table Example	59
Figure 51. Calibration/Test Result Details Example.....	60
Figure 52. Delete All Results.....	61
Figure 53. Save/Load/Create Test Sessions	62
Figure 54. Modulation Type “PAM3” Setting	64
Figure 55. Jitter Clock Source Setting.....	65
Figure 56. PPG Misc2 Settings	66
Figure 57. Pattern Setting.....	67
Figure 58. PPG Emphasis Setting.....	68
Figure 59. SSC Setup for Test Case 1.....	69
Figure 60. CM and DM Setting.....	70
Figure 61. SJ1 Setting.....	71
Figure 62. RJ Setting.....	72
Figure 63. Turn on Glitch-free.....	73
Figure 64. Oscilloscope Vertical and Horizontal Setup	74
Figure 65. Modulation Type “PAM3” Setting	94
Figure 66. Jitter Clock Source Setting.....	95
Figure 67. PPG Misc2 Settings	96
Figure 68. Pattern Setting	97
Figure 69. PPG Emphasis Setting.....	98
Figure 70. SSC Setting for Test Case 2.....	99
Figure 71. CM and DM Setting.....	100
Figure 72. SJ1 Setting.....	101
Figure 73. RJ Setting	102
Figure 74. Turn on Glitch-free.....	103

Figure 75. Oscilloscope Vertical and Horizontal Setup.....	104
Figure 76. Test Setup for BERT Assembly Return Loss Extraction	123
Figure 77. Test Setup for BERT Assembly Step Response Extraction	124
Figure 78. Frequency Variation Dynamics for Case 1	132
Figure 79. Frequency Variation Dynamics for Case 2	135
Figure 80. Keysight Connection Expert.....	140
Figure 81. Oscilloscope's VISA Address	141
Figure 82. OpenChoice Instrument Manager In Start Menu.....	142
Figure 83. OpenChoice Instrument Manager Menu	143

List of Tables

Table 1. Equipment Requirements – Systems.....	11
Table 2. Equipment Requirements –Accessories	12
Table 3. Equipment Requirements – Connection Cables.....	13
Table 4. All Tests Parameters Description.....	33
Table 5. Calibration Parameters Description	34
Table 6. Rx Test Parameters Description	56
Table 7. Oscilloscope Vertical and Horizontal Setup	73
Table 8. Oscilloscope ACCM Setup.....	74
Table 9. Oscilloscope Vertical and Horizontal Setup.....	103
Table 10. Oscilloscope ACCM Setup	104
Table 11. Network Analyzer Setup.....	122
Table 12. Oscilloscope Setup for BERT Assembly Step Response Extraction.....	124
Table 13. Network Analyzer Setup for Test Channel Measurement.....	125
Table 14. Oscilloscope Setup for Receiver Frequency Variation Calibration for Case 1	131
Table 15. Oscilloscope Setup for Receiver Frequency Variation Calibration for Case 2.....	134

1 Introduction

This MOI & User Guide contains the procedure for testing an electrical receiver for USB4® Version 2.0 (or USB4 Gen 4) certification at 80 Gbps (40 Gbps x2) using the Anritsu MP1900A BERT, High Performance Real-Time Oscilloscope, and GRL-USB4-V2-RXA Test Automation Software as per USB-IF standards.

The main body of this MOI & User Guide describes how to perform automated Calibration and Testing of USB4 Gen 4 Rx Hosts and Devices using the GRL-USB4-V2-RXA software, with an appendix describing the manual calibration process as a technical reference.

The tests in this MOI are the tests carried out by USB Independent Test Labs (ITL's). If performing the tests yourself, it is important for you to follow the MOI's as described in this document before submitting your Device Under Test (DUT) for Certification in order for you to be confident that your device will pass. ITL's also provide pre-compliance test services if your company does not have the equipment or resources to carry out the tests. Contact GRL Platform Solutions @ support@grlps.com for USB pre-compliance and compliance test services.

For Devices and Hosts with a USB Type-C® Connector, the USB-IF, VESA (DisplayPort over USB Type-C), and Thunderbolt™ Compliance programs all require USB4 Gen 4 receiver compliance testing.

In summary, this User Guide & MOI basically describes using the GRL-USB4-V2-RXA software to:

1. Calibrate and Test a USB4 Gen 4 Receiver.
2. Generate Test Report for Compliance Reporting.

2 Resource Requirements

2.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS – SYSTEMS

System	Qty.	Description	Key Specification Requirement
Oscilloscope	1	High Performance Real-time Oscilloscope	• ≥ 25 GHz bandwidth^[a] • DC to 25 GHz at -3 db bandwidth or higher • Sampling rate ≥ 80 Gs/s • Sample clock jitter/intrinsic jitter < 100 fs rms within the acquired time range of 10 to 50 μsec/div • Intrinsic vertical noise < 3 mV rms within the acquired voltage range of 10 to 100 mV/div • SNDR ≥ 38.5 dB measured using common test methodology for ADC, by applying high quality/low noise sine wave (3 sine-wave test frequencies: 6,10,12.8 GHz, magnitude 800 mV p-p differential) at scope input and measuring the output signal-to-noise-and-distortion ratio while compensating scope intrinsic noise as defined by USB4 V2 standard • Scope measurement software, e.g. Keysight InfiniiSim for Keysight scope or Tektronix DPOJET for Tektronix scope
BERT	1	Anritsu MP1900A Signal Quality Analyzer (SQA) MP1900A Signal Quality Analyzer, with following modules: • MU181000A/B 12.5 GHz Synthesizer • MU181500B Jitter Modulation Source • MU195020A 32G bit/s SI Pulse Pattern Generator • MU196020A 64.2G bit/s or 64.2G baud PAM4 Pulse Pattern Generator (2 units required) • MU195050A Noise Generator	SQA Software Version 10.03.04 or above

System	Qty.	Description	Key Specification Requirement
Vector Network Analyzer (VNA)	1	Anritsu MS46524B ShockLine™ 4-Port Performance Vector Network Analyzer	- MS46524B-020 – Frequency Domain option (50 kHz to 20 GHz) - Firmware Version: V2018.2.1 or above > 20 GHz, 140 dB max
Or ENA Vector Network Analyzer (ENA)	1	Or Keysight E5080B / E5071C 4-Port ENA Vector Network Analyzer - For Channel calibration to worst case condition - The Keysight N4433A calibration kit is required for both Keysight E5080B and E5071C ENA calibration	- Firmware Version: B.14.14 or above 20 GHz
Control PC	1	High-performance computer with SigTest application installed - For automation control (running GRL-USB4-V2-RXA software)	- Windows 11 OS and above - High-performance CPU with Multicore - Minimum system requirements: 32GB RAM memory - Recommended system requirements: 48GB RAM memory

^[a] Oscilloscope with scope bandwidth as specified in vendor specific MOI's.

TABLE 2. EQUIPMENT REQUIREMENTS –ACCESSORIES

Accessory	Qty.	Description	Key Specification Requirement
Plug Test Fixture	1	USB4 Gen 4 (Case 1) Plug Test Fixture	
Receptacle Test Fixture	2	USB4 Gen 4 (Case 2) Receptacle Test Fixture	
TP3 Test Cables	1	0.8m USB Type-C Passive Cable	
Microcontroller	1	USB4 Gen 4 Microcontroller	
Differential Linear Amplifier	1	Anritsu AH54192A	

Accessory	Qty.	Description	Key Specification Requirement
Power Supply	1	Anritsu AH54192A-01	Power supply for Anritsu AH54192A
Cable Deskew Fixture	4	Anritsu V241C	V-connector power splitter
RF Coaxial Adapter	2	Anritsu 34VKF50A	DC to 40 GHz, V(m) to K(f), 50 ohm
Power Splitter	4	Mini-Circuits ZX10-2-183-S+	2 Ways DC Pass Power Splitter, 1500 to 18000 MHz, 50 Ω , SMA connectors
DC Block	2		Bandwidth of at least 33GHz
Attenuator	2		3 dB
	2		6 dB

Note: Cable connector type and length requirements may vary according to the lab setup and the dimensions of the DUT board. Table below is a recommended list. Please also refer to the respective manufacturer for detailed cabling recommendations related to USB4 Version 2.0.

TABLE 3. EQUIPMENT REQUIREMENTS – CONNECTION CABLES

Connection Cable	Qty.	Key Specification Requirement
MU181000A/B to MU181500B	1	Anritsu J1624A SMA-SMA cable (0.3 m)
MU181500A/B to MU196020A	1	Anritsu J1624A SMA-SMA cable (0.3 m)
MU181000A/B to MU195020A	1	Anritsu J1624A SMA-SMA cable (0.3 m)
MU181500A/B to MU196020A	1	SMA-SMA cable (0.5 m)
Coaxial Cable	1 pair	V-connector coaxial cable (40 cm, 1.85 mm)
SMA Cable	5	1 m
	1	0.5 m
JTAG Ribbon Cable	1	For connecting Anritsu AH54192A-01 power supply and Anritsu AH54192A differential linear amplifier
USB Type-C Passive Cables	1	For connecting Gen 4 controller and TP2 Plug Fixture

2.2 Software Requirements

Software	Source
GRL-USB4-V2-RXA	GRL Platform Solutions USB4 Version 2.0 (80 Gbps) Automated Receiver Calibration and Compliance Test Solution – www.grlps.com Includes test setup and pattern files for USB4 Gen 4 Rx testing Included with Node Locked License to single oscilloscope or PC OS
VISA (Virtual Instrument Software Architecture) API Software	VISA Software is required to be installed on the controller PC running GRL-USB4-V2-RXA software. GRL Platform Solutions' software framework has been tested to work with all three versions of VISA available on the Market: 1. NI-VISA: http://www.ni.com/download/ni-visa-17.0/6646/en/ 2. Keysight IO Libraries: www.keysight.com (Search on IO Libraries) 3. Tektronix TekVISA: www.tek.com (Downloads > Software > TekVisa)
MX190000A	Anritsu High-Speed Serial Data Test Software – Mainframe MX190000A SQA Control Software (Version 10.03.04 or above). This software is located on the MP1900A BERT.
SigTest Application	Downloadable from USB-IF's website. (Note: Approval and NDA as a USB-IF Adopter is required to gain access to USB-IF products.)
USB4 Electrical Test Tool (ETT)	Downloadable from USB-IF's website. See Section 3.1.1 for more details.
MATLAB MCR R2024a (24.1)	Downloadable from MATLAB's website. (Note: This is required to run the USB4 Gen 4 SigTest.)

3 Installing and Setting Up GRL-USB4-V2-RXA Software

This section provides the procedure for installing, configuring and verifying the operation of the GRL-USB4-V2-RXA software. It also helps you familiarize yourself with the basic operation of the software.

The software installer automatically creates shortcuts in the Desktop and Start Menu. To open the software application, follow the procedure in the following section.

3.1 Download and Set Up GRL-USB4-V2-RXA Software

Install, launch and set up the GRL-USB4-V2-RXA software on a PC or an oscilloscope (where GRL-USB4-V2-RXA is referred to as ‘Controller PC’ or ‘Scope’ respectively in this MOI & User Guide):

1. Install VISA (Virtual Instrument Software Architecture) on to the PC/Scope where GRL-USB4-V2-RXA is to be used (see Section 2.2).
2. Download the GRL-USB4-V2-RXA ZIP file package from the GRL Platform Solutions support site.
3. The ZIP file contains:
 - **USB4V2RxANPatternFilesInstallationxxxxxxxxxxSetup.exe** – Run this on the Anritsu Signal Quality Analyzer to install the test pattern setup files.
 - **USB4V2RxANTestApplicationxxxxxxxxxxSetup.exe** – Run this on the controller PC or scope to install the GRL-USB4-V2-RXA application.
 - **USB4V2RxANTestScopeSetupFilesInstallationxxxxxxxxxxSetup.exe** – Run this on the scope to install the scope setup files.
4. Launch and set up the software as follows:
 - Open the **GRL** folder from the Windows Start Menu. Click on **GRL – Automated Test Solutions** within the GRL folder to launch the GRL Platform Solutions software framework.

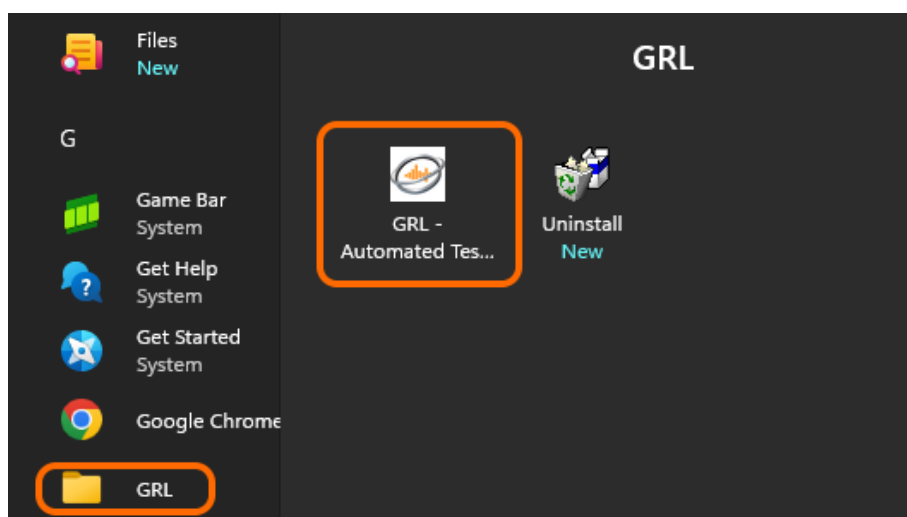


FIGURE 1. LAUNCHING GRL PLATFORM SOLUTIONS SOFTWARE FRAMEWORK

- From the **Application** → **Rx Test Solution** drop-down menu, select **Anritsu USB4 V2 Rx Test**. If the selection is grayed out, it means that your license has expired.

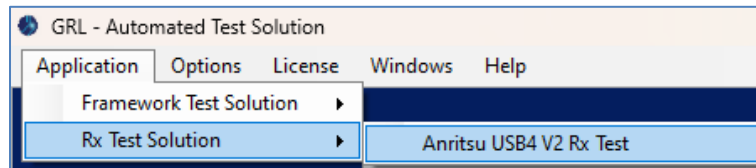


FIGURE 2. LAUNCHING ANRITSU USB4 V2 RX TEST APPLICATION

- To enable license, go to **License** → **License Info**.

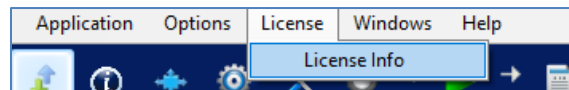


FIGURE 3. LICENSE DETAILS

- Check the license status for the installed application.

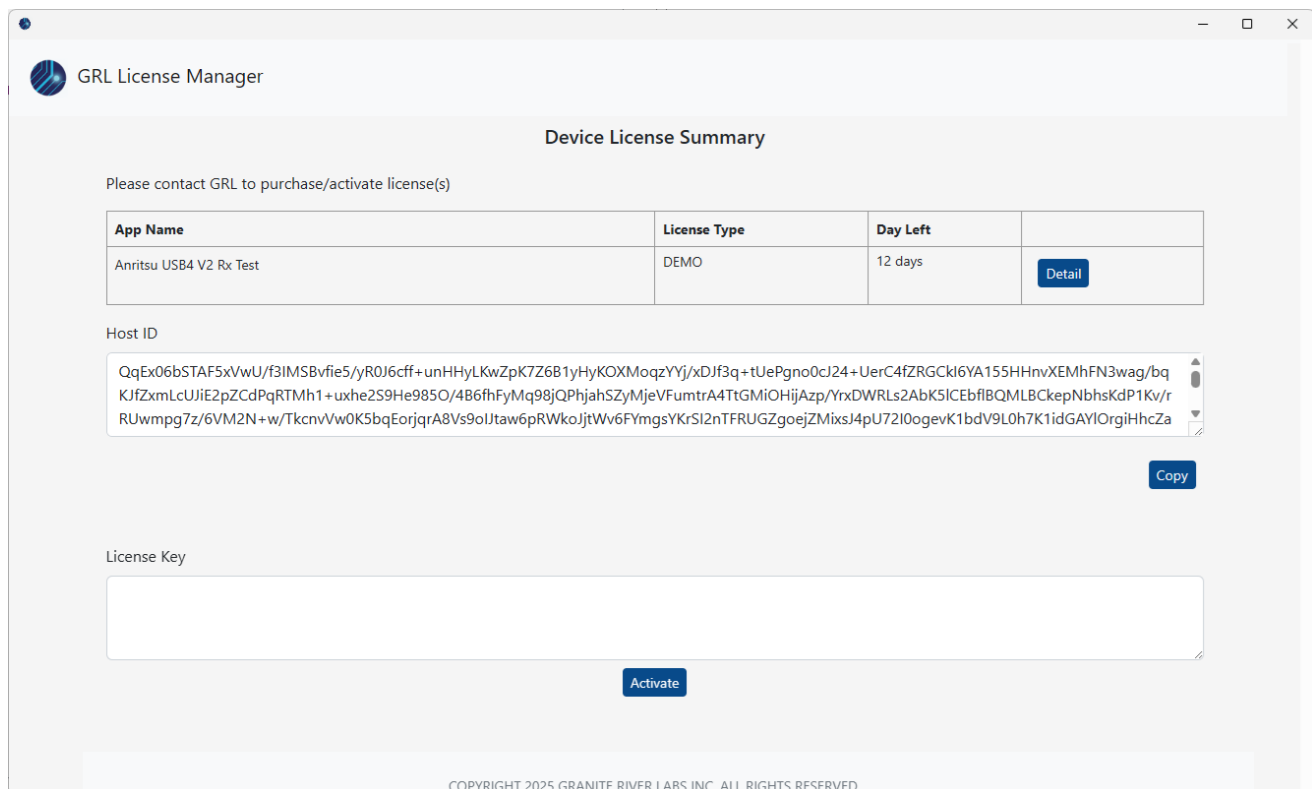


FIGURE 4. CHECK LICENSE FOR INSTALLED APPLICATION

- Activate License:
 - If you have an Activation Key, enter it in the **License Key** field provided and select **Activate**. The installed application is ready for use upon successful activation.
 - If you do not have an Activation Key, close the above window to use a demo version of the application over a free 12-day trial period.

Note: Once the 12-day trial period ends, you will need to request an Activation Key to continue using the application on the same computer by contacting support@grlps.com.

3.1.1 Download and Install USB4 V2 Electrical Test Tools (ETT)

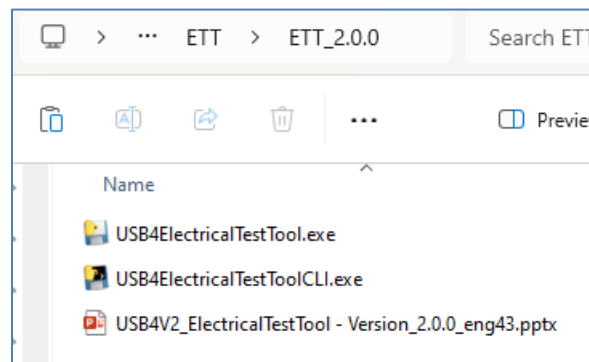
For USB4 V2 Rx measurements, the Host/Device's CIO PHY must be in an active state during testing. Its transmitters shall be transmitting PRBS31 into the analyzer measurement channel during testing and its receivers shall have their terminations enabled during testing. Thus, a PHY microcontroller must be used to put the DUT into the right state for USB4 V2 Rx testing.

Download ETT:

Visit the USB-IF official website and download "USB4 Electrical Test Tool" (ETT) at <https://www.usb.org/usb4tools>.

Install ETT:

Before running ETT, configure the Control PC's environment using the instructions in **USB4V2_ElectricalTestTool – Version_2.0.0_eng43.pptx** from the ETT package downloaded from USB-IF.



For USB4 V2 Host Testing:

- The ETT can be loaded on the Control PC with the GRL-USB4-V2-RXA software. In this case, the USB4 Gen 4 microcontroller is required. The DUT is controlled using a 0.8m USB Type-C passive cable from the USB4 Gen 4 microcontroller to the USB4 V2 Test Fixture.

For USB4 Device Testing:

- Upstream Facing Port (UFP):** The ETT can be loaded on the Control PC with the GRL-USB4-V2-RXA software. In this case, the USB4 Gen 4 microcontroller is required. The DUT is controlled using a 0.8m USB Type-C passive cable from the USB4 Gen 4 microcontroller to the USB4 V2 Test Fixture.
- Downstream Facing Port (DFP):** Connect the DUT's UFP to any USB4 V2 Host via the USB4 Type-C cable. The ETT tools can be loaded on the Control PC with the GRL-USB4-V2-RXA software. In this case, the USB4 Gen 4 microcontroller is required. The DUT is controlled using a 0.8m USB Type-C passive cable from the microcontroller to the USB4 V2 Test Fixture. *Take note for the device DUT, if the port under test is a Downstream Facing Port (DFP), a USB4 V2 Host will be required to connect to the DUT's Upwards Facing Port (UFP).*

3.1.2 Launch and Set Up GRL-USB4-V2-RXA Software

3.1.2.1 On the Scope or Controller PC

1. Launch GRL Platform Solutions Host Application from **Start Menu** → **GRL** → **GRL – Automated Test Solutions**.
2. Select **Application** → **Rx Test Solution** → **Anritsu USB4 V2 Rx Test**.
3. Select the Equipment Setup icon  on the Anritsu USB4 V2 Rx Test Application menu.
4. Connect the Anritsu MP1900A BERT via LAN to the GRL Platform Solutions automation control enabled Scope or PC. The BERT can be connected using a connection string format similar to the following example:

- BERT: “TCPIP0::192.168.0.14::5001::SOCKET” or “192.168.0.14:5001”

Note the addresses listed above are only examples and should be changed according to the actual network connection being used.

5. On the Scope or controller PC, obtain the network addresses for all the connected instruments from the device settings. Note these addresses as they will be used to connect the instruments to the GRL Platform Solutions automation software.
6. On the Equipment Setup page of the Anritsu USB4 V2 Rx Test Application, type in the address of each connected instrument into the ‘Address’ field.

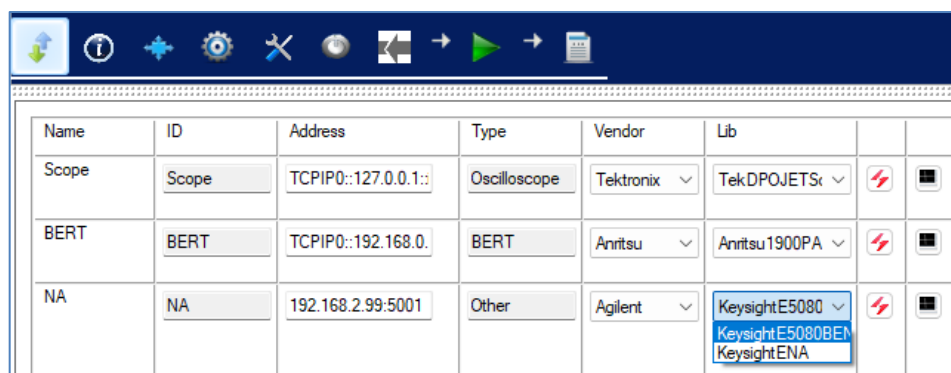
(Note: If the GRL Platform Solutions software is installed on the **Keysight Scope**, type in the Scope IP address, for example “TCPIP0::127.0.0.1::inst0::INSTR”.)

(Note: If the GRL Platform Solutions software is installed on the **Keysight Scope**, and if there is error in connection, type in the Scope IP address as “TCPIP0::192.168.0.35::5025::SOCKET”.)

(Note: If the GRL Platform Solutions software is installed on the **Tektronix Scope**, ensure the Scope is connected via GPIB and type in the GPIB network address, for example “GPIB8::1::INSTR”.)

If the GRL Platform Solutions software is installed on the PC to control the Scope, type in the Scope IP address, for example “TCPIP0::192.168.0.35::inst0::INSTR”. Note to **omit** the Port number from the address.

(Note: The Keysight E5080B / E5071C 4-Port ENA Vector Network Analyzer can be selected as shown below.)



7. If the GRL Platform Solutions software is installed on the PC to control the Scope, set up the Remote File Server as described in Section 3.1.3.
8. Then select the “lightning” button () for each connected instrument.

The “lightning” button should turn green () once the software has successfully established connection with each instrument.

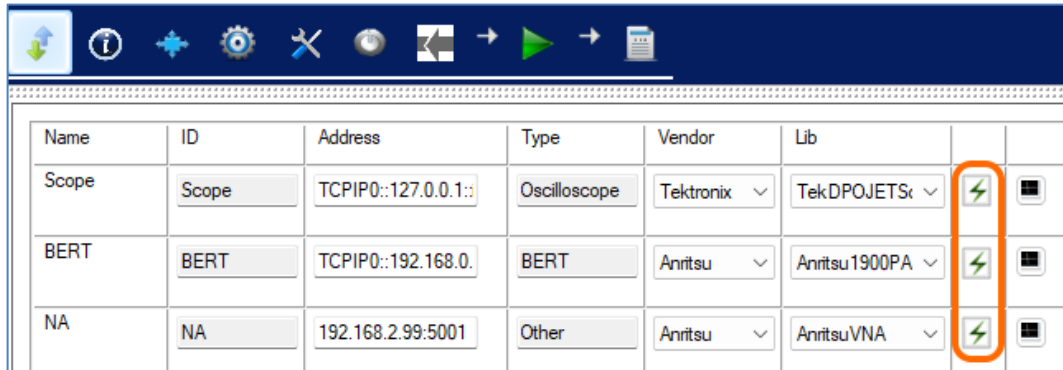


FIGURE 5. GRL PLATFORM SOLUTIONS SOFTWARE INSTRUMENT CONNECTION SETUP

Note: Additional information for connecting the Keysight and Tektronix oscilloscopes to the controller PC is provided in the Appendix of this document.

3.1.3 Set Up Remote File Server

1. The **GRLRemoteProxyServer.exe** will also be installed along with the **USB4V2RxANTestScopeSetupFilesInstallationxxxxxxxxxxSetup.exe** on the Scope. The GRLRemoteProxyServer.exe is installed under the “C:\GRL\GRLRemoteProxyServer” directory.

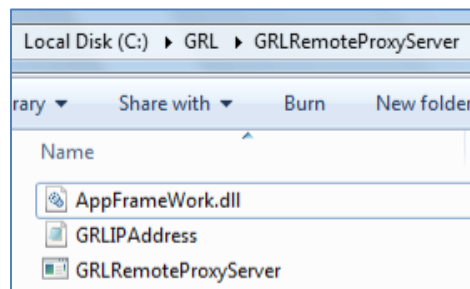


FIGURE 6. INSTALLED GRLREMOTEPROXYSERVER.EXE FILE DIRECTORY

2. If the GRL Platform Solutions software is installed on the PC to control the Scope, the GRLRemoteProxyServer.exe must be run on the Scope to move large waveform files back to the controller PC. The GRL Platform Solutions software will then perform post-processing and analysis of these waveforms using SigTest.
3. When running the GRLRemoteProxyServer.exe, make sure that the controller PC and Scope are connected to the same network, using IP addresses as in following example:
 - Controller PC IP address: 192.168.100.8
 - Scope IP address: 192.168.100.35

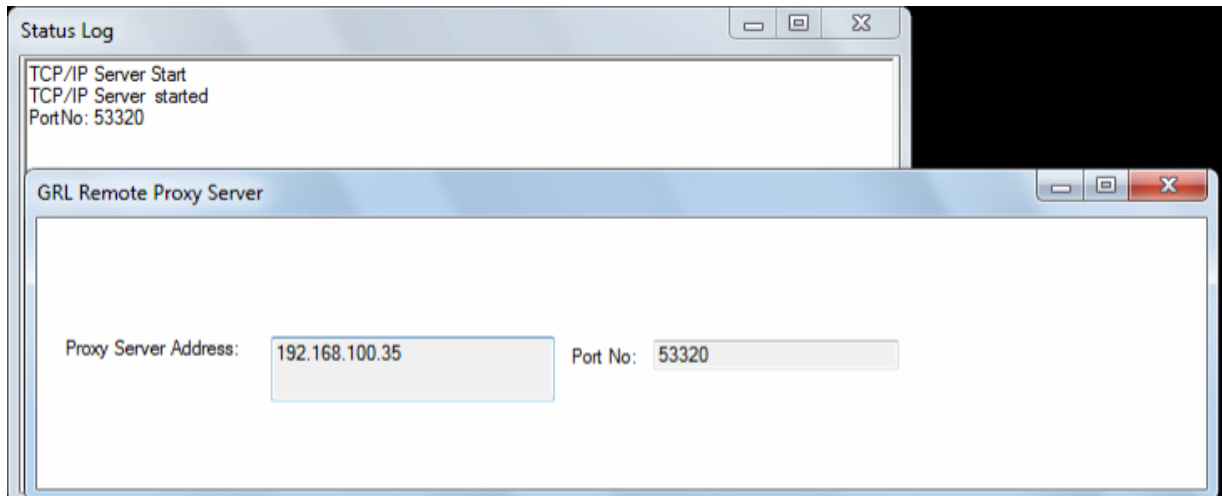


FIGURE 7. VERIFY PROXY SERVER CONNECTION FOR CONTROLLER PC AND SCOPE

4. On the Anritsu USB4 V2 Rx Test Application, go to the Setup Configuration  page and select the “SigTest Setting” tab. Configure the **Remote File Server IP Address** and **Remote File Server Port** parameters to match the network settings of the Remote Proxy Server as shown in the example below:

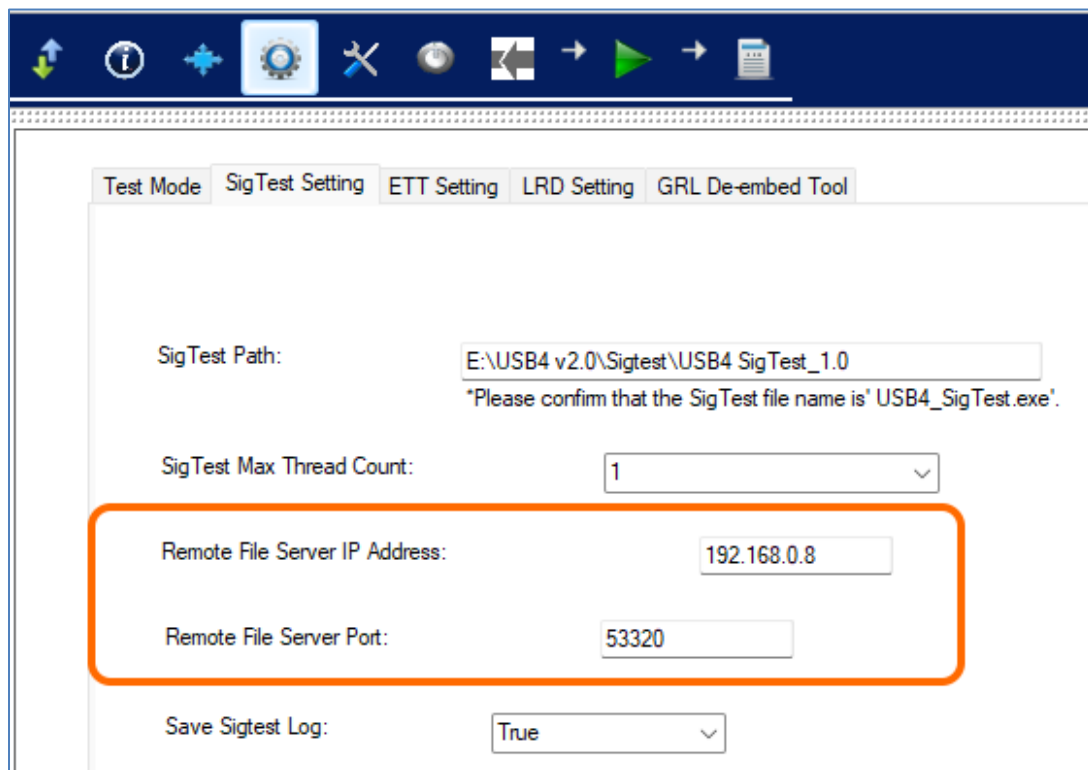


FIGURE 8. CONFIGURE REMOTE PROXY SERVER NETWORK SETTINGS ON GRL PLATFORM SOLUTIONS SOFTWARE

Refer Section 5.4 for more details on parameters available on the Setup Configuration page.

4 Receiver Calibration Setups

The GRL-USB4-V2-RXA test solution supports automated Rx calibration for USB4 Gen 4 electrical specification using the SigTest signal quality and stress tolerance analysis application. To perform calibration, the GRL-USB4-V2-RXA software is run from the PC or oscilloscope to enable automation control for each step of calibration and signal quality test sequence.

Pre-calibration will be performed prior to calibration to measure the insertion loss compensation, maximum intrinsic EVEN-ODD jitter and maximum intrinsic ACCM of the MP1900A BERT. This will be followed by voltage swing calibration, oscilloscope intrinsic noise measurement, calibration at the TP3' (Case 1) and TP3 (Case 2) test points to calibrate for level mismatch, RJ, SNDR (Signal Noise Distortion Ratio), ACCM and UDJ. Calibration will then be performed for the BERT trigger output and clock signal output to be used as aggressor signals during the Rx DUT compliance tests. The BERT assembly step response calibration will also be carried out to check on the BERT output data.

Next, the Gen 4 channel will need to be calibrated for the worst-case condition which will include an ISI trace and a 0.8M USB Type-C passive cable. This includes the link operating margin evaluation for the Rx and Tx lanes of the host/device. The cable is connected in between test receptacle fixtures with ISI channel to measure the trace S4P file with a network analyzer. The trace S4P file will be saved along with other files for post-processing using SigTest.

This will then be followed by adjustments of the PJ magnitude for Case 2. After this, calibration will be performed for receiver frequency variation where it will apply the transmitter frequency variation and verify that the DUT does not lose lock and record errors for Case 1 and Case 2 respectively. Lastly, the LFPS calibration will be carried out to ensure the LFPS signal applied to the Rx DUT meets the exact amplitude, duty cycle, frequency variation and waveform requirements defined by the USB4 V2 CTS.

If a captive device is present, calibration will be performed at the TP2 test point which is defined at the output of a compliance plug fixture or the transmitter port connector output.

When calibration is completed, the GRL-USB4-V2-RXA software will generate a test report detailing all results obtained from the calibration.

The following sections show the calibration setup connection diagrams using the Anritsu MP1900A BERT and a high-performance real-time oscilloscope.

The fixtures and channels used for USB4 Gen 4 calibration and compliance testing are available from USB-IF.

4.1 Connection Setup for Scope Intrinsic Noise Measurement

Figure 9 below shows the setup diagram to measure the intrinsic noise generated by the oscilloscope with no external signal applied. The intrinsic noise waveforms will be captured and saved for SigTest processing in subsequent calibration steps.

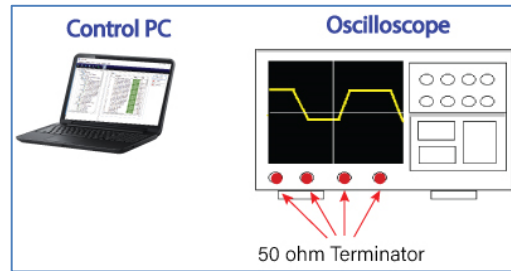


FIGURE 9. SETUP FOR SCOPE INTRINSIC NOISE MEASUREMENT

Connection Step:

Connect 50-ohm terminators to the oscilloscope channels 1 and 3.

4.2 General Calibration Connection Setup

Figure 10 below shows the setup diagram for the following calibration types:

- Voltage Swing Calibration
- Case 1 & Case 2 Calibration (level mismatch, RJ, SNDR, ACCM, UDJ and PJ)
- Aggressor Signal Calibration
- BERT Assembly Step Response Extraction Swing Calibration
- Case 2 PJ Magnitude Adjustment
- Receiver Frequency Variation Calibration

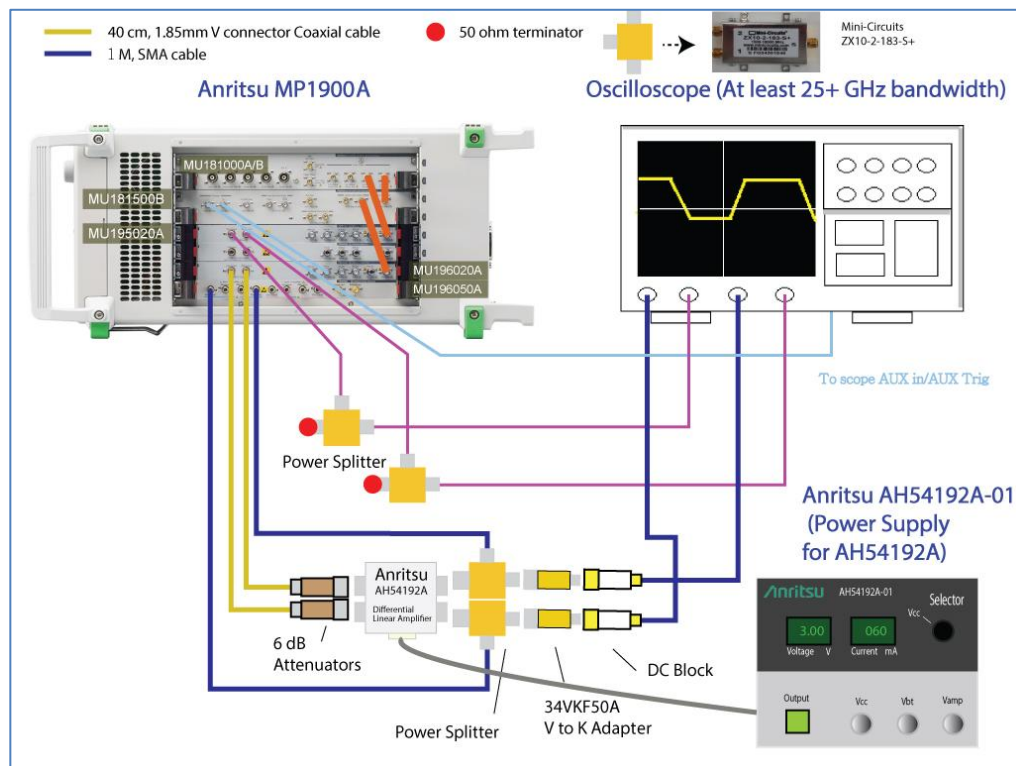


FIGURE 10. GENERAL SETUP FOR USB4 GEN 4 CALIBRATION

Connection Steps:

1. Using J1624A SMA-SMA (0.3m) cables, connect the Clock Outputs of the MU181000A/B Synthesizer to the Ext Clock Inputs of the MU181500B Jitter Modulator and MU195020A SI Pulse Pattern Generator respectively.
2. Using the J1624A SMA-SMA (0.3m) cable, connect the Jittered Clock Output of the MU181500B Jitter Modulator to the Ext Clock Input of the MU196020A PAM4 Pulse Pattern Generator.
3. Using a SMA-SMA (0.5m) cable, connect the MU181500B IQ Output Q to the AUX Input of the MU196020A PAM4 Pulse Pattern Generator.
4. Using a SMA cable, connect the MU181500B IQ Output I to the oscilloscope AUX In/AUX Trig.
5. Using SMA cables, connect the MU195020A Data Outputs to the oscilloscope channels 2 and 4 through V-connector Power Splitters.
6. Using V-connector coaxial (40cm) cables, connect the MU196020A Data Outputs to V-connector 6 dB Attenuators.
7. Connect the V-connector 6 dB Attenuators to the Anritsu AH54192A Differential Linear Amplifier.
8. Using a ribbon cable, connect the Anritsu AH54192A-01 Power Supply to the Anritsu AH54192A Differential Linear Amplifier.
9. Connect another pair of V-connector Power Splitters to the Anritsu AH54192A Differential Linear Amplifier.
10. Using a SMA (1m) cable, connect the MU195050A Data Outputs to the V-connector Power Splitters.
11. Connect the V-connector Power Splitters to the 34VKF50A V to K Adapter.
12. Connect K-connector DC blocks to the 34VKF50A V to K Adapter.
13. Using SMA (1m) cable, connect the K-connector DC blocks to the oscilloscope channels 1 and 3.

4.3 Connection Setup for Case 2 Link Operating Margin Evaluation (RX & TX) Calibration

Figure 11 to Figure 14 show the calibration setup diagrams for link operating margin evaluation for RX0, RX1, TX0 and TX1 lanes of the DUT using an ISI channel, USB-IF test receptacle fixture and a 0.8M USB Type-C passive cable.

Note: The test receptacle fixture must be de-embedded from the physical channel s4p trace (Test_Channel.S4P file).

Note: Calibration for the RX1 and TX1 link operating margin evaluation are optional and not mandatory for compliance.

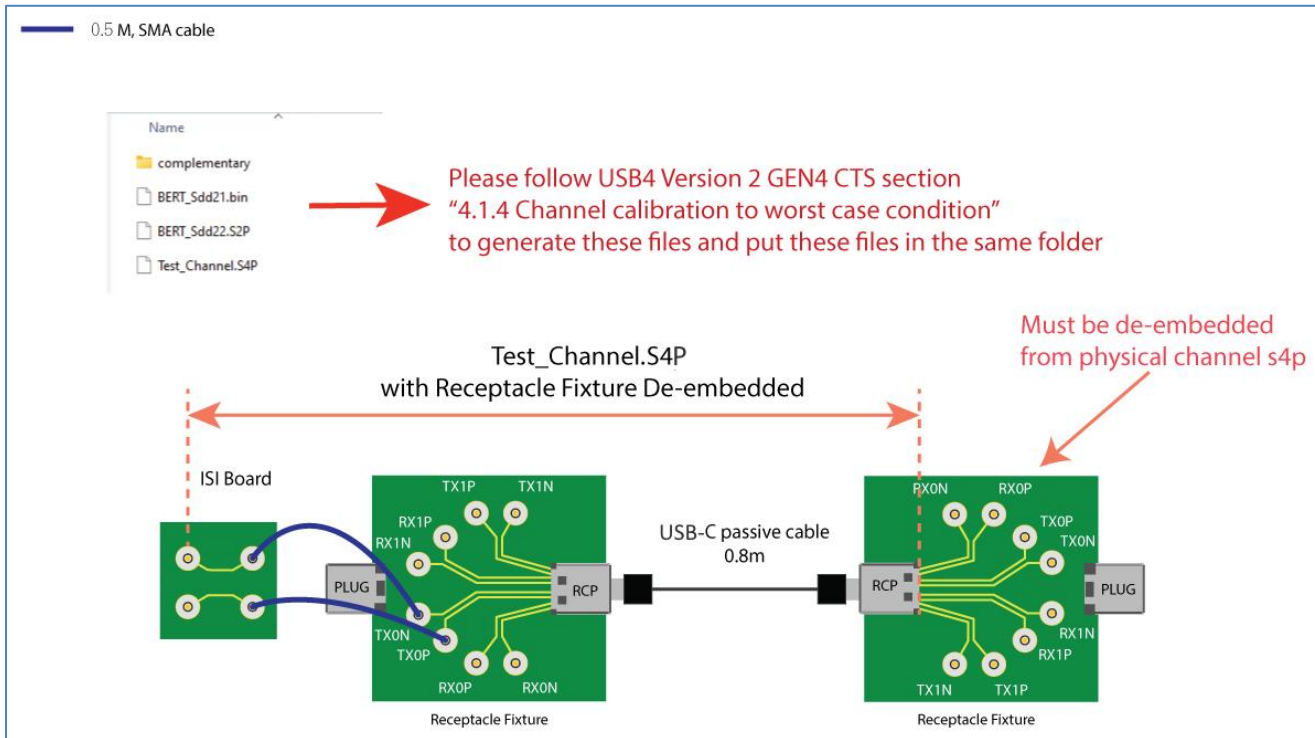


FIGURE 11. SETUP FOR LINK OPERATING MARGIN EVALUATION FOR RX0

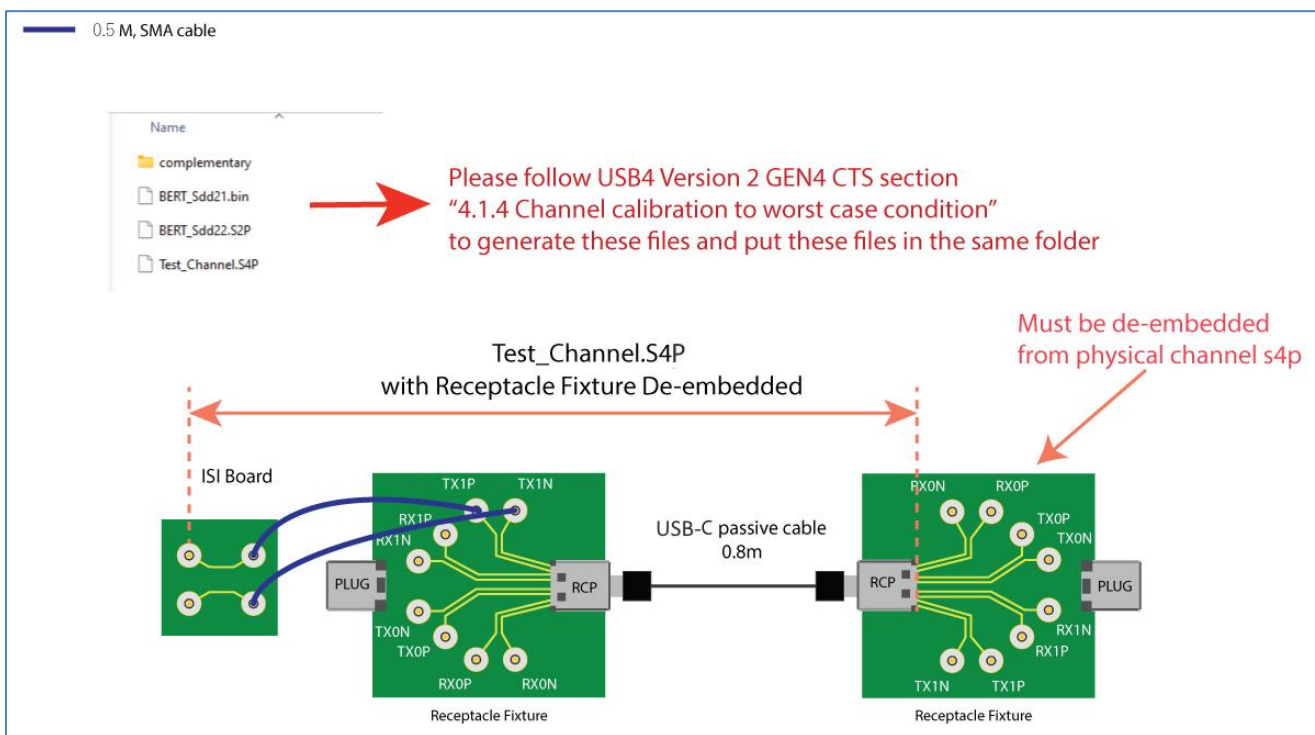


FIGURE 12. SETUP FOR LINK OPERATING MARGIN EVALUATION FOR RX1 (OPTIONAL)

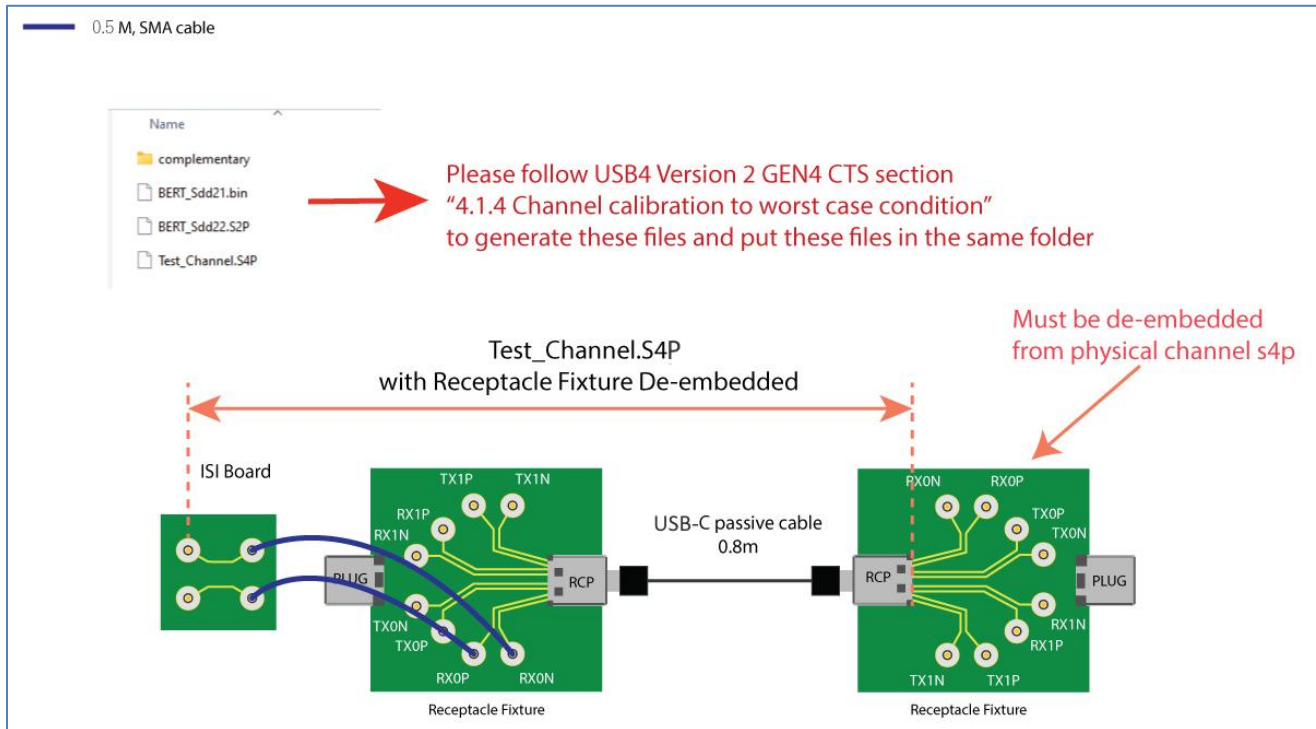


FIGURE 13. SETUP FOR LINK OPERATING MARGIN EVALUATION FOR TX0

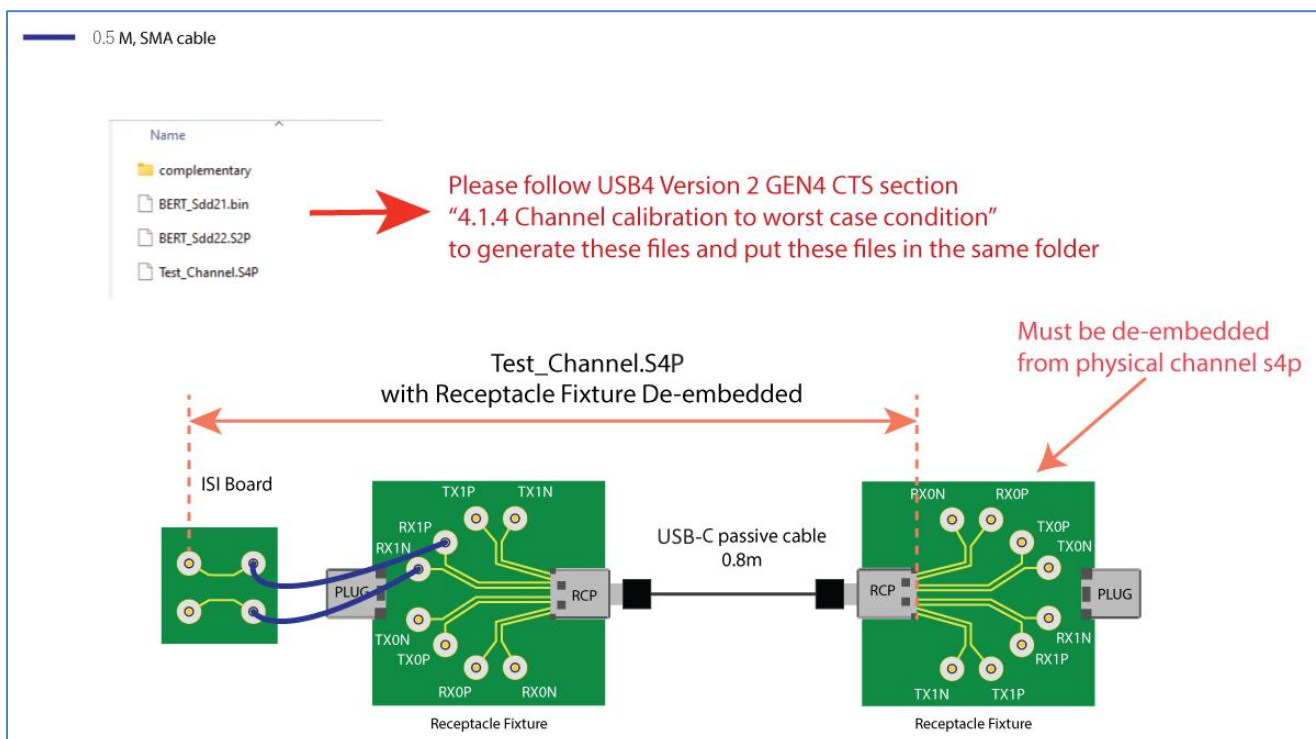


FIGURE 14. SETUP FOR LINK OPERATING MARGIN EVALUATION FOR TX1 (OPTIONAL)

Connection Steps:

1. Set up the connection as shown above.
2. Refer to the procedure in USB4 Version 2 GEN 4 CTS section “4.1.4 Channel calibration to worst case condition” to generate the following files:
 - BERT_Sdd21.bin
 - BERT_Sdd22.S2P
 - Test_Channel.S4P
3. Place the above files in the same folder, which is the path specified in the “RX0/RX1/TX0/TX1 Channel Worst Case Condition Files Path” configuration.

5 Calibrating Using GRL-USB4-V2-RXA Software

5.1 Enter Calibration/Test Session Information

Select  from the software menu to access the **Session Info** page. Enter the information as required for the calibration/test session that is currently being run. The information provided will be included in the test report generated by the software once calibration/tests are completed.

- The fields under **DUT Info** and **Test Info** are defined by the user.
- The **Software Info** field is automatically populated by the software.

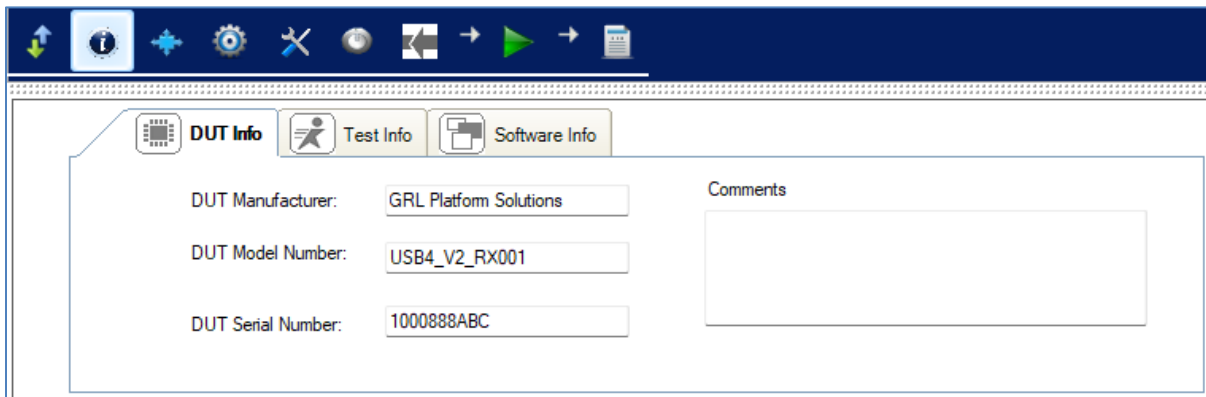


FIGURE 15. ENTER CALIBRATION/TEST SESSION INFORMATION

5.2 Set Up Conditions for Calibration/Testing

Select  from the software menu to access the Conditions page.

In this section, conditions for calibration and testing will need to be set.

Note: The condition options prefixed with 'LRD' are applicable only to LRD test cases.

1. Select the **Test Point(s)** for calibration and testing:
 - “Case 1” for the receiver DUT setup with low insertion loss. This applies to the Case 1 calibration and tests.
 - “Case 2” for the receiver DUT setup with maximum insertion loss. This applies to the Case 2a (passive cable) and Case 2b (LRD cable) calibration only.
 - “Case 2a” for the passive cable setup with maximum insertion loss which requires the receiver DUT to be connected with a USB4 Gen 4 passive cable. This applies to the Case 2a TER tests only.
 - “Case 2b” for the linear re-driver (LRD) cable setup with maximum insertion loss which requires the receiver DUT to be connected with a USB Type-C LRD cable. This applies to the Case 2b TER tests only.
 - “Captive Device” for the captive device calibration and tests at TP3 Prime. The TP3 Prime test point is defined at the output of a compliance plug fixture.

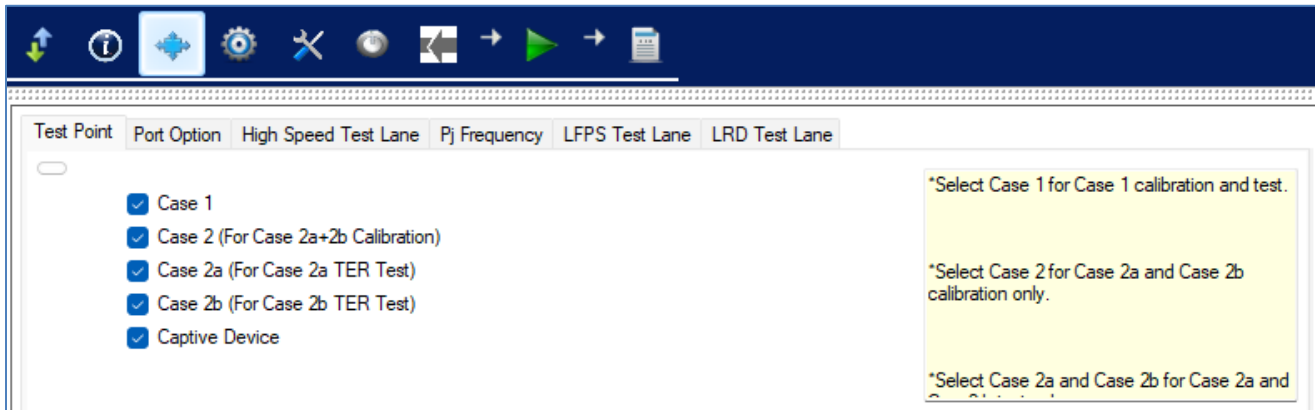


FIGURE 16. SELECT TEST POINTS FOR CALIBRATION AND TESTING

2. Select the test **Port Option** consisting of the USB4 Symmetric Link (where the number of TX and RX lanes are the same, e.g. “1*TX/1*RX” or “2*TX/2*RX”) or Asymmetric Link (where one side transmits e.g. “3*TX/1*RX” while the other side transmits “1*TX/3*RX” or 3 transmit lanes from one side and 3 receive lanes toward that side “3*TX/3*RX”).

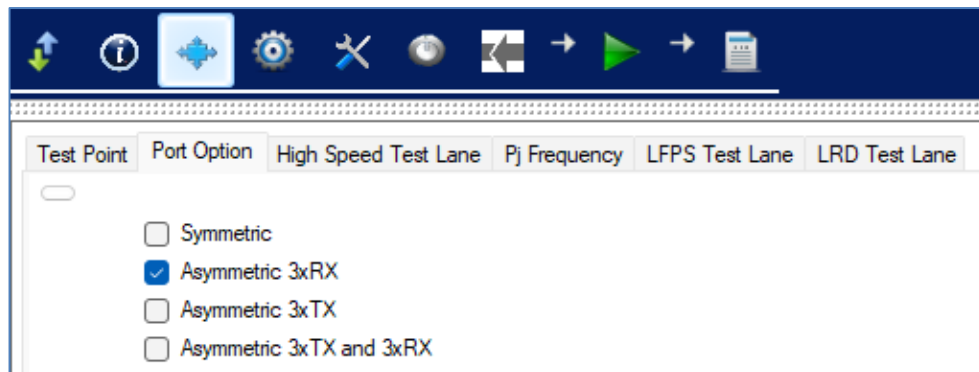


FIGURE 17. SELECT USB4 SYMMETRIC LINK OR ASYMMETRIC LINK

3. Select the **High Speed Test Lane(s)** for the above selected Symmetric Link or Asymmetric Link.

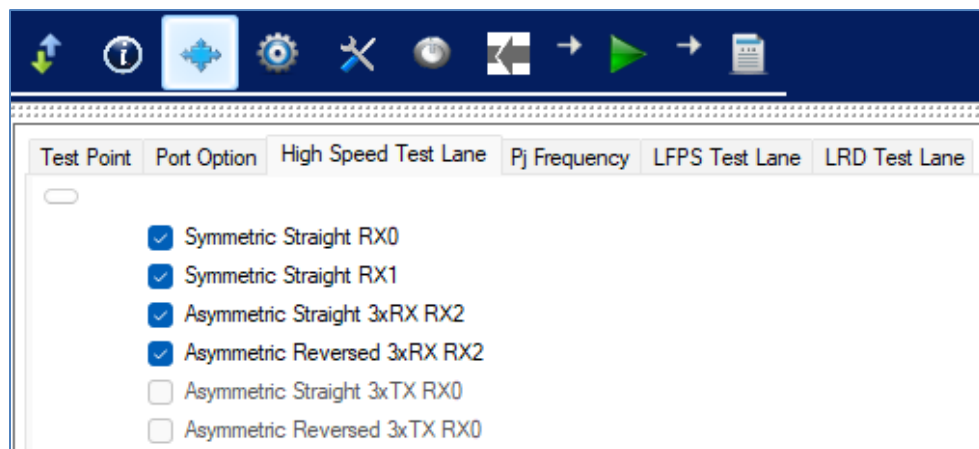


FIGURE 18. SELECT HIGH SPEED TEST LANES FOR SYMMETRIC OR ASYMMETRIC LINK

4. Select the PJ Frequency(s).

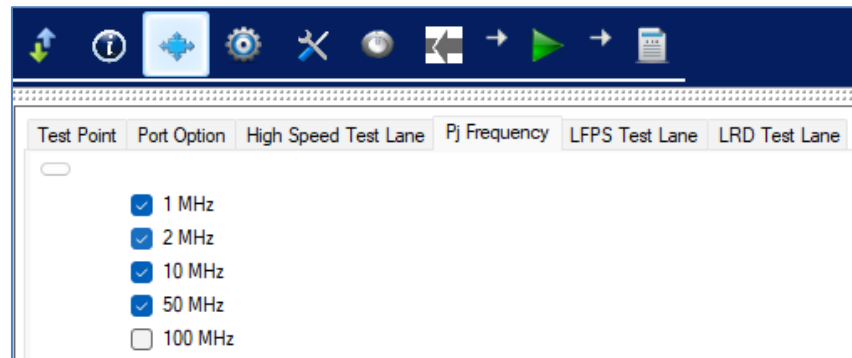


FIGURE 19. SELECT PJ FREQUENCY

5. Select the **LFPS Test Lane(s)** for the above selected Symmetric Link or Asymmetric Link. The selected LFPS test lane(s) will be stimulated with the LFPS signal and monitored for correct LFPS detection behavior.

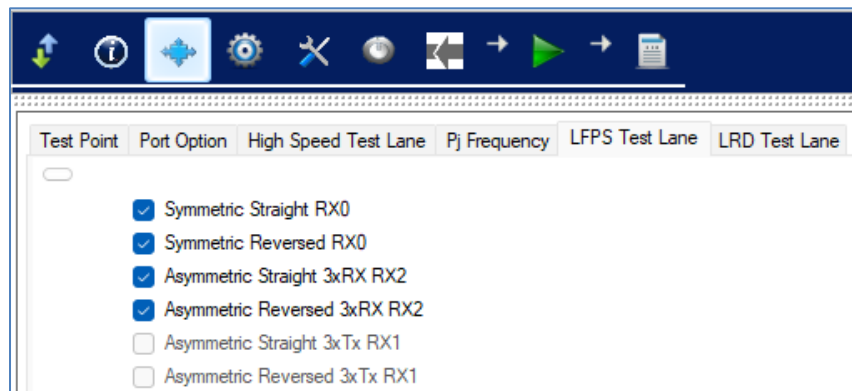


FIGURE 20. SELECT LFPS TEST LANES FOR SYMMETRIC OR ASYMMETRIC LINK

6. Select the **LRD Test Lane(s)** to verify the Rx DUT's ability to handle USB4 V2 high-speed traffic under compliance stress conditions.

Note: To access and run the LRD tests, the user is required to purchase the “GRL-USB4V2-LRD-AN” license from GRL Platform Solutions @ support@grlps.com.

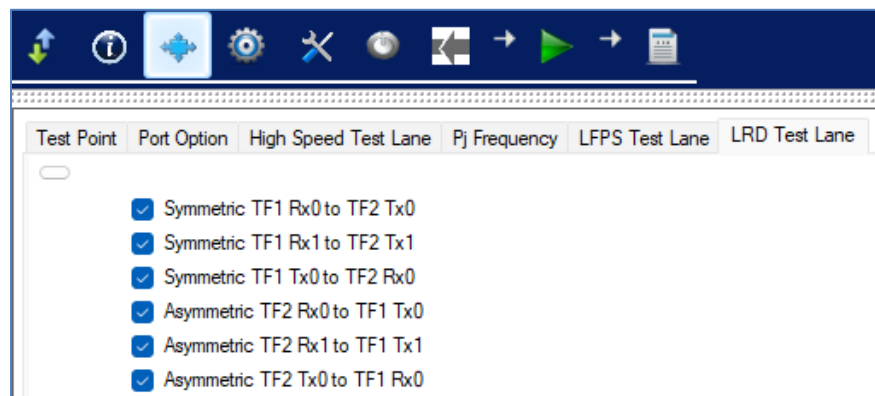


FIGURE 21. SELECT LRD TEST LANES FOR SYMMETRIC OR ASYMMETRIC LINK

5.3 Select Calibration

The test selection page allows calibration/tests that need to be performed to be selected. Initially when starting for the first time or changing anything in the setup, it is suggested to run Calibration first. If the calibration is not completed, the Rx Tests will throw an error message.

The GRL-USB4-V2-RXA software automatically runs the selected calibration when initiated. See Section 5.8 on running the calibration.

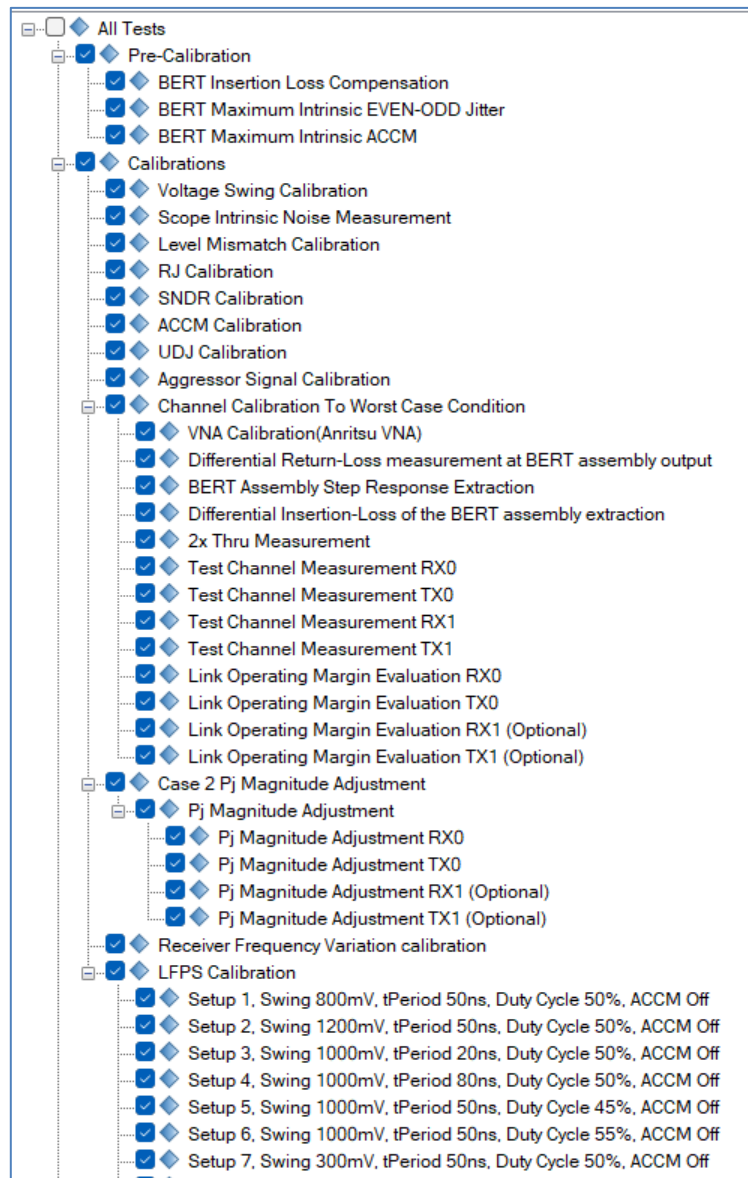


FIGURE 22. SELECT CALIBRATION

Note: The marking shown on the left of each test parameter indicates the status of the calibration/test result of the parameter. In the above example,  indicates that calibration/testing has not been run for the specific calibration/test parameter. When calibration/testing has been run and completed successfully for the specific calibration/test parameter with a Pass result, this will be indicated with .

5.4 Set Up SigTest Environment

SigTest allows waveforms captured with the oscilloscope to be analyzed and checked against the specified pass/fail criteria.

Select  from the software menu to access the Setup Configuration page.

Select the **SigTest Setting** tab to set up the SigTest components as described below:

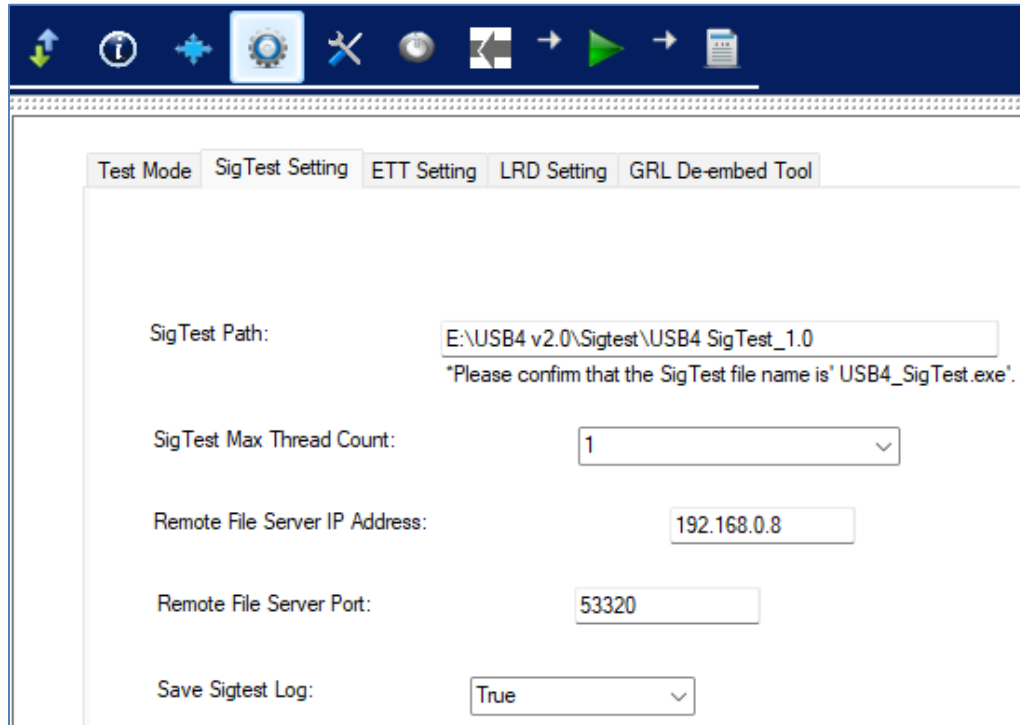


FIGURE 23. CONFIGURE SIGTEST

1. Enter the full **SigTest Path** in the test controller system. Ensure that the SigTest file name is “USB4_SigTest.exe”.
2. Select the **SigTest Max Thread Count** to generate the maximum process threads for checking the Rx device functionality when running SigTest.
3. Enter the **Remote File Server IP Address** and **Port** number for the GRL Platform Solutions Remote Proxy Server. See Section 3.1.3 on how to set up the remote file server.
4. Set the **Save SigTest Log** to “True” to generate a detailed log of all activities during the SigTest run.

5.5 Perform De-embedding of Test Receptacle Fixture

The GRL De-embed Tool can be used to de-embed the test receptacle fixture from the physical channel S4P trace (Test_Channel.s4p file) for the Case 2 link operating margin evaluation (Rx & Tx) calibration. The test channel with receptacle fixture trace de-embedded S-parameters will be used in the link operating margin evaluation calibration.

Select  from the software menu to access the Setup Configuration page.

Select the **GRL De-embed Tool** tab to call the respective S4P files for the test receptacle fixture de-embedding:

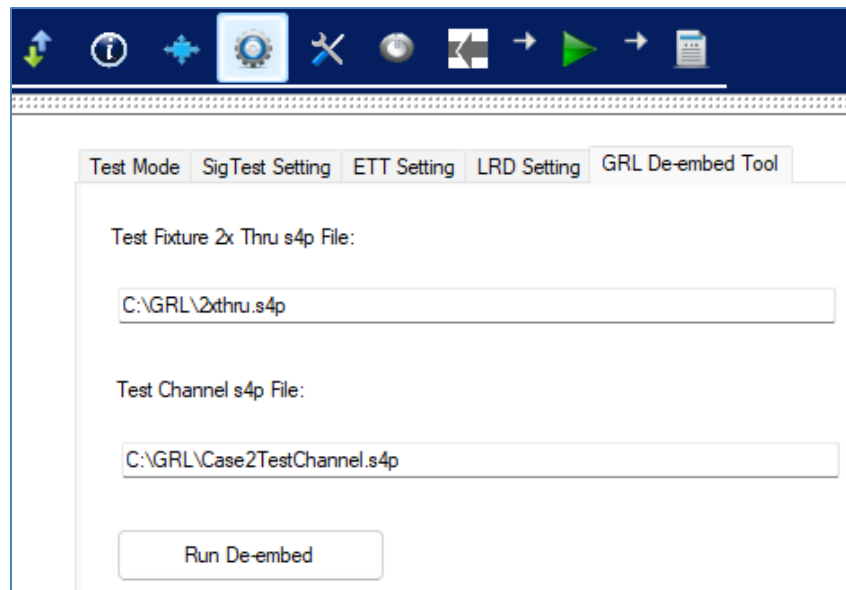


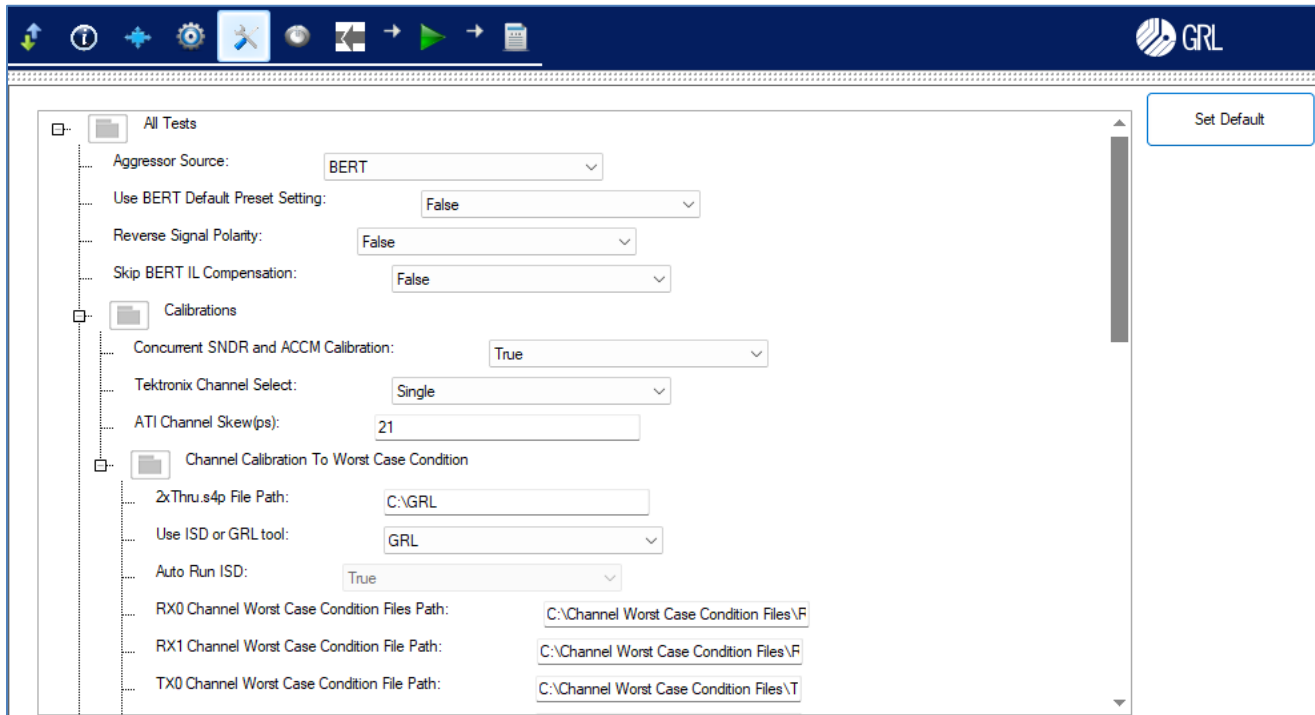
FIGURE 24. SET UP DE-EMBEDDING OF TEST RECEPTACLE FIXTURE

- In the **Test Fixture 2x Thru s4p File** field, enter the S4P file path of the captured test channel S-parameters for the receptacle test fixture trace loss de-embedding via the 2xThru structure.
- In the **Test Channel s4p File** field, enter the S4P trace file path of the physical channel.
- Click on the **Run De-embed** button to start the de-embedding process.

5.6 Configure Calibration Parameters

After selecting the desired calibration and setting up SigTest, select  from the software menu to access the Configurations page. Set the required parameters for calibration as described below.

To return all parameters to their default values, select the ‘Set Default’ button.



The screenshot shows the GRL software interface with the 'Configurations' page selected. The 'All Tests' section is expanded, showing various parameters. The 'Calibrations' section is also expanded, showing parameters for concurrent SNDR and ACCM calibration, Tektronix channel select, ATI channel skew, and channel calibration to worst case condition. The 'Set Default' button is visible in the top right corner.

FIGURE 25. CONFIGURE CALIBRATION PARAMETERS

TABLE 4. ALL TESTS PARAMETERS DESCRIPTION

Parameter	Description
Aggressor Source	Select the Aggressor source from the MP1900A BERT SI Pulse Pattern Generator or using an external signal generator.
Use BERT Default Preset Setting	“False” is usually the case of which the GRL Platform Solutions software will apply the calibrated preset setting from the Preset Calibration to the TER test. If you change this to “True”, the default preset setting of the MP1900A BERT will be used.
Reverse Signal Polarity	“False” is usually the case. If you change this to “True”, reverse polarity for the signal is enabled.
Skip BERT IL Compensation	“False” is usually the case. If you change this to “True”, compensation for the insertion loss (IL) by the MP1900A BERT will be skipped.

TABLE 5. CALIBRATION PARAMETERS DESCRIPTION

Parameter	Description
Concurrent SNDR and ACCM Calibration	“True” is usually the case. Select “False” to disable the SNDR and ACCM calibration from happening in tandem.
Tektronix Channel Select	If using the Tektronix scope, select either the Single-shot based scope or the Tektronix' owned Dual Asynchronous Time Interleaving (Dual ATI) based scope.
ATI Channel Skew (ps)	If using the Tektronix ATI based scope, enter the channel skew or timing to perform alignment of the scope channels.
2xThru.s4p File Path	Enter the path to save the captured test channel S-parameters in s4p format for the receptacle test fixture trace loss de-embedding using the 2xThru structure.
Use ISD or GRL tool	Select one of the following tools to perform de-embedding of the channel test fixture. - The “ISD” or In-Situ De-embedding tool can be used to remove the effects of test fixture components when measuring the USB4 V2 Case 2 test channel. If ISD is selected, the GRL Platform Solutions software will request the user to perform de-embedding on their own. - If “GRL” is selected, the GRL Platform Solutions software will utilize the GRL Platform Solutions tool to perform de-embedding of the test fixture.
Auto Run ISD	If the “ISD” tool is selected, “True” is usually the case where the ISD is automatically executed. Otherwise, select “False” to cancel this process.
RX0 Channel Worst Case Condition Files Path	Enter the path to save the RX0 Channel Worst Case Condition file and the waveform file generated from the BERT Assembly Step Response Extraction Swing Calibration. This configuration only applies for Case 2.
RX1 Channel Worst Case Condition Files Path	Enter the path to save the RX1 Channel Worst Case Condition file and the waveform file generated from the BERT Assembly Step Response Extraction Swing Calibration. This configuration only applies for Case 2.
TX0 Channel Worst Case Condition Files Path	Enter the path to save the TX0 Channel Worst Case Condition file and the waveform file generated from the BERT Assembly Step Response Extraction Swing Calibration. This configuration only applies for Case 2.
TX1 Channel Worst Case Condition Files Path	Enter the path to save the TX1 Channel Worst Case Condition file and the waveform file generated from the BERT Assembly Step Response Extraction Swing Calibration. This configuration only applies for Case 2.

5.7 Configure Calibration Target Values

For debugging purposes ONLY, the default calibration target values can be changed for the respective calibration. To do this, select  from the menu to access the Calibration page.

By default, the calibration target values are those defined in the specification. To change the values, un-select the 'Use Default Value' checkbox. In case the default values are required again, just select the checkbox to allow all existing values to be reset to default.

Note: The PID Control setting is used to adjust the step width for steps calculation if the target measurement cannot be met with the current step. To adjust, use a lower PID Control value to reduce the subsequent step or increase the control value to make the subsequent step bigger.

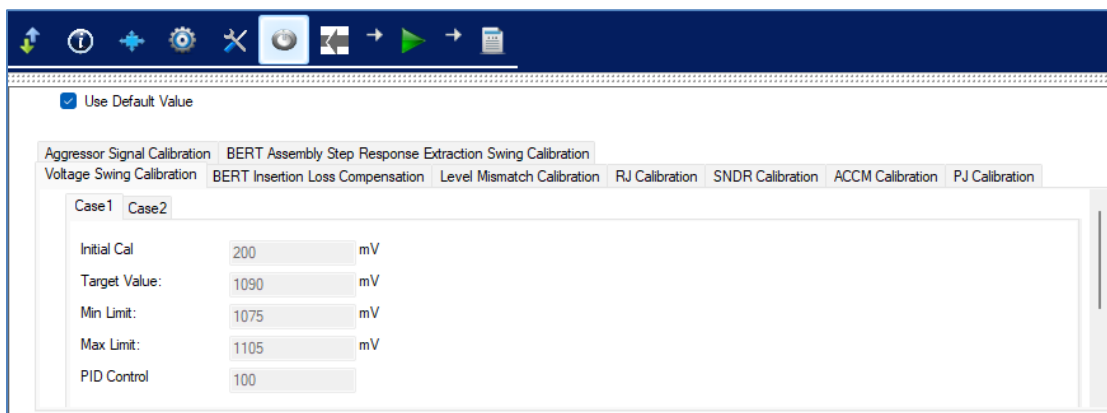


FIGURE 26. CALIBRATION TARGET OVERWRITE PAGE

5.8 Run Calibration

Select  in the main software menu to access the Run Tests page.

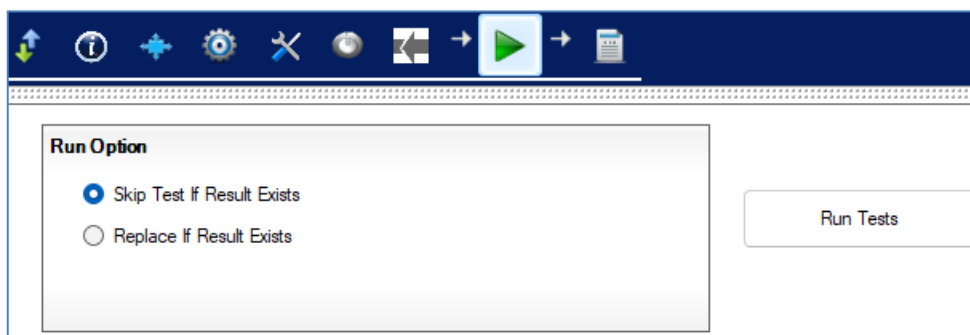


FIGURE 27. RUN CALIBRATION

Select the Run Option before clicking the “Run Tests” button to start selected calibration:

- **Skip Test if Result Exists.** If previous calibration results exist, then the software will *skip* the calibration steps that have existing reports.
- **Replace if Result Exists.** If previous calibration results exist, then the software will *replace* each step in the calibration with new results.

When calibration is running, the connection setup diagram of the respective calibration will initially appear as a guide for the user to make sure all connections are proper before calibration is performed.

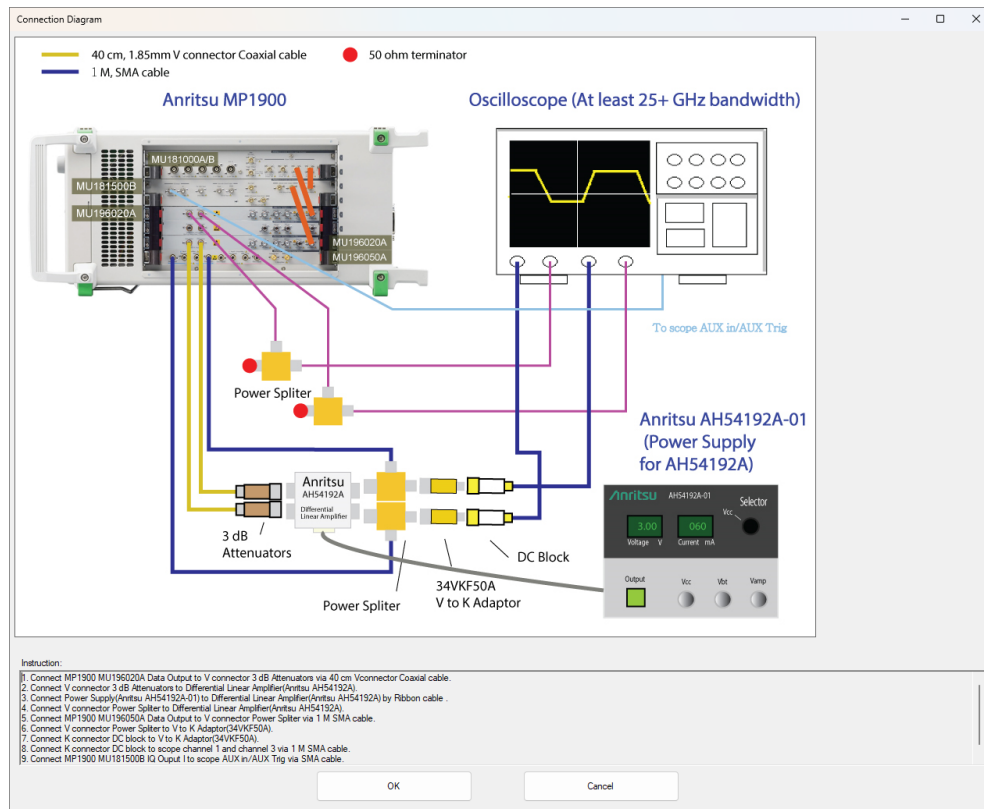


FIGURE 28. CONNECTION SETUP DIAGRAM DIALOG EXAMPLE

If you need to re-run only certain calibration on certain conditions, delete the calibration results from the Report tab and Run with **Skip Test if Result Exists**. The GRL Platform Solutions software will keep track of the missing calibration results in the report and perform those calibration only. See Section 7.2, Delete Test Results for details.

6 Compliance Testing Using GRL-USB4-V2-RXA Software

After calibration has completed successfully, testing for receiver TER (Trit Error Ratio) compliance, frequency variation, LFPS and LRD as well as aggressor signal monitoring can then be performed. The GRL-USB4-V2-RXA software automates the Gen 4 receiver compliance testing for TER of $1E-8$ or lower without FEC (Forward Error Correction), at the spec-defined jitter frequency steps. The DUT will also undergo signal frequency variations during Link training for the Case 1 and Case 2 setups, before obtaining steady state.

LFPS (Low Frequency Periodic Signaling) testing is used to verify that the DUT can correctly detect and respond to LFPS signaling sequences used for link initialization, power management and mode transitions. LRD testing is performed to ensure the DUT works correctly with Linear Re-Driver (LRD) active cables.

The GRL-USB4-V2-RXA software also performs aggressor signal checks to ensure that the intended crosstalk stress is being applied to the DUT during compliance testing.

When testing is completed, the results will be logged in an aggregated test report which can be generated into PDF format.

6.1 Connection Setups for Receiver TER Testing

This section describes the test setups for the host/device DUT using the USB4 V2 microcontroller and MP1900A BERT. Test scripts as listed in Section 2.2 are required to run the automation tests. Also refer to Section 3.1.1 for options on how to configure the test setup.

6.1.1 MP1900A BERT Standard Modes

The MP1900A BERT has three modes for USB4 V2 Rx calibration and testing: **Standard BERT for PAM4 with MU196050A**, **Standard BERT for PAM4 with MU195050A** and **Standard BERT for SI**. The differences between these modes are in the BERT modules used and the slot configurations. Therefore, the connection setup of each mode will also be different.

6.1.1.1 Standard BERT for PAM4 with MU196050A Mode

Figure 29 below shows the setup diagram using the Standard BERT for PAM4 with MU196050A mode with the following BERT modules and slot configurations:

- MU195020A SI Pulse Pattern Generator at slot 5
- MU196020A PAM4 Pulse Pattern Generator at slot 7
- MU196050A Noise Generator at slot 8

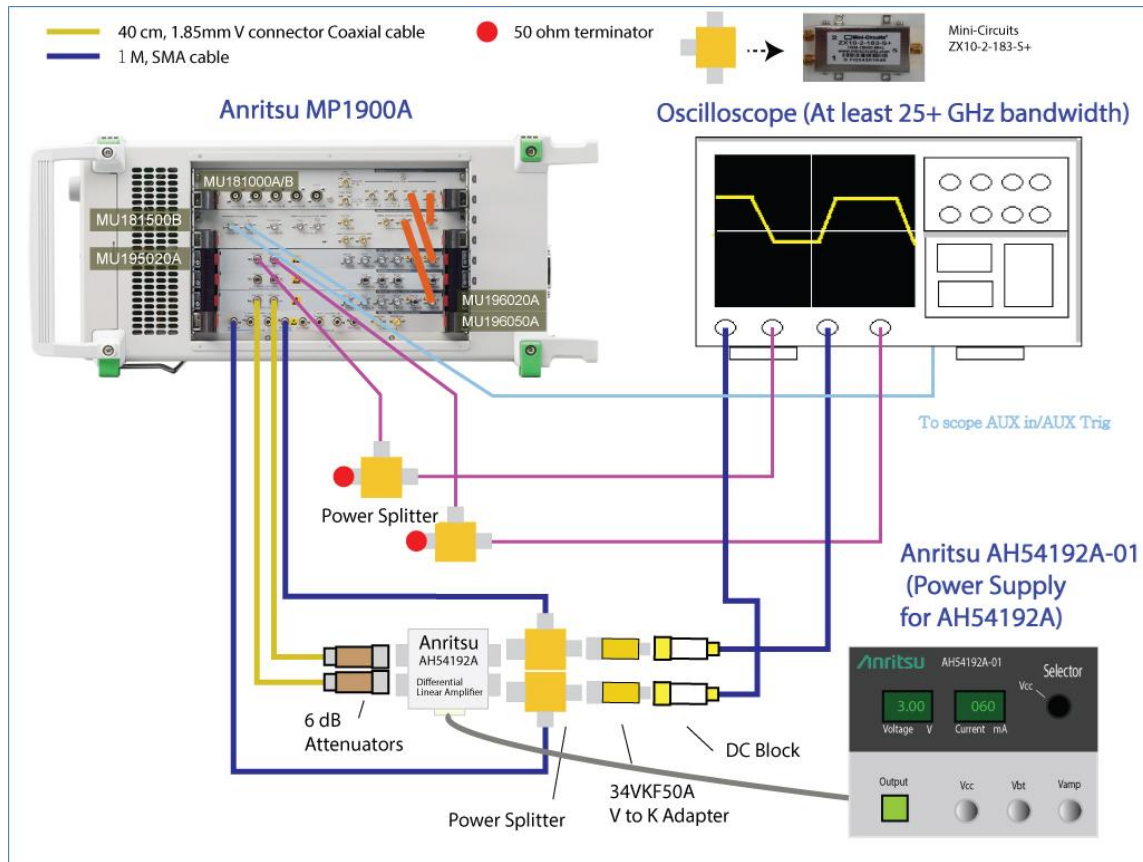


FIGURE 29. STANDARD BERT FOR PAM4 WITH MU196050A SETUP

Connection Steps:

1. Using J1624A SMA-SMA (0.3m) cables, connect the Clock Outputs of the MU181000A/B Synthesizer to the Ext Clock Inputs of the MU181500B Jitter Modulator and MU195020A SI Pulse Pattern Generator respectively.
2. Using the J1624A SMA-SMA (0.3m) cable, connect the Jittered Clock Output of the MU181500B Jitter Modulator to the Ext Clock Input of the MU196020A PAM4 Pulse Pattern Generator.
3. Using a SMA-SMA (0.5m) cable, connect the MU181500B IQ Output Q to the AUX Input of the MU196020A Pulse Pattern Generator.
4. Using a SMA cable, connect the MU181500B IQ Output I to the oscilloscope AUX In/AUX Trig.
5. Using SMA cables, connect the MU195020A Data Outputs to the oscilloscope channels 2 and 4 through V-connector Power Splitters.
6. Using V-connector coaxial (40cm) cables, connect the MU196020A Data Outputs to V-connector 6 dB Attenuators.
7. Connect the V-connector 6 dB Attenuators to the Anritsu AH54192A Differential Linear Amplifier.
8. Using a ribbon cable, connect the Anritsu AH54192A-01 Power Supply to the Anritsu AH54192A Differential Linear Amplifier.

9. Connect another pair of V-conductor Power Splitters to the Anritsu AH54192A Differential Linear Amplifier.
10. Using a SMA (1m) cable, connect the MU196050A Data Outputs to the V-conductor Power Splitters.
11. Connect the V-conductor Power Splitters to the 34VKF50A V to K Adapter.
12. Connect K-conductor DC blocks to the 34VKF50A V to K Adapter.
13. Using SMA (1m) cable, connect the K-conductor DC blocks to the oscilloscope channels 1 and 3.

6.1.1.2 Standard BERT for PAM4 with MU195050A Mode

Figure 30 below shows the setup diagram using the Standard BERT for PAM4 with MU195050A mode with the following BERT modules and slot configurations:

- MU195020A SI Pulse Pattern Generator at slot 5
- MU196020A PAM4 Pulse Pattern Generator at slot 7
- MU195050A Noise Generator at slot 8

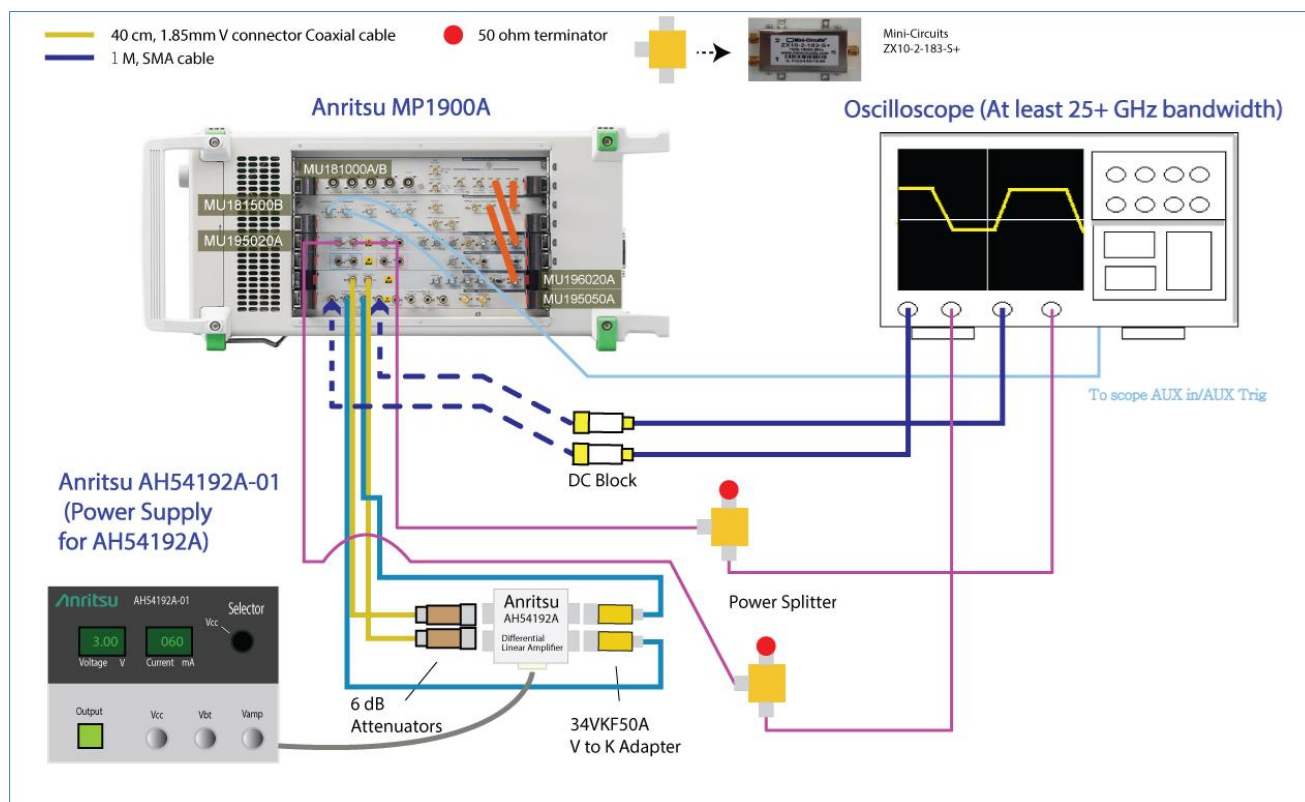


FIGURE 30. STANDARD BERT FOR PAM4 WITH MU195050A SETUP

Connection Steps:

1. Using J1624A SMA-SMA (0.3m) cables, connect the Clock Outputs of the MU181000A/B Synthesizer to the Ext Clock Inputs of the MU181500B Jitter Modulator and MU195020A SI Pulse Pattern Generator respectively.

2. Using the J1624A SMA-SMA (0.3m) cable, connect the Jittered Clock Output of the MU181500B Jitter Modulator to the Ext Clock Input of the MU196020A PAM4 Pulse Pattern Generator.
3. Using a SMA-SMA (0.5m) cable, connect the MU181500B IQ Output Q to the AUX Input of the MU196020A PAM4 Pulse Pattern Generator.
4. Using a SMA cable, connect the MU181500B IQ Output I to the oscilloscope AUX In/AUX Trig.
5. Using SMA cables, connect the MU195020A Data Outputs to the oscilloscope channels 2 and 4 through V-connector Power Splitters.
6. Using V-connector coaxial (40cm) cables, connect the MU196020A Data Outputs to V-connector 6 dB Attenuators.
7. Connect the V-connector 6 dB Attenuators to the Anritsu AH54192A Differential Linear Amplifier.
8. Using a ribbon cable, connect the Anritsu AH54192A-01 Power Supply to the Anritsu AH54192A Differential Linear Amplifier.
9. Connect the 34VKF50A V to K Adapter to the Anritsu AH54192A Differential Linear Amplifier.
10. Using a SMA (1m) cable, connect the 34VKF50A V to K Adapter to the MU195050A Data Inputs.
11. Using a SMA (1m) cable, connect the MU195050A Data Outputs to the oscilloscope channels 1 and 3 through DC blocks.

6.1.1.3 Standard BERT for SI Mode

Figure 31 below shows the setup diagram using the Standard BERT for SI mode with the following BERT modules and slot configurations:

- MU195020A SI Pulse Pattern Generator at slot 7
- MU196020A PAM4 Pulse Pattern Generator at slot 5
- MU195050A Noise Generator at slot 8

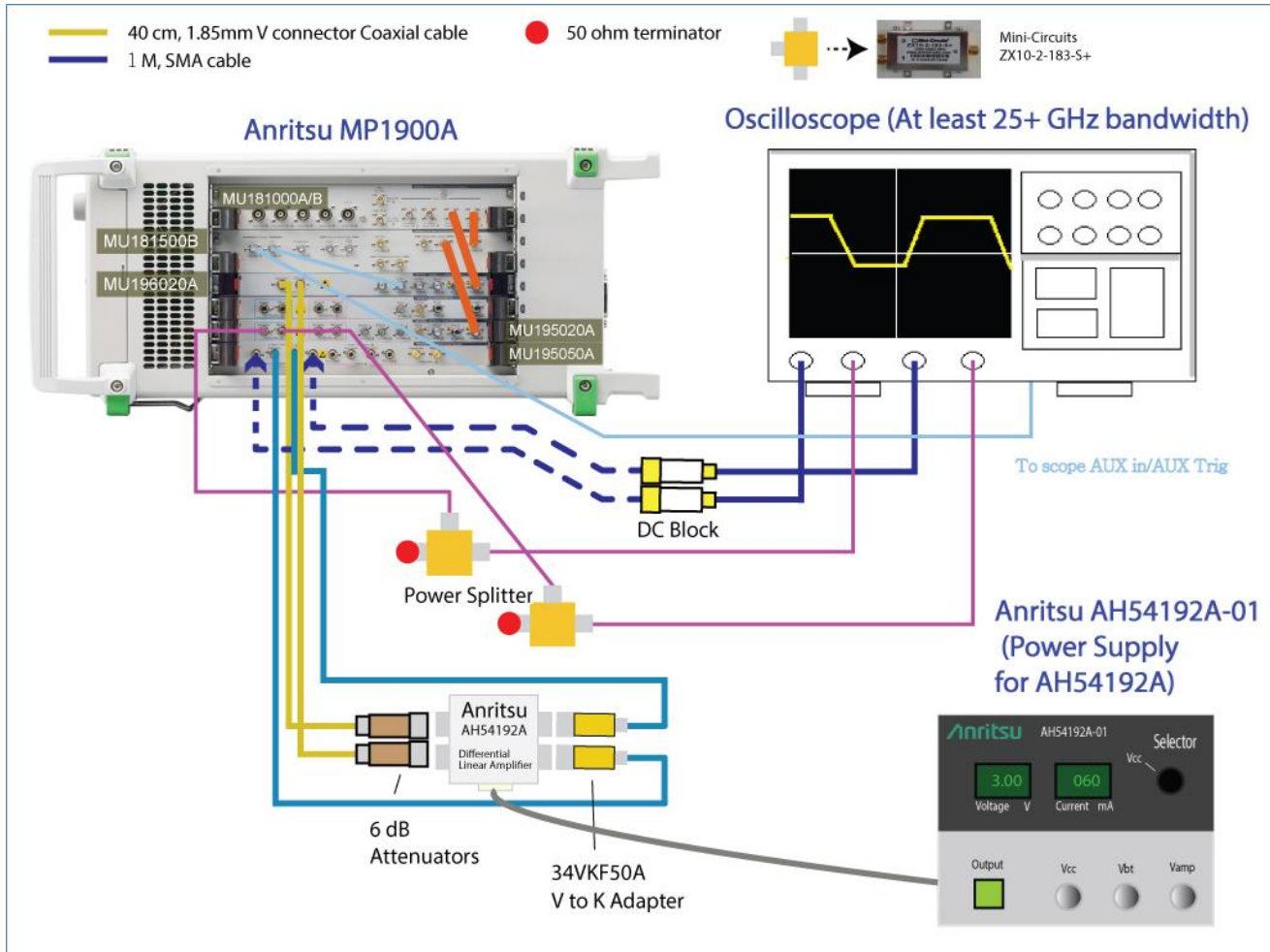


FIGURE 31. STANDARD BERT FOR SI

Connection Steps:

1. Using J1624A SMA-SMA (0.3m) cables, connect the Clock Outputs of the MU181000A/B Synthesizer to the Ext Clock Inputs of the MU181500B Jitter Modulator and MU195020A SI Pulse Pattern Generator respectively.
2. Using the J1624A SMA-SMA (0.3m) cable, connect the Jittered Clock Output of the MU181500B Jitter Modulator to the Ext Clock Input of the MU196020A PAM4 Pulse Pattern Generator.
3. Using a SMA-SMA (0.5m) cable, connect the MU181500B IQ Output Q to the AUX Input of the MU196020A PAM4 Pulse Pattern Generator.
4. Using a SMA cable, connect the MU181500B IQ Output I to the oscilloscope AUX In/AUX Trig.
5. Using SMA cables, connect the MU195020A Data Outputs to the oscilloscope channels 2 and 4 through V-connector Power Splitters.
6. Using V-connector coaxial (40cm) cables, connect the MU196020A Data Outputs to V-connector 6 dB Attenuators.

7. Connect the V-connector 6 dB Attenuators to the Anritsu AH54192A Differential Linear Amplifier.
8. Using a ribbon cable, connect the Anritsu AH54192A-01 Power Supply to the Anritsu AH54192A Differential Linear Amplifier.
9. Connect the 34VKF50A V to K Adapter to the Anritsu AH54192A Differential Linear Amplifier.
10. Using a SMA (1m) cable, connect the 34VKF50A V to K Adapter to the MU195050A Data Inputs.
11. Using a SMA (1m) cable, connect the MU195050A Data Outputs to the oscilloscope channels 1 and 3 through DC blocks.

6.1.2 TER Test Setup for Case 1

6.1.2.1 Standard BERT for PAM4 with MU195050A Mode

Figure 32 shows the USB4 V2 host/device DUT test setup diagram for Case 1 using the USB4 V2 microcontroller and the MP1900A BERT for the Standard BERT for PAM4 with MU195050A mode. The calibrated stressed signal is attached to the test fixture and crosstalk is added to the fixture from the MP1900A MU195020A SI Pulse Pattern Generator which generates aggressor signals. The microcontroller is used to directly control the DUT by executing the ETT.

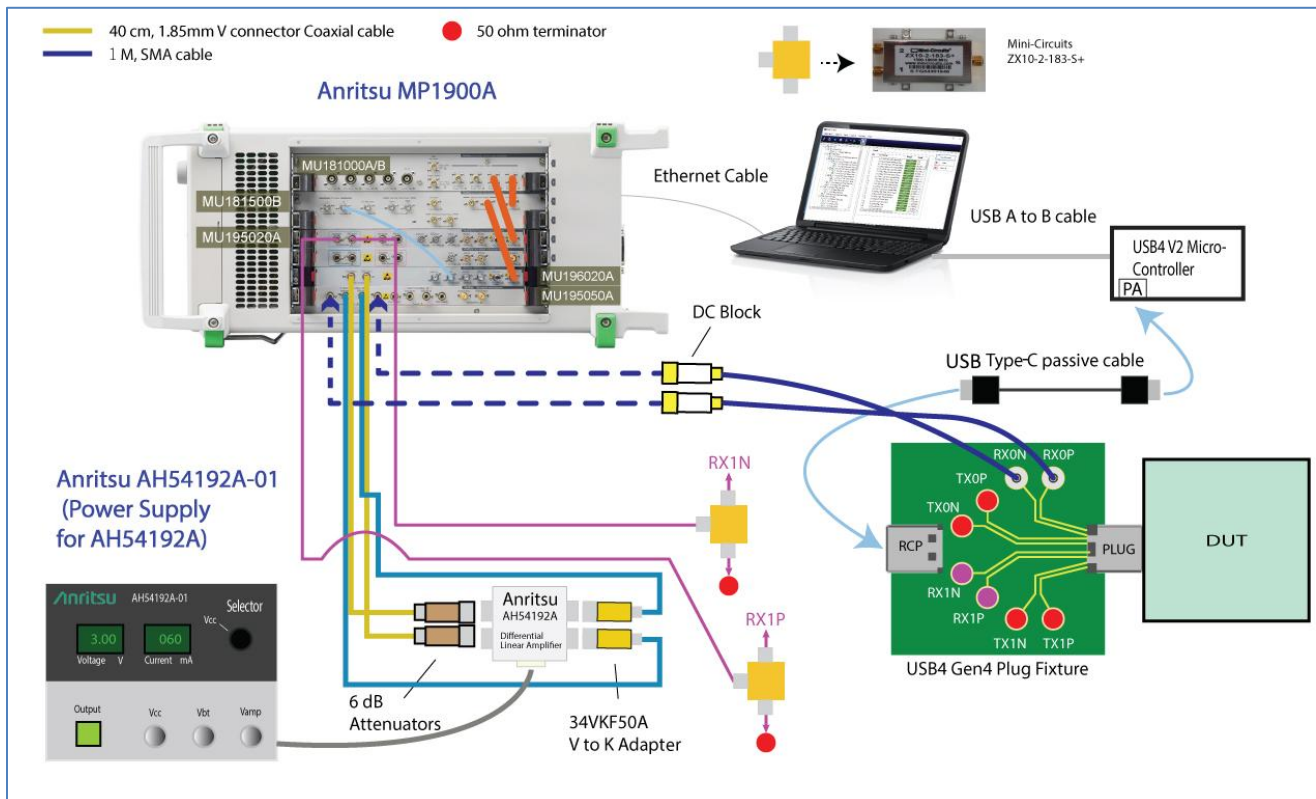


FIGURE 32. Rx TER TEST SETUP FOR CASE 1 USING PAM4 STANDARD BERT MODE WITH MU195050A

Connection Steps:

1. Continuing from the “Standard BERT for PAM4 with MU195050A Mode” setup in Section 6.1.1.2, disconnect and remove the oscilloscope from the setup.
2. Attach the USB4 Gen 4 plug fixture to the DUT.
3. Using a USB Type-C passive cable, connect the USB4 Gen 4 plug fixture to the USB4 V2 microcontroller.
4. Connect the USB4 V2 microcontroller to power supply and to the control PC using a USB Type-A to Type-B cable.
5. Connect the control PC to the MP1900A BERT using an Ethernet cable.
6. Connect the MU195050A data outputs through DC blocks to the RXON and RXOP pins of the USB4 Gen 4 plug fixture.
7. Connect the unterminated ports of the V-connector power splitters (that are connected to the MU195020A Data Outputs) to the RX1N and RX1P pins of the USB4 Gen 4 plug fixture.
8. Run the USB4 V2 microcontroller to control the DUT using ETT.

6.1.2.2 Standard BERT for PAM4 with MU196050A Mode

Figure 33 shows the USB4 V2 host/device DUT test setup diagram for Case 1 using the USB4 V2 microcontroller and the MP1900A BERT for the Standard BERT for PAM4 with MU196050A mode.

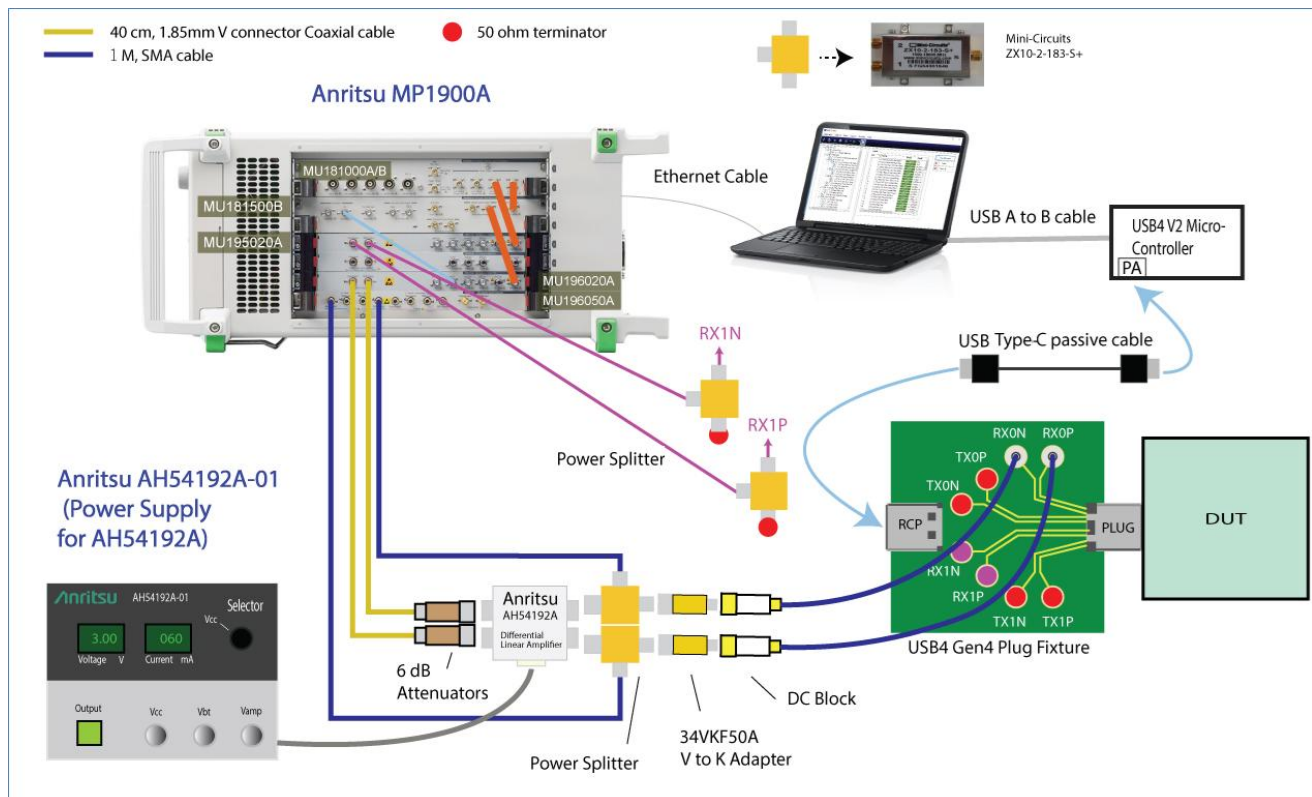


FIGURE 33. Rx TER TEST SETUP FOR CASE 1 USING PAM4 STANDARD BERT MODE WITH MU196050A

Connection Steps:

1. Continuing from the “Standard BERT for PAM4 with MU196050A Mode” setup in Section 6.1.1.1, disconnect and remove the oscilloscope from the setup.
2. Attach the USB4 Gen 4 plug fixture to the DUT.
3. Using a USB Type-C passive cable, connect the USB4 Gen 4 plug fixture to the USB4 V2 microcontroller.
4. Connect the USB4 V2 microcontroller to power supply and to the control PC using a USB Type-A to Type-B cable.
5. Connect the control PC to the MP1900A BERT using an Ethernet cable.
6. Connect the unterminated ports of the V-conductor power splitters (that are connected to the MU195020A Data Outputs) to the RX1N and RX1P pins of the USB4 Gen 4 plug fixture.
7. Connect the DC blocks (from the MU196020A Data Outputs) to the RX0N and RX0P pins of the USB4 Gen 4 plug fixture.
8. Run the USB4 V2 microcontroller to control the DUT using ETT.

6.1.2.3 Standard BERT for SI Mode

Figure 34 shows the USB4 V2 host/device DUT test setup diagram for Case 1 using the USB4 V2 microcontroller and the MP1900A BERT for the Standard BERT for SI mode.

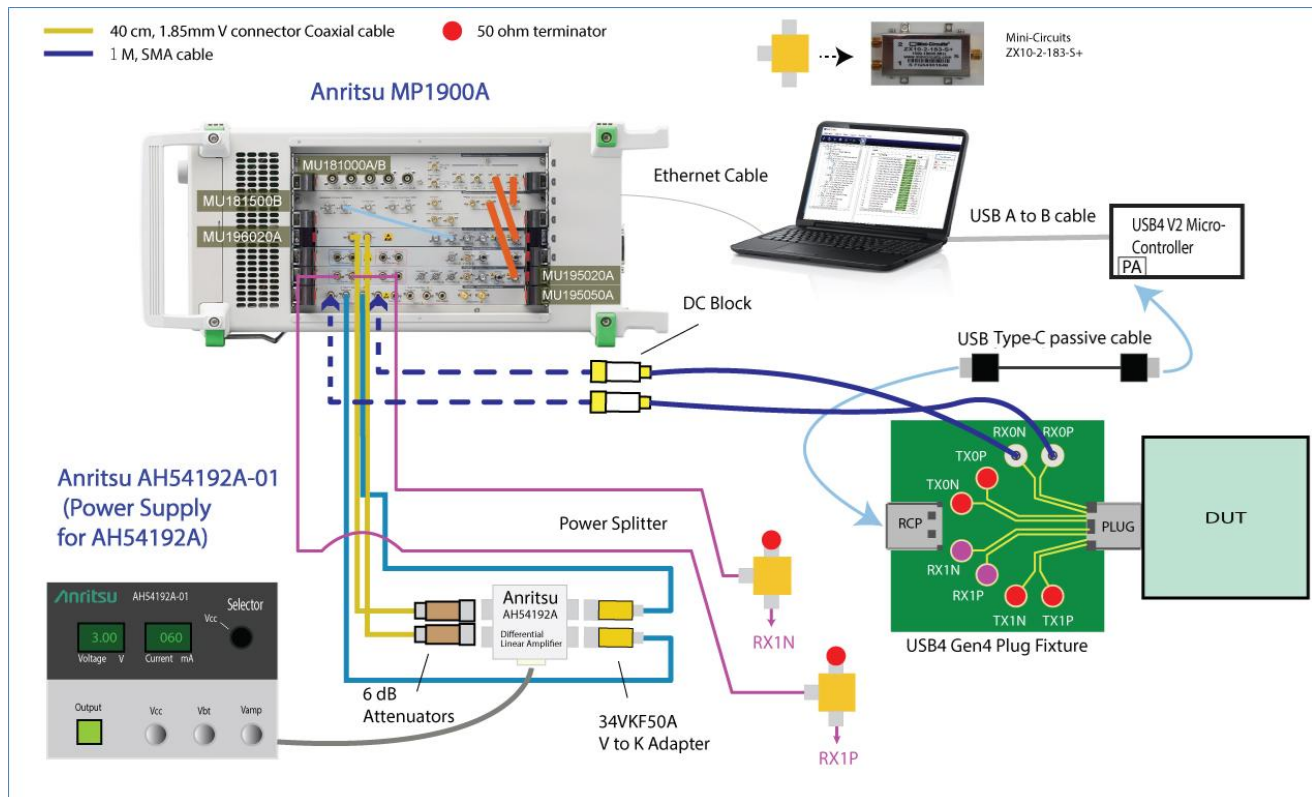


FIGURE 34. Rx TER TEST SETUP FOR CASE 1 USING SI STANDARD BERT MODE

Connection Steps:

1. Continuing from the “Standard BERT for SI Mode” setup in Section 6.1.1.3, disconnect and remove the oscilloscope from the setup.
2. Attach the USB4 Gen 4 plug fixture to the DUT.
3. Using a USB Type-C passive cable, connect the USB4 Gen 4 plug fixture to the USB4 V2 microcontroller.
4. Connect the USB4 V2 microcontroller to power supply and to the control PC using a USB Type-A to Type-B cable.
5. Connect the control PC to the MP1900A BERT using an Ethernet cable.
6. Connect the DC blocks (from the MU195050A Data Outputs) to the RX0N and RX0P pins of the USB4 Gen 4 plug fixture.
7. Connect the unterminated ports of the V-connector power splitters (that are connected to the MU195020A Data Outputs) to the RX1N and RX1P pins of the USB4 Gen 4 plug fixture.
8. Run the USB4 V2 microcontroller to control the DUT using ETT.

6.1.3 TER Test Setup for Case 2

6.1.3.1 Standard BERT for PAM4 with MU195050A Mode

Figure 35 shows the USB4 V2 host/device DUT test setup diagram for Case 2 using the USB4 V2 microcontroller and the MP1900A BERT for the Standard BERT for PAM4 with MU195050A mode. The USB Type-C cable is disconnected from the USB4 V2 microcontroller and connected to the host/device DUT's USB Type-C receptacle connector.

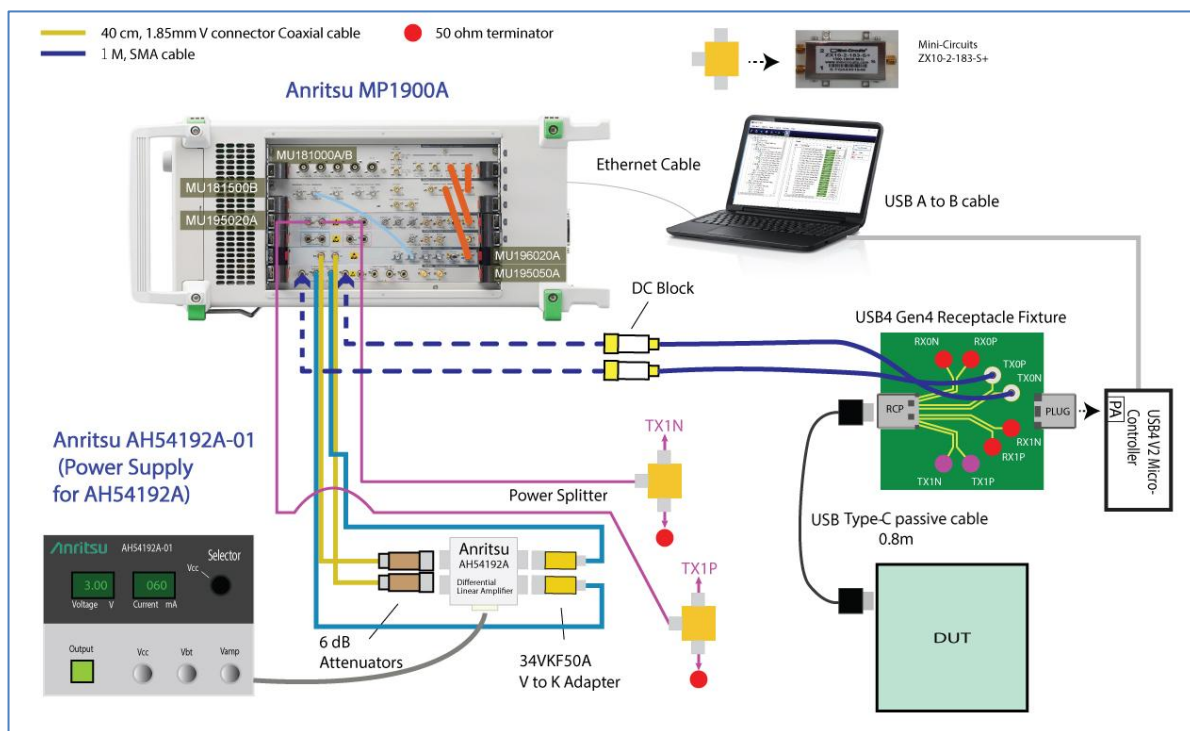


FIGURE 35. RX TER TEST SETUP FOR CASE 2 USING PAM4 STANDARD BERT MODE WITH MU195050A

Connection Steps:

1. Continuing from the “Standard BERT for PAM4 with MU195050A Mode” setup in Section 6.1.1.2, disconnect and remove the oscilloscope from the setup.
2. Attach the USB4 Gen 4 receptacle fixture to the USB4 V2 microcontroller.
3. Using a USB Type-C passive cable, connect the USB4 Gen 4 receptacle fixture to the DUT.
4. Connect the USB4 V2 microcontroller to power supply and to the control PC using a USB Type-A to Type-B cable.
5. Connect the control PC to the MP1900A BERT using an Ethernet cable.
6. Connect the MU195050A data outputs through DC blocks to the TXON and TXOP pins of the USB4 Gen 4 receptacle fixture.
7. Connect the unterminated ports of the V-connector power splitters (that are connected to the MU195020A Data Outputs) to the TX1N and TX1P pins of the USB4 Gen 4 receptacle fixture.
8. Run the USB4 V2 microcontroller to control the DUT using ETT.

6.1.3.2 Standard BERT for PAM4 with MU196050A Mode

Figure 36 shows the USB4 V2 host/device DUT test setup diagram for Case 2 using the USB4 V2 microcontroller and the MP1900A BERT for the Standard BERT for PAM4 with MU196050A mode.

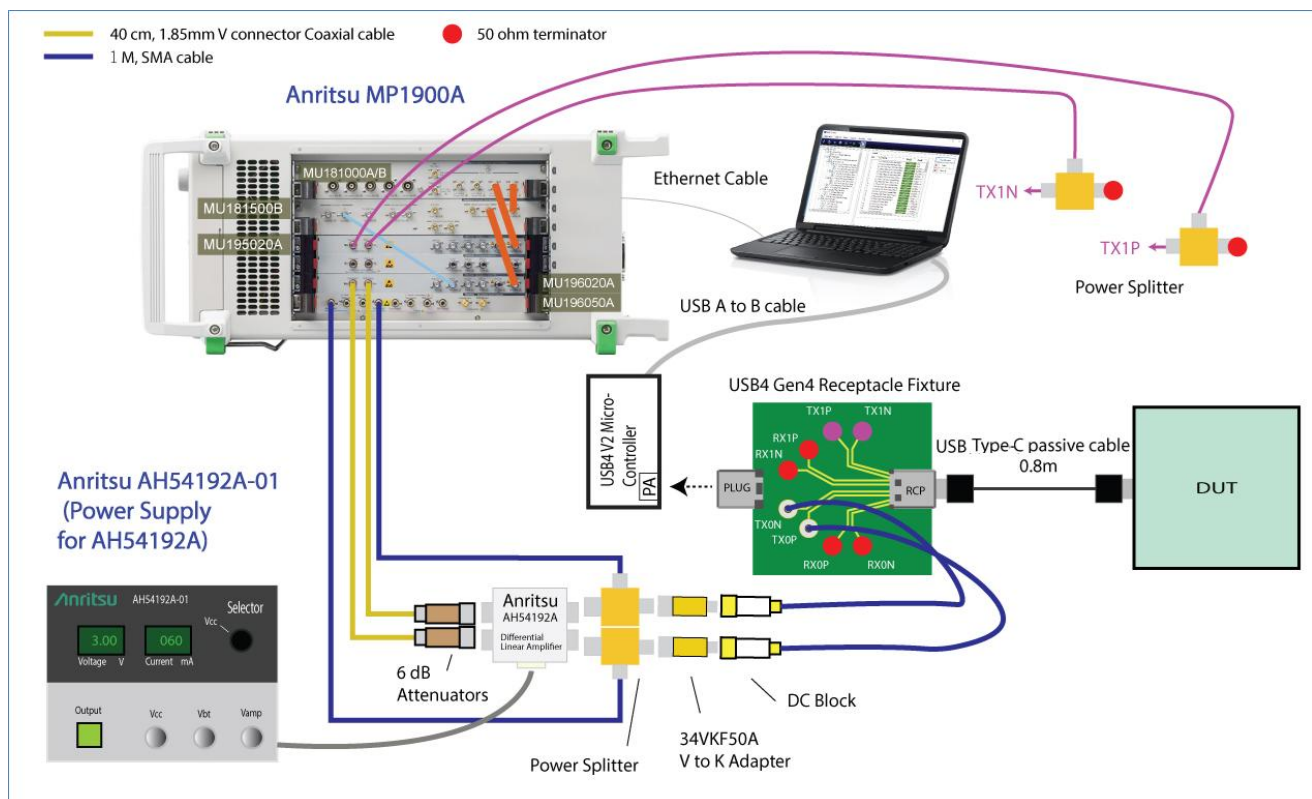


FIGURE 36. RX TER TEST SETUP FOR CASE 2 USING PAM4 STANDARD BERT MODE WITH MU196050A

Connection Steps:

1. Continuing from the “Standard BERT for PAM4 with MU196050A Mode” setup in Section 6.1.1.1, disconnect and remove the oscilloscope from the setup.
2. Attach the USB4 Gen 4 receptacle fixture to the USB4 V2 microcontroller.
3. Using a USB Type-C passive cable, connect the USB4 Gen 4 receptacle fixture to the DUT.
4. Connect the USB4 V2 microcontroller to power supply and to the control PC using a USB Type-A to Type-B cable.
5. Connect the control PC to the MP1900A BERT using an Ethernet cable.
6. Connect the unterminated ports of the V-conductor power splitters (that are connected to the MU195020A Data Outputs) to the TX1N and TX1P pins of the USB4 Gen 4 receptacle fixture.
7. Connect the DC blocks (from the MU196020A Data Outputs) to the TX0N and TX0P pins of the USB4 Gen 4 receptacle fixture.
8. Run the USB4 V2 microcontroller to control the DUT using ETT.

6.1.3.3 Standard BERT for SI Mode

Figure 37 shows the USB4 V2 host/device DUT test setup diagram for Case 2 using the USB4 V2 microcontroller and the MP1900A BERT for the Standard BERT for SI mode.

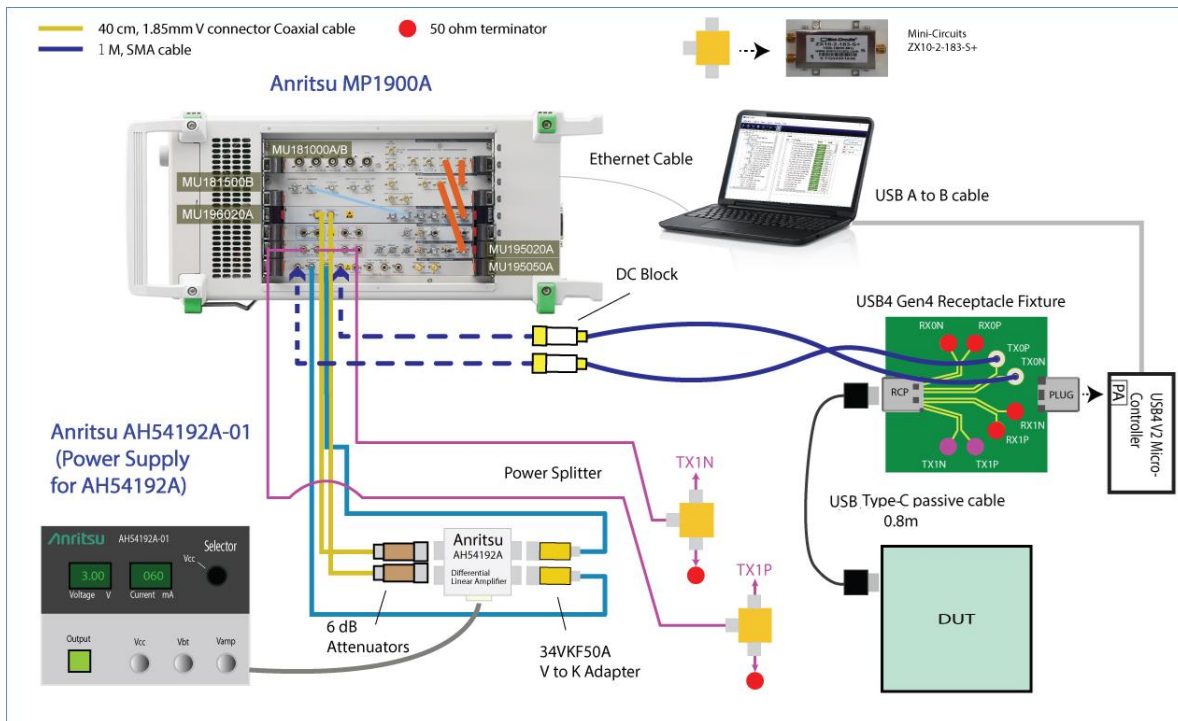


FIGURE 37. RX TER TEST SETUP FOR CASE 2 USING SI STANDARD BERT MODE

Connection Steps:

1. Continuing from the “Standard BERT for SI Mode” setup in Section 6.1.1.3, disconnect and remove the oscilloscope from the setup.
2. Attach the USB4 Gen 4 receptacle fixture to the USB4 V2 microcontroller.
3. Using a USB Type-C passive cable, connect the USB4 Gen 4 receptacle fixture to the DUT.

4. Connect the USB4 V2 microcontroller to power supply and to the control PC using a USB Type-A to Type-B cable.
5. Connect the control PC to the MP1900A BERT using an Ethernet cable.
6. Connect the DC blocks (from the MU195050A Data Outputs) to the TX0N and TX0P pins of the USB4 Gen 4 receptacle fixture.
7. Connect the unterminated ports of the V-conductor power splitters (that are connected to the MU195020A Data Outputs) to the TX1N and TX1P pins of the USB4 Gen 4 receptacle fixture.
8. Run the USB4 V2 microcontroller to control the DUT using ETT.

6.2 Receiver LFPS Test Setups

Note: To access and run the LFPS tests, the user is required to purchase the “GRL-USB4V2-LFPS-AN” license from GRL Platform Solutions @ support@grlps.com.

6.2.1 Standard BERT for PAM4 with MU195050A Mode

Figure 38 shows the receiver LFPS test setup diagram using the USB4 V2 microcontroller, MP1900A BERT and oscilloscope for the Standard BERT for PAM4 with MU195050A mode. The calibrated stressed signal is attached to the USB4 Gen4 plug fixture, and crosstalk is added to the fixture from the MP1900A MU195020A SI Pulse Pattern Generator which generates aggressor signals. The microcontroller is used to directly control the DUT by executing the ETT.

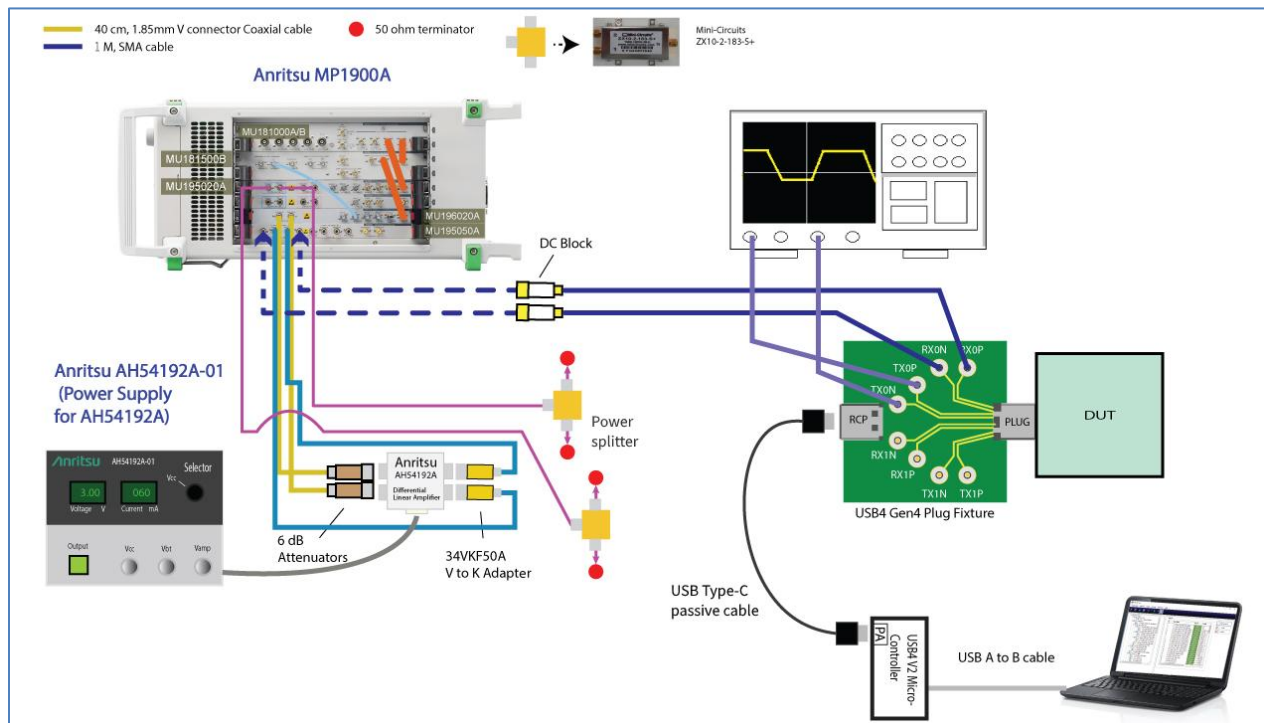


FIGURE 38. Rx LFPS TEST SETUP USING PAM4 STANDARD BERT MODE WITH MU195050A

Connection Steps:

1. Continuing from the “Standard BERT for PAM4 with MU195050A Mode” setup in Section 6.1.1.2, disconnect all connections to the oscilloscope.

2. Remove the connection between the MU181500B IQ Output I and the oscilloscope AUX In/AUX Trig.
3. Attach the USB4 Gen 4 plug fixture to the DUT.
4. Using a USB Type-C passive cable, connect the USB4 Gen 4 plug fixture to the USB4 V2 microcontroller.
5. Connect the USB4 V2 microcontroller to power supply and to the control PC using a USB Type-A to Type-B cable.
6. Connect the MU195050A data outputs through DC blocks to the RXON and RXOP pins of the USB4 Gen 4 plug fixture.
7. Terminate the other end of the port of both V-connector power splitters.
8. Connect the TXON and TXOP pins of the USB4 Gen 4 plug fixture to the oscilloscope channels 1 and 3 respectively.
9. Run the USB4 V2 microcontroller to control the DUT using ETT.

6.2.2 Standard BERT for PAM4 with MU196050A Mode

Figure 43 shows the receiver LFPS test setup diagram using the USB4 V2 microcontroller, MP1900A BERT and oscilloscope for the Standard BERT for PAM4 with MU196050A mode.

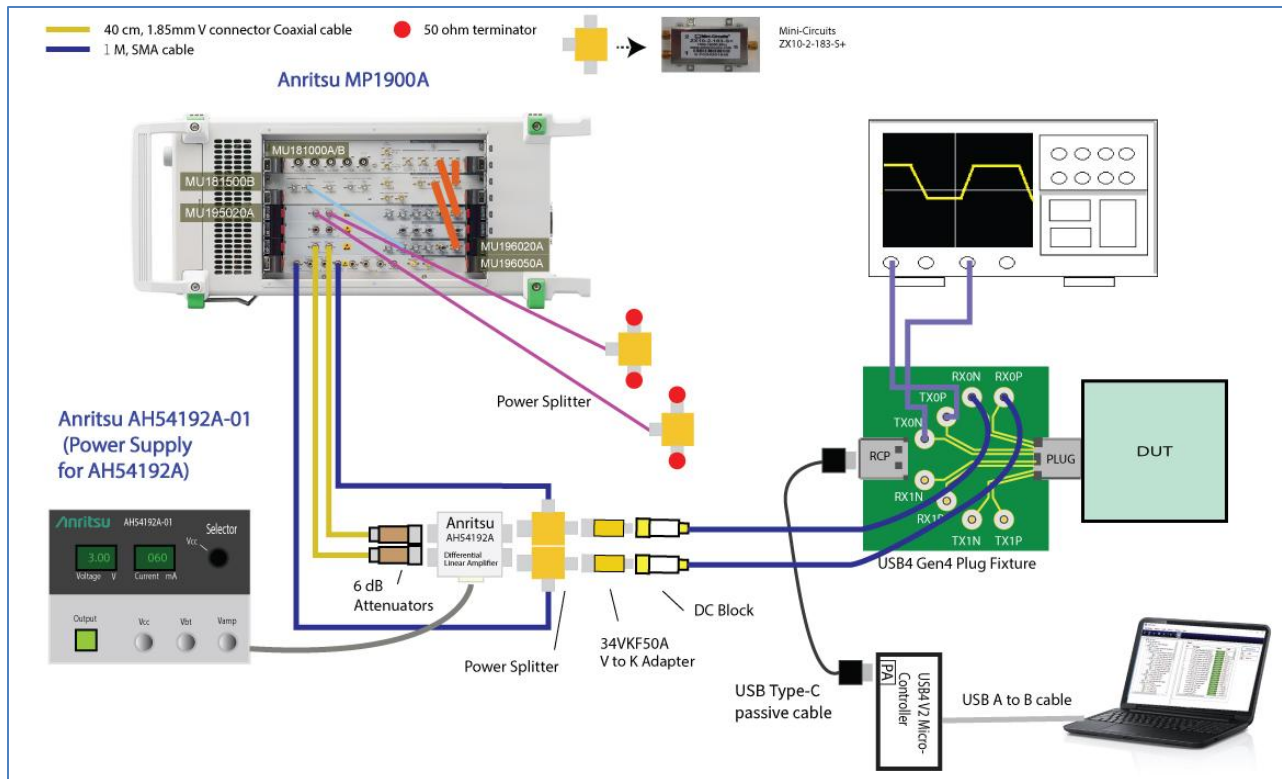


FIGURE 39. RX LFPS TEST SETUP USING PAM4 STANDARD BERT MODE WITH MU196050A

Connection Steps:

1. Continuing from the “Standard BERT for PAM4 with MU196050A Mode” setup in Section 6.1.1.1, disconnect all connections to the oscilloscope.
2. Remove the connection between the MU181500B IQ Output I and the oscilloscope AUX In/AUX Trig.
3. Attach the USB4 Gen 4 plug fixture to the DUT.

4. Using a USB Type-C passive cable, connect the USB4 Gen 4 plug fixture to the USB4 V2 microcontroller.
5. Connect the USB4 V2 microcontroller to power supply and to the control PC using a USB Type-A to Type-B cable.
6. Terminate the other end of the port of both V-conductor power splitters.
7. Connect the DC blocks (from the MU196020A Data Outputs) to the RX0N and RX0P pins of the USB4 Gen 4 plug fixture.
8. Connect the TX0P and TX0N pins of the USB4 Gen 4 plug fixture to the oscilloscope channels 1 and 3 respectively.
9. Run the USB4 V2 microcontroller to control the DUT using ETT.

6.2.3 Standard BERT for SI Mode

Figure 40 shows the receiver LFPS test setup diagram using the USB4 V2 microcontroller, MP1900A BERT and oscilloscope for the Standard BERT for SI mode.

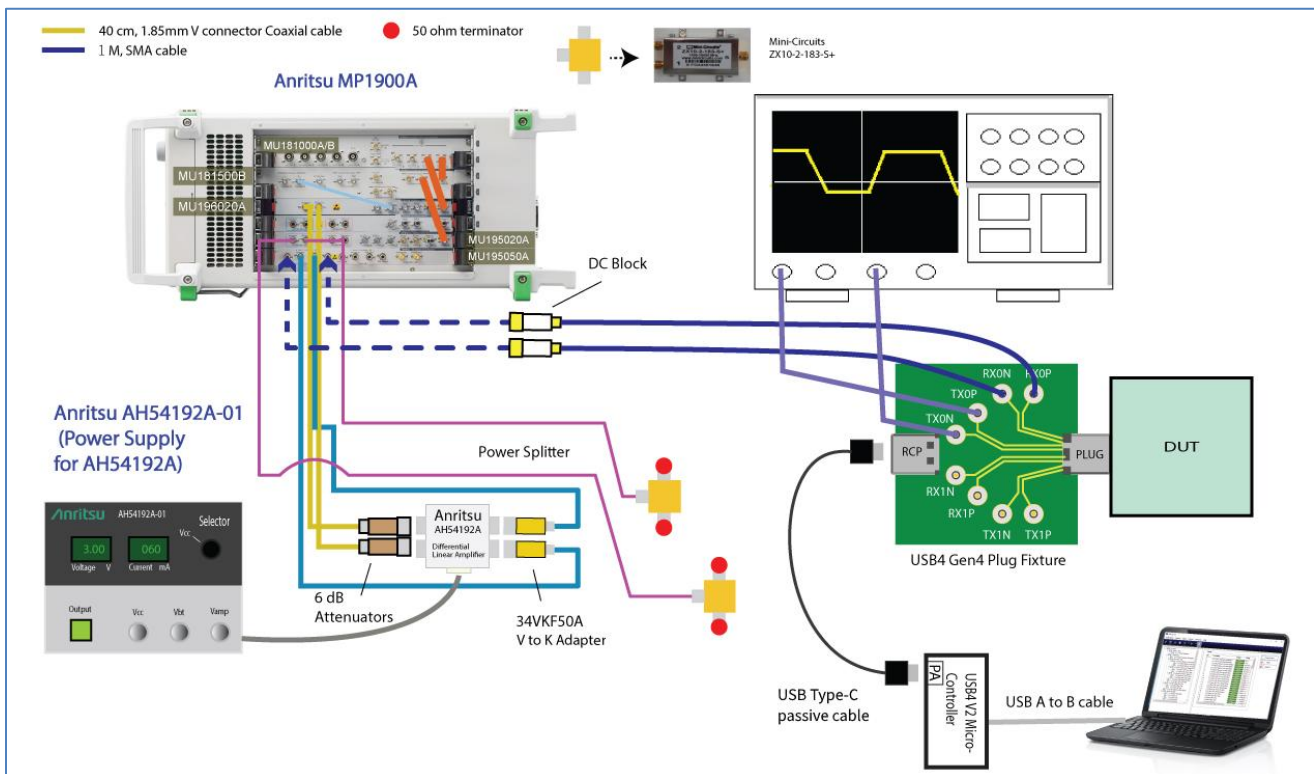


FIGURE 40. RX LFPS TEST SETUP USING SI STANDARD BERT MODE

Connection Steps:

1. Continuing from the “Standard BERT for SI Mode” setup in Section 6.1.1.3, disconnect all connections to the oscilloscope.
2. Remove the connection between the MU181500B IQ Output I and the oscilloscope AUX In/AUX Trig.
3. Attach the USB4 Gen 4 plug fixture to the DUT.
4. Using a USB Type-C passive cable, connect the USB4 Gen 4 plug fixture to the USB4 V2 microcontroller.

5. Connect the USB4 V2 microcontroller to power supply and to the control PC using a USB Type-A to Type-B cable.
6. Terminate the other end of the port of both V-connector power splitters.
7. Connect the DC blocks (from the MU195050A Data Outputs) to the RX0N and RX0P pins of the USB4 Gen 4 plug fixture.
8. Connect the TX0P and TX0N pins of the USB4 Gen 4 plug fixture to the oscilloscope channels 1 and 3 respectively.
9. Run the USB4 V2 microcontroller to control the DUT using ETT.

6.3 Select DUT Rx Compliance, Aggressor Signal Monitoring, Frequency Variation, Margin Search, LFPS and LRD Tests

On the test selection page, un-select all Calibration selections as they were completed in the previous section. Scroll down to access the Receiver compliance, Aggressor signal check, Frequency Variation, Margin Search test (optional), Rx LFPS and LRD test selections. Select the check boxes of the respective tests to be run.

Note: The LFPS and LRD test selections are only available with purchase of the “GRL-USB4V2-LFPS-AN” and “GRL-USB4V2-LRD-AN” licenses from GRL Platform Solutions @ support@grlps.com respectively.

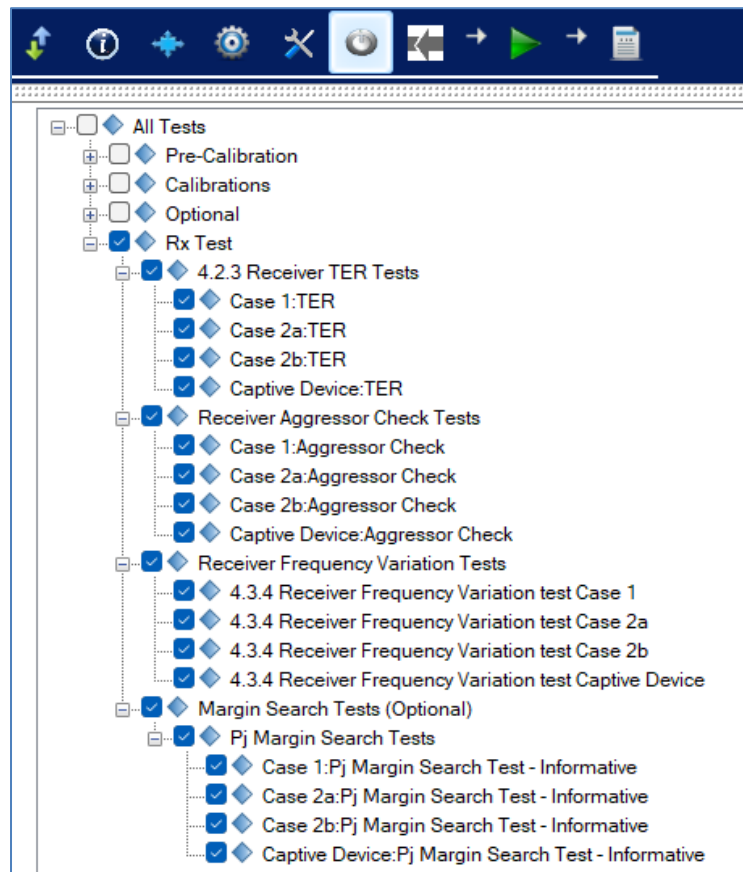


FIGURE 41. SELECT DUT RX COMPLIANCE, AGGRESSOR SIGNAL CHECK, FREQUENCY VARIATION AND MARGIN SEARCH TESTS TO BE RUN

6.4 Select Test Mode

Select  from the software menu to access the Setup Configuration page and select the **Test Mode** tab.

Select the checkbox to run tests in compliance mode for the DUT to meet the USB4 V2 Rx CTS compliance.

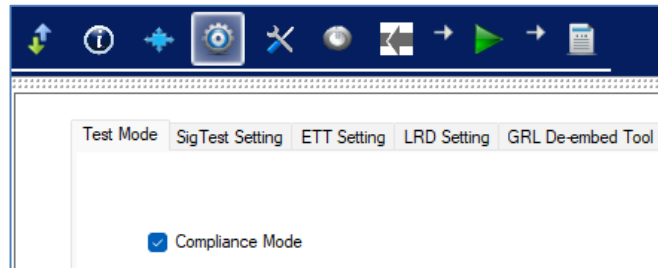


FIGURE 42. SELECT TEST MODE

6.5 Set Up USB4 ETT Environment

Select  from the software menu to access the Setup Configuration page.

Select the **ETT Setting** tab to call the ETT script from a remote host as described below:

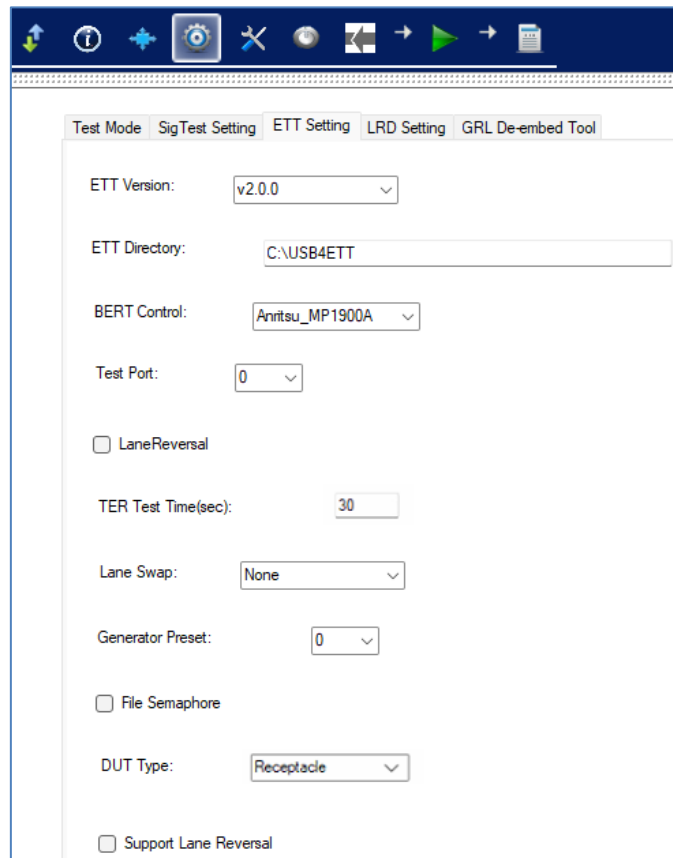


FIGURE 43. SETUP FOR ETT ENVIRONMENT

1. Select the **ETT Version** to be used.
2. Set the **ETT Directory** field to the path where the ETT script is installed in the host PC.
3. Select the **BERT Control** as “Anritsu_MP1900A” (using the Anritsu MP1900A BERT automation control).
4. Select the **Test Port** of the DUT to validate for ETT test port mapping.
5. Select the **Lane Reversal** checkbox to enable reverse insertion of the USB Type-C connector.
6. Set the **TER Test Time** in seconds to run the Receiver TER tests.
7. To perform lane switching for the DUT, select the router and/or re-timer setup in the **Lane Swap** field.
8. Configure the BERT to preset # as selected in the **Generator Preset** field.
9. Select the **File Semaphore** checkbox to enable the ETT “File Semaphore” function: Use File Semaphore for FFE Preset Request.
10. Select the **DUT Type** to map to the ETT DUT Type configuration.
11. Select the **Support Lane Reversal** checkbox if the DUT supports reverse insertion of the USB Type-C connector.

6.6 Set Up LRD Test Environment

Note: To access and run the LRD tests, the user is required to purchase the “GRL-USB4V2-LRD-AN” license from GRL Platform Solutions @ support@grlps.com.

Select  from the software menu to access the Setup Configuration page.

Select the **LRD Setting** tab as described below:

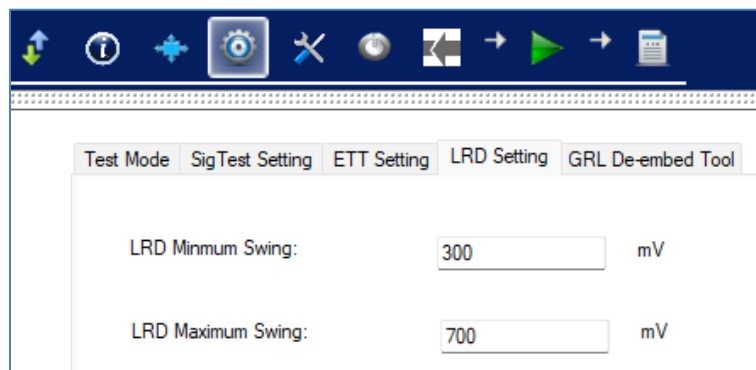


FIGURE 44. SETUP FOR LRD TEST ENVIRONMENT

Set the **LRD Minimum** and **Maximum Swing** values for the LRD swing calibration item “LRD PRTS7 Swing Calibration”.

6.7 Configure Margin Search Test Values

Select  from the menu to access the Margin Test page. The user can configure the PJ margin search test values, i.e. jitter initial value, step size, maximum error, test duration and maximum step to be applied in the Case 1 or Case 2a PJ margin search tests.

By default, the PJ margin search test values are those defined in the specification. To apply the default values, select the 'Use Default Value' checkbox to allow all existing values to be reset to default.

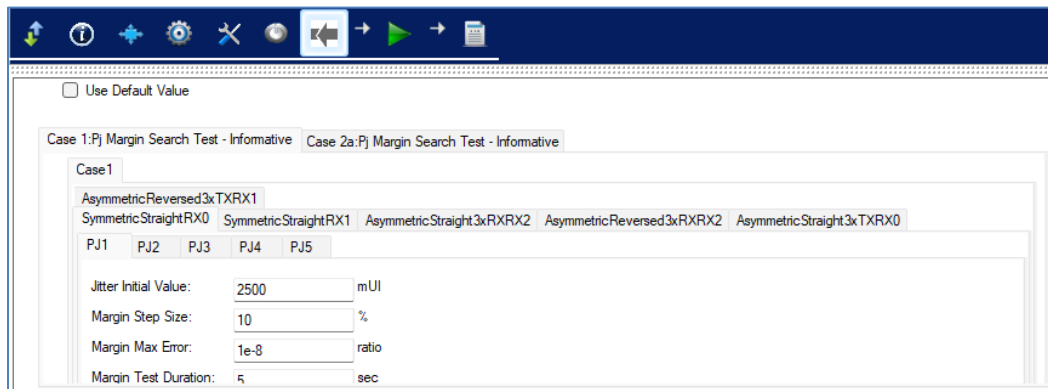


FIGURE 45. CONFIGURE PJ MARGIN SEARCH TEST VALUES

6.8 Configure Test Parameters

After selecting the desired Rx tests and setting up the test environment, select  from the software menu to access the Configurations page. Set the required parameters for the Rx tests as described below.

To return all parameters to their default values, select the 'Set Default' button.

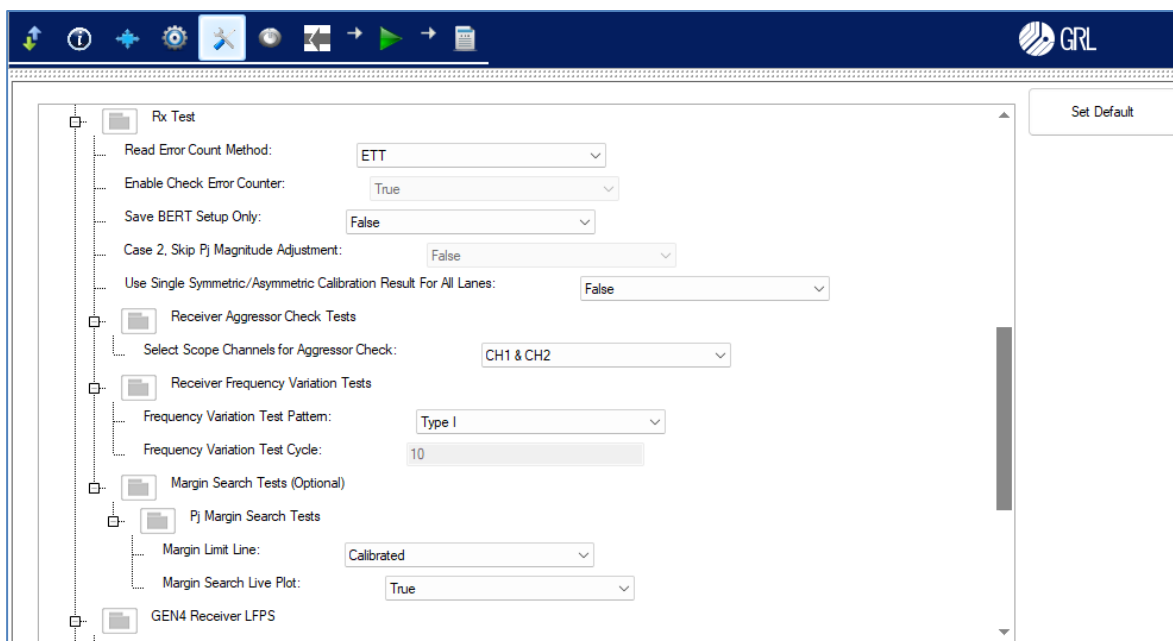
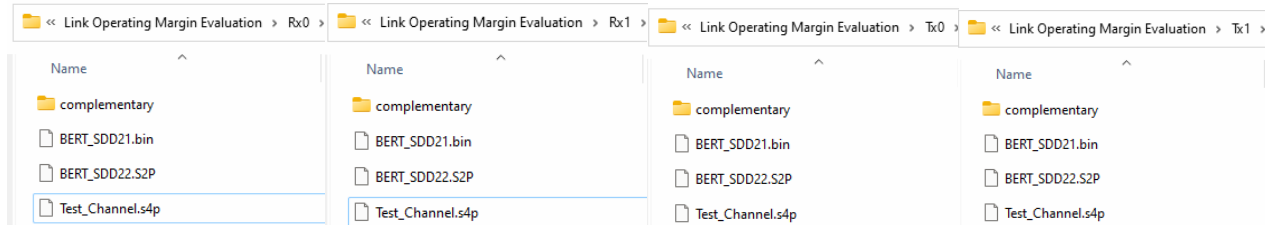


FIGURE 46. CONFIGURE TEST PARAMETERS

For the USB4 V2 Rx test, as any of the four high-speed signal pairs in the USB Type-C cable can be used as the Rx Lane, all four high-speed signal pairs need to be measured for Link Operating Margin Evaluation. Each of the four path directories should contain the corresponding lane files as follows:

- Test_Channel.s4p
- BERT_Sdd22.s2p
- BERT_Sdd21.[scope format]
- complementary (In the SigTest package downloaded from USB-IF)



Under the “Calibrations” parameters, set “**Use Single Tx and Rx Lane For Test**” to “True” to use the RX0 and TX0 lane Calibration results for RX1 and TX1 TER tests by flipping the USB Type-C cable at the DUT side.

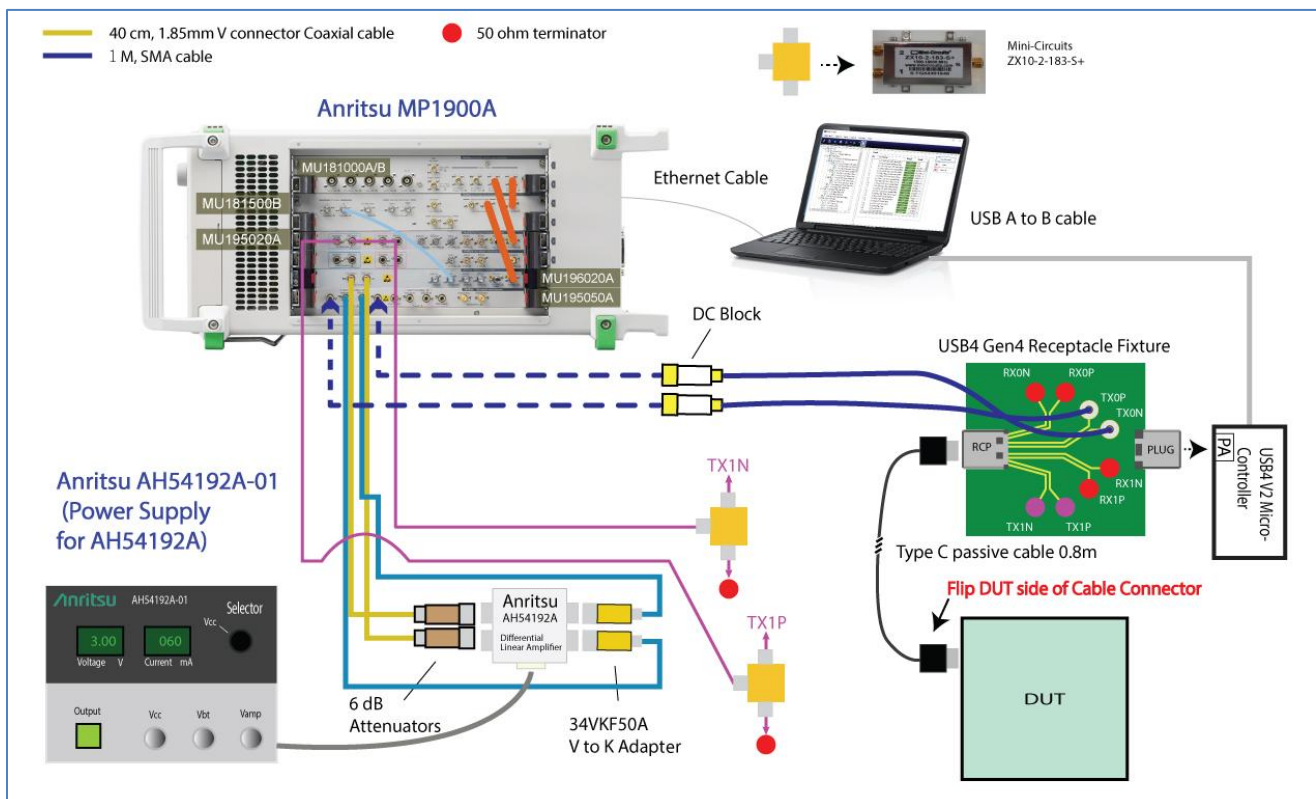


TABLE 6. RX TEST PARAMETERS DESCRIPTION

Parameter	Description
Read Error Count Method	Select the “ETT” method or a “Manual” method to read the error counter.
Enable Check Error Counter	“True” is usually the case. Set to “False” if you want to disable verification for the error count in the Rx test.
Save BERT Setup Only	“False” is usually the case. Set to “True” if you are sure that you only want to save the BERT test setup (calibrated results for Case 1 and Case 2) in the Rx test.
Case 2, Skip PJ Magnitude Adjustment	“False” is usually the case. Set to “True” if you want to keep the periodic jitter at its fixed spec value and calibrate the stressed eye using other impairments.
Use Single Symmetric/Asymmetric Calibration Result For All Lanes	“False” is usually the case. Set to “True” if you want to apply a single calibration result from the symmetric or asymmetric link for all test lanes, assuming that all lanes behave identically.
Receiver Aggressor Check Tests	
Select Scope Channels for Aggressor Check	Select either a single channel (CH1/CH2) as the positive aggressor path being monitored or both channels (CH1 & CH2 / CH2 & CH1) to allow simultaneous observation of both aggressor lanes on the oscilloscope.
Receiver Frequency Variation Tests	
Frequency Variation Test Pattern	Select the test pattern to be used in the Rx Frequency Variation tests.
Frequency Variation Test Cycle	Set the number of frequency variation test iterations (10 times as defined by the CTS).
PJ Margin Search Tests (Optional)	
Margin Limit Line	Select the option to use a limit based on calibrated or specification values for margin search tests.
Margin Search Live Plot	“True” is usually the case which enables a graphical margin plot that updates as the margin test is performed to indicate progress of the test results.
Gen4 Receiver LFPS	
Swing Setting of Setup 7 8	Select the low or high-power mode for the LFPS voltage swing at specific configurations.
Receiver LFPS Aggressor Signal Check	
Select Scope Channels for LFPS Aggressor Check	Select channel 1 (CH1) or channel 2 (CH2) on the oscilloscope to be used to verify that the required LFPS interference environment is correctly established and that the DUT maintains proper LFPS detection thresholds and timing against

	adjacent-lane LFPS activity.
LRD Test	
LRD Save BERT Setup Only	“False” is usually the case. Set to “True” if you are sure that you only want to save the BERT test setup for the LRD test.
LRD Waveform Acquisition	
ETT Link Type	Select the Symmetric Link or Asymmetric Link of either Asymmetric_3RX (transmits “1*TX/3*RX”) or Asymmetric_3TX (transmits “3*TX/1*RX”) to be applied for LRD waveform capture.

6.9 Run DUT Rx Tests

Select  from the software menu to access the Run Tests page. Select the Run Option as desired before clicking on the Run Tests button to start testing the DUT. (*This is similar to Section 5.8; refer for more details.*)

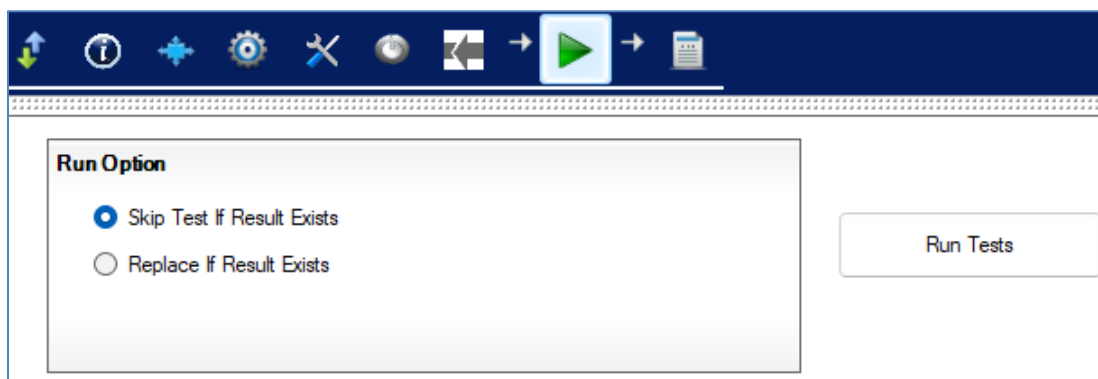


FIGURE 47. RUN TESTS

7 Test Results and Reports Using GRL-USB4-V2-RXA Software

The **Report**  page has all the results from all the test runs displayed. If some of the results are not desired, they can be individually deleted by using the **Delete** button. Also for a PDF report, select the **Generate report** button. To have the calibration data plotted in the report, make sure the **Plot Calibration Data** box is checked.

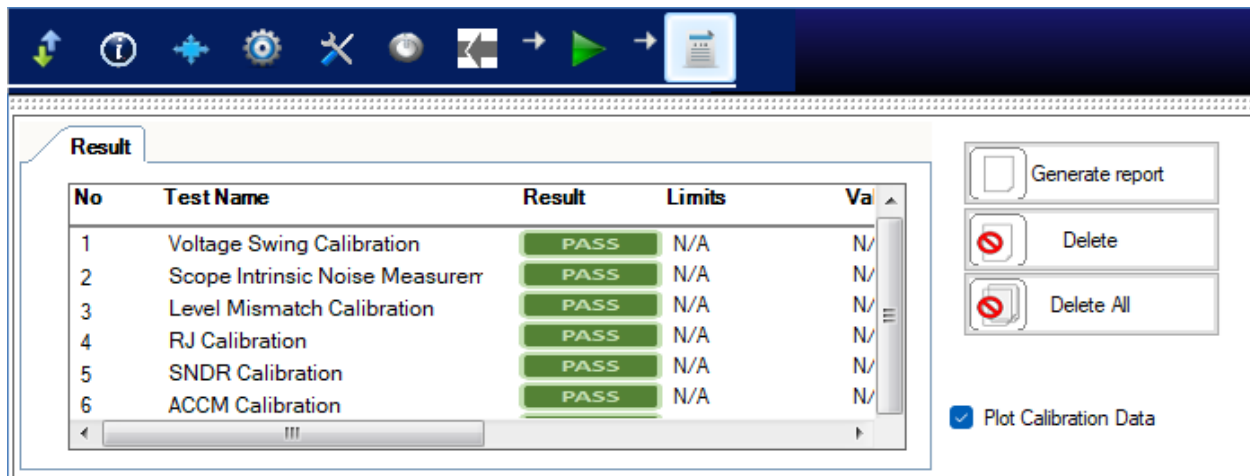


FIGURE 48. REPORT RESULTS PAGE

7.1.1 DUT Information

This portion is populated from the information in the DUT tab from the **Session Info** tab.

Anritsu USB4 V2 Rx Test Report	
DUT Information	
DUT Manufacturer	: GRL
DUT Model Number	: USB4_V2_RX001
DUT Serial Number	: 1000888ABC
DUT Comments	:
Test Information	
Test Lab	: Granite River Labs
Test Operator	: David
Test Date	: 16 Apr 2024
Software Version	
Software Revision	: 1.00.16

FIGURE 49. DUT INFORMATION

7.1.2 Results Summary Table

This portion is populated from the calibration and tests performed with their respective results. This gives an overall view of all the results and test conditions.

No	TestName	Limits	Value	Results	Test Point	Link Type	Test Lane	Pj Frequency
1	Voltage Swing Calibration	N/A	N/A	Pass	Case 1	N/A	N/A	N/A
2	Voltage Swing Calibration	N/A	N/A	Pass	Case 2 (For Case 2a+2b Calibration)	N/A	N/A	N/A
3	Level Mismatch Calibration	N/A	N/A	Pass	Case 1	N/A	N/A	N/A
4	Level Mismatch Calibration	N/A	N/A	Pass	Case 2 (For Case 2a+2b Calibration)	N/A	N/A	N/A
5	RJ Calibration	N/A	N/A	Pass	Case 1	N/A	N/A	N/A
6	RJ Calibration	N/A	N/A	Pass	Case 2 (For Case 2a+2b Calibration)	N/A	N/A	N/A
7	SNDR Calibration	N/A	N/A	Pass	Case 1	N/A	N/A	N/A
8	SNDR Calibration	N/A	N/A	Pass	Case 2 (For Case 2a+2b Calibration)	N/A	N/A	N/A
9	ACCM Calibration	N/A	N/A	Pass	Case 1	N/A	N/A	N/A
10	ACCM Calibration	N/A	N/A	Pass	Case 2 (For Case 2a+2b Calibration)	N/A	N/A	N/A
11	PJ Calibration	N/A	N/A	Pass	Case 1	N/A	N/A	1 MHz
12	PJ Calibration	N/A	N/A	Pass	Case 1	N/A	N/A	2 MHz
13	PJ Calibration	N/A	N/A	Pass	Case 1	N/A	N/A	10 MHz
14	PJ Calibration	N/A	N/A	Pass	Case 1	N/A	N/A	50 MHz
15	PJ Calibration	N/A	N/A	Pass	Case 1	N/A	N/A	100 MHz
16	PJ Calibration	N/A	N/A	Pass	Case 2 (For Case 2a+2b Calibration)	N/A	N/A	1 MHz
17	PJ Calibration	N/A	N/A	Pass	Case 2 (For Case 2a+2b Calibration)	N/A	N/A	2 MHz
18	PJ Calibration	N/A	N/A	Pass	Case 2 (For Case 2a+2b Calibration)	N/A	N/A	10 MHz

FIGURE 50. RESULTS SUMMARY TABLE EXAMPLE

7.1.3 Calibration & Test Result Details

This portion is populated with results from each of the calibration and test runs. Here the results are explained in depth with supporting data points and screenshots. If the Plot Calibration Data checkbox is selected, then the plots are also displayed.

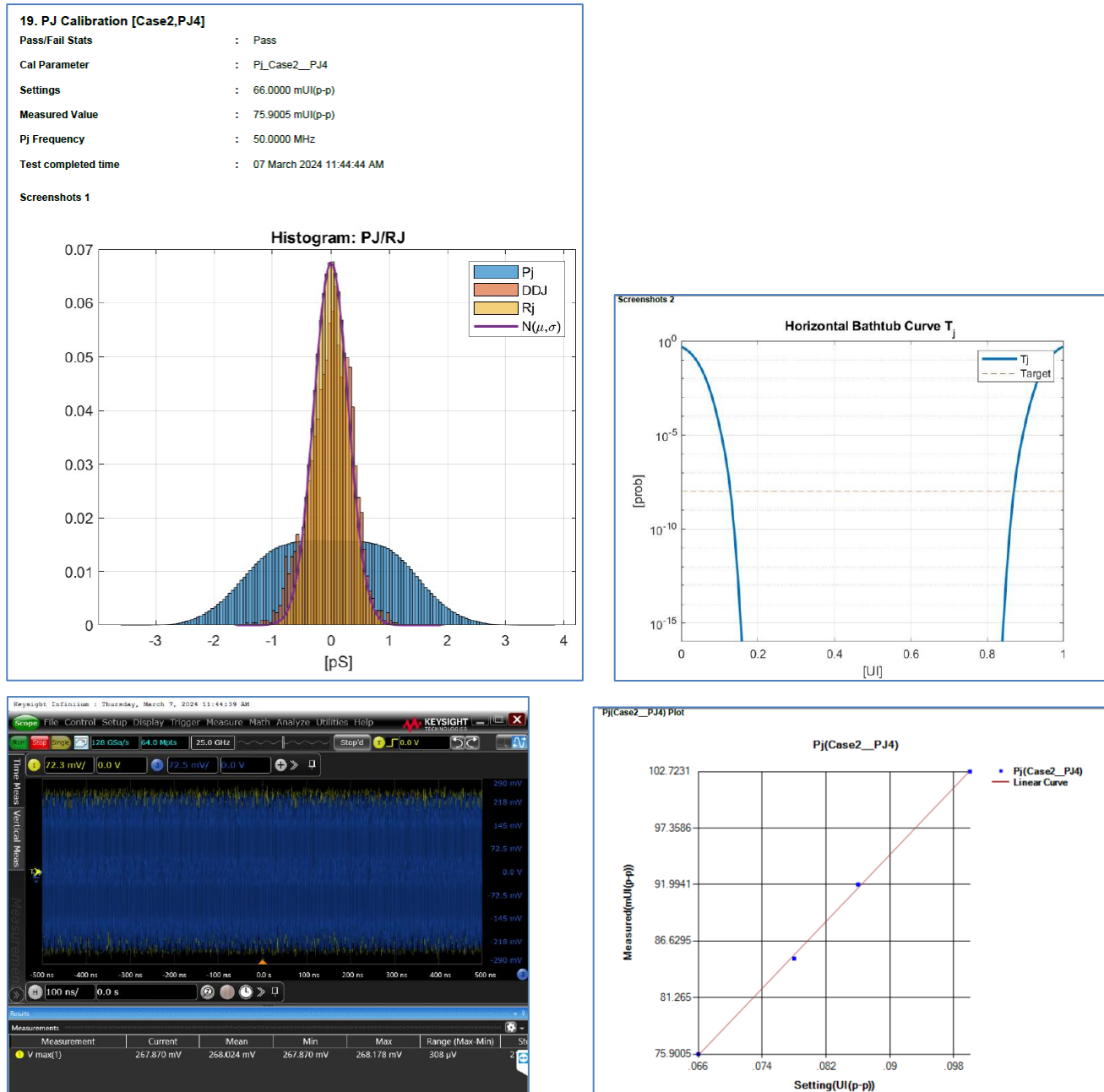


FIGURE 51. CALIBRATION/TEST RESULT DETAILS EXAMPLE

7.2 Delete Test Results

To individually delete any unwanted calibration/test results, select the corresponding result row and **Delete** button.

To entirely remove all existing calibration/test results, select the **Delete All** button.

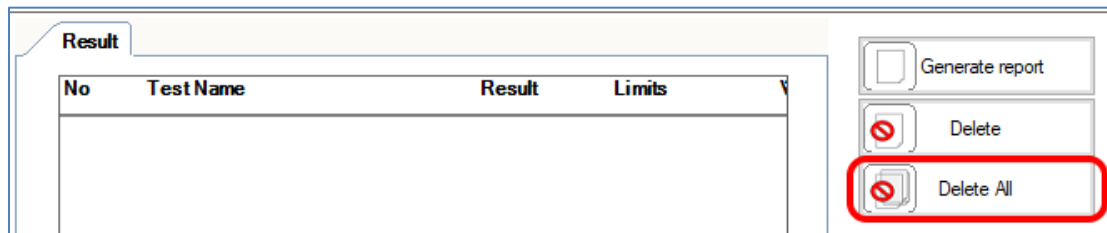


FIGURE 52. DELETE ALL RESULTS

8 Saving and Loading GRL-USB4-V2-RXA Test Sessions

The usage model for the GRL-USB4-V2-RXA software is that the test results are created and maintained as a 'Live Session' in the application. This allows the user to quit the application and return later to continue where the user left off.

Save and Load Sessions are used to save a test session that the user may want to recall later. The user can 'switch' between different sessions by saving and loading them when needed.

- To **save a test session**, with all of the test parameter information, test results, and any waveforms, select the Options drop-down menu and then select 'Save Session'.
- To **load a test session** back into the application, including the saved test parameter settings, select Options → 'Load Session'.
- To **create a new test session** and return the application back to the default configuration, select Options → 'New Session'.

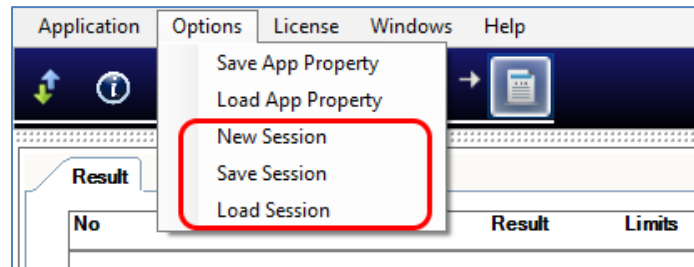


FIGURE 53. SAVE/LOAD/CREATE TEST SESSIONS

The test configuration and session results are saved in a file with the '.ses' extension, which is a compressed zip-style file, containing a variety of information.

9 Appendix A: Manual Calibration & Test Methodologies

Note the MP1900A BERT is used in the following calibration and test methodologies.

9.1 Initialize Setting of BERT and Scope for Receiver Stressed Eye Calibration for Case 1

Set up the physical equipment connections without the ISI channel, as per Figure 10.

9.1.1 Set up the MP1900A BERT as follows:

- i. Go to Menu Bar → File → Initialize.
- ii. Switch modulation type to “PAM3”. See Figure 54.
- iii. Go to Jitter tab and set Clock Source to “Unit1:Slot2:MU181000B”. See Figure 55.
- iv. Go to PPG → Misc2.
- v. Set Clock Source to “Unit1:Slot4:MU181500B”. See Figure 56.
- vi. Set Bit Rate to 25.6Gbit/s. See Figure 56.
- vii. Set Offset (ppm) to 0 ppm.
- viii. Set Output Clock Rate to “Halfrate”. See Figure 56.
- ix. Set Test Pattern on PPG to “PRTS” and Length to “3⁷-1” bits. See Figure 57.
- x. Turn on PPG Data Output.
- xi. Go to PPG → Emphasis tab and turn on “Manual Setting”. See Figure 58.
- xii. Turn on “SSC”, with settings of 32kHz with 3400ppm triangle down spread. (SSC will remain on for all of the following steps.) See Figure 59.
- xiii. Adjust Total Amplitude on the BERT. A differential amplitude just over the 1090mV voltage swing should show as an initial value.
- xiv. Set initial CM frequency to 400MHz and amplitude to 0 mVpp. Turn off CM output. See Figure 60.
- xv. Set initial DM frequency to 10GHz and amplitude to 0 mVpp. Turn off DM output. See Figure 60.
- xvi. Set SJ1 frequency to 100 MHz and amplitude to 0 U1pp. Turn off SJ1 output. See Figure 61.
- xvii. Set RJ amplitude to 0 U1pp and turn off RJ output. See Figure 62.
- xviii. Go to PPG → Output.
- xix. Turn on Glitch-free. See Figure 63.

[7] PAM4 PPG
PAM3 ▼
Q: OFF
Warming Up

Output

Emphasis

Pattern

Error Addition

Misc1

Misc2

Clock Setting

Clock Source Unit1:Slot4:MU181500B ▼

Bit Rate USB4 Gen4 ▼

25.600 004 GBaud

Offset 0 ppm

Output Clock Rate Halfrate ▼ Max: 64.200G

Reference Clock Internal ▼

FIGURE 54. MODULATION TYPE “PAM3” SETTING

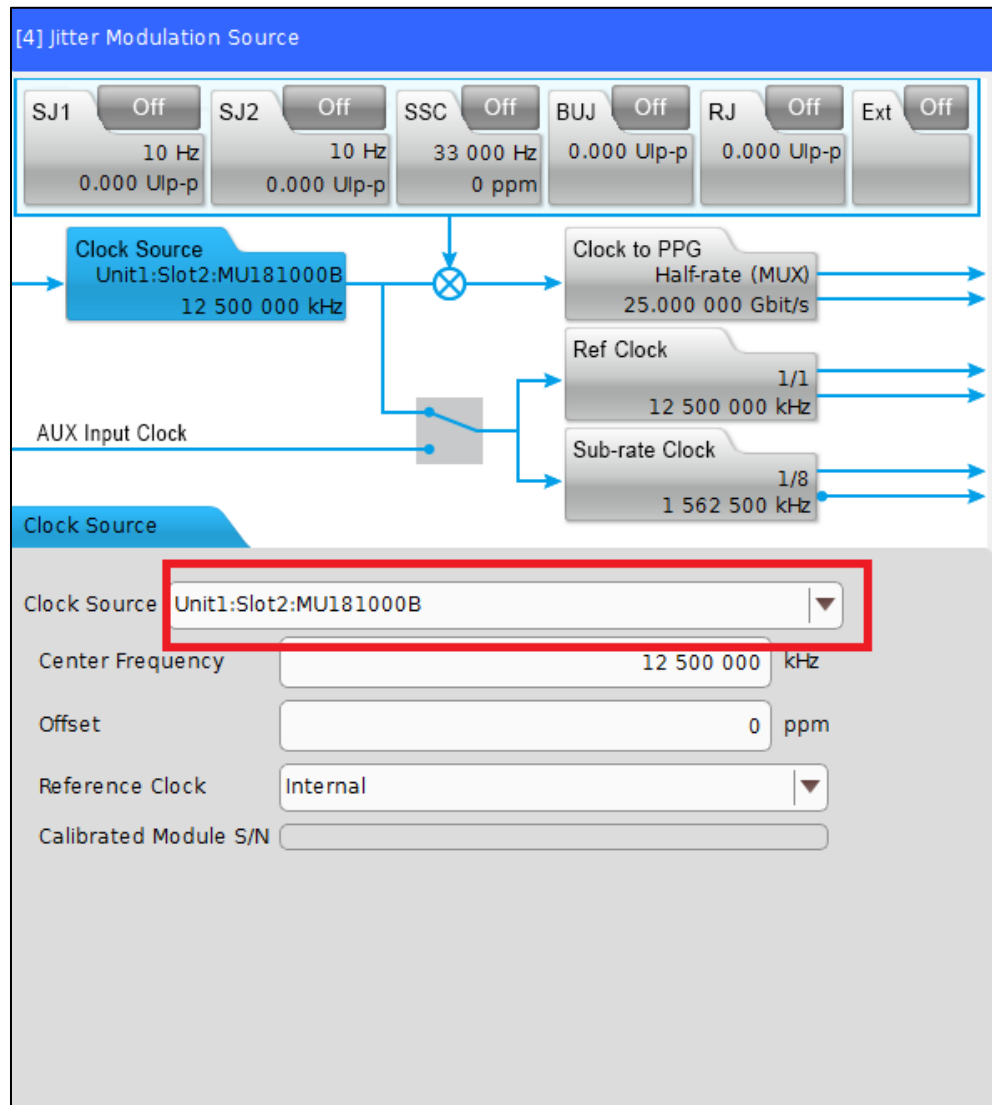


FIGURE 55. JITTER CLOCK SOURCE SETTING

[7] PAM4 PPG
PAM3
C: OFF
Warming Up

Output
 Emphasis
 Pattern
Error Addition
Misc1
Misc2

Clock Setting

Clock Source Unit1:Slot4:MU181500B

Bit Rate USB4 Gen4 25.600 004 GBaud

Offset 0 ppm

Output Clock Rate Halfrate Max: 64.200G

Reference Clock Internal

FIGURE 56. PPG MISC2 SETTINGS

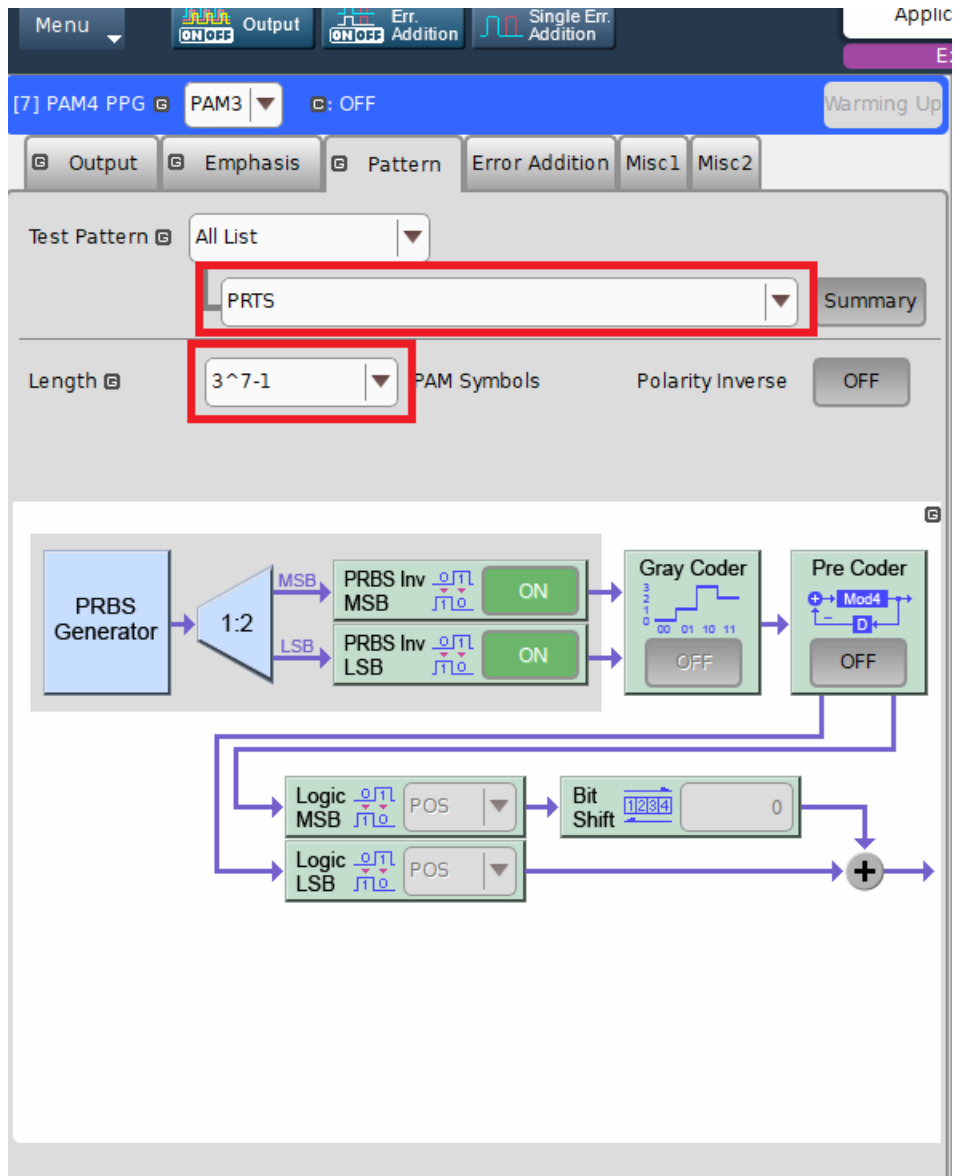


FIGURE 57. PATTERN SETTING

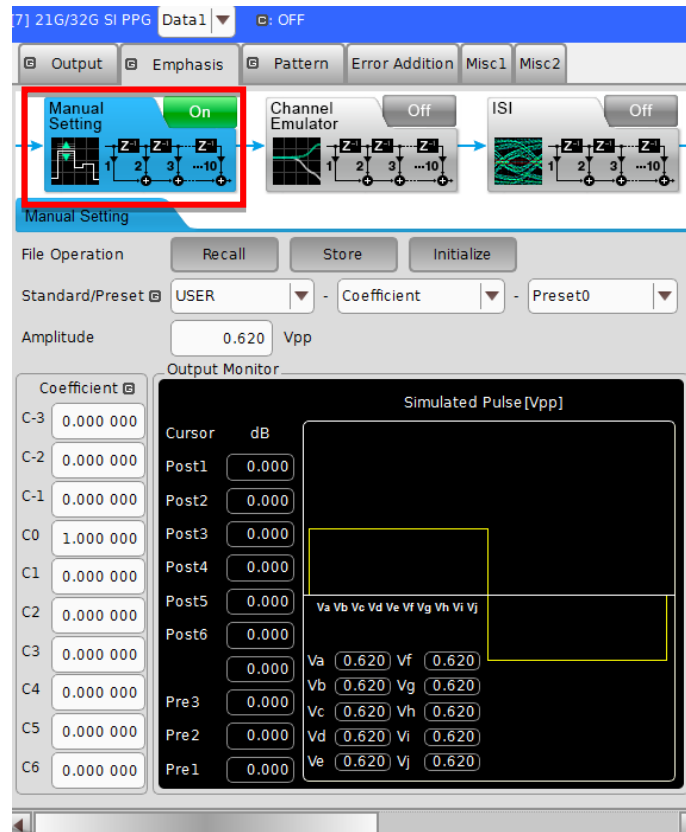


FIGURE 58. PPG EMPHASIS SETTING

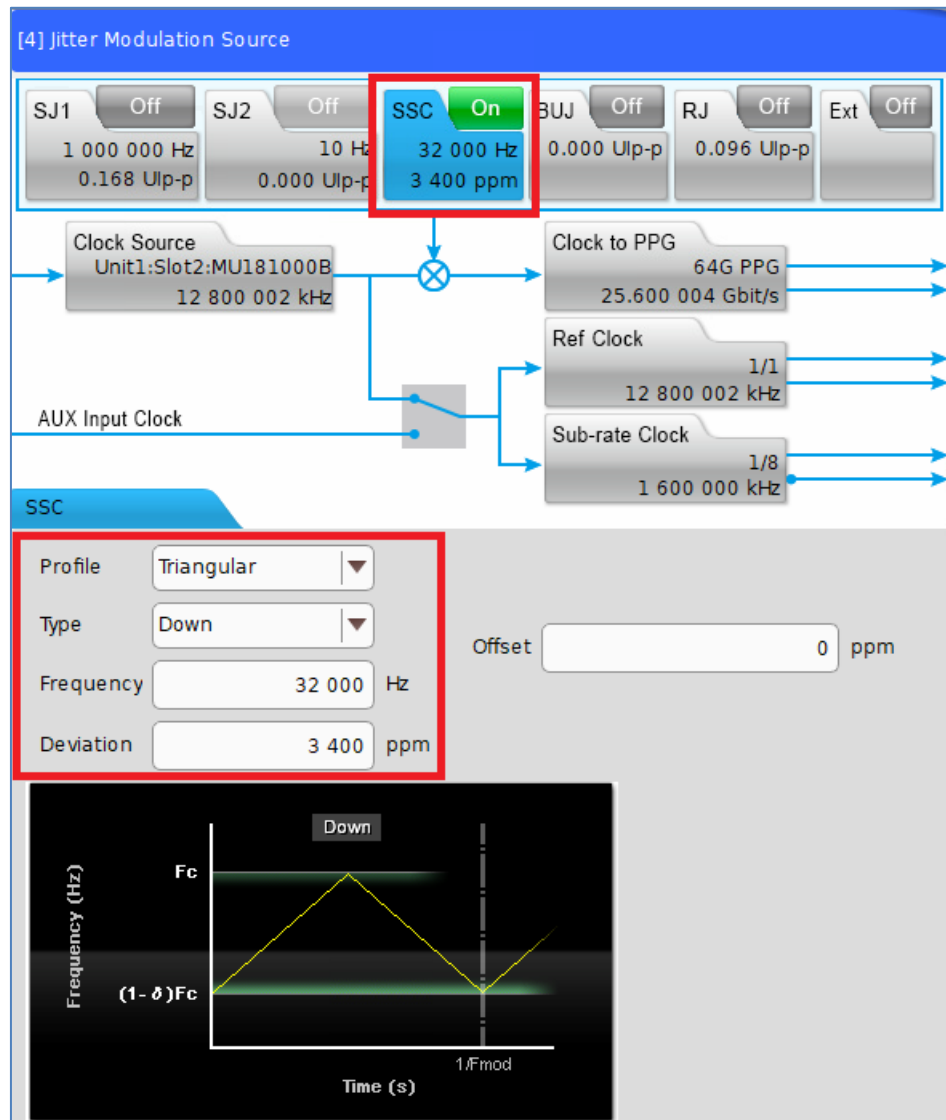


FIGURE 59. SSC SETUP FOR TEST CASE 1

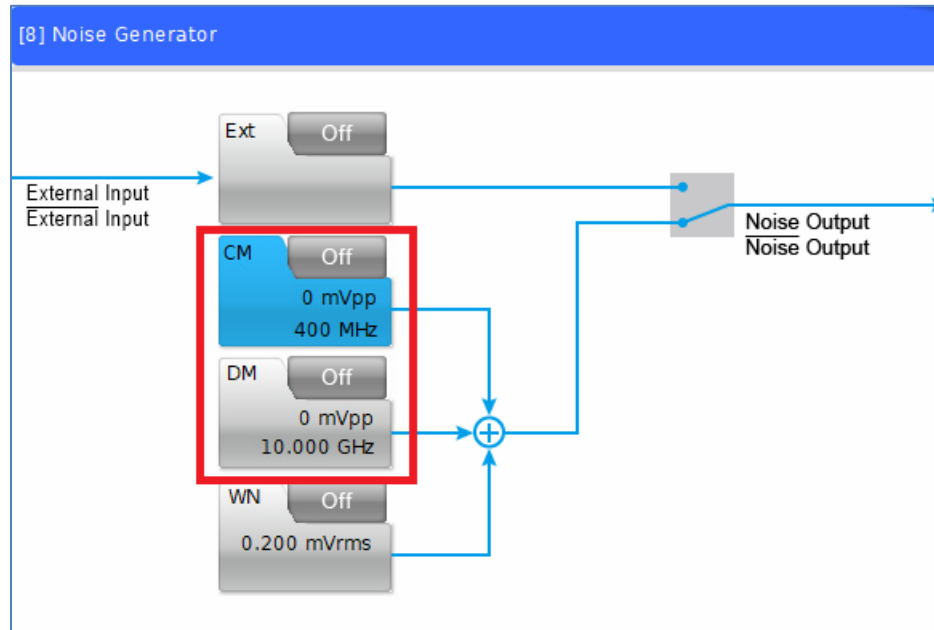


FIGURE 60. CM AND DM SETTING

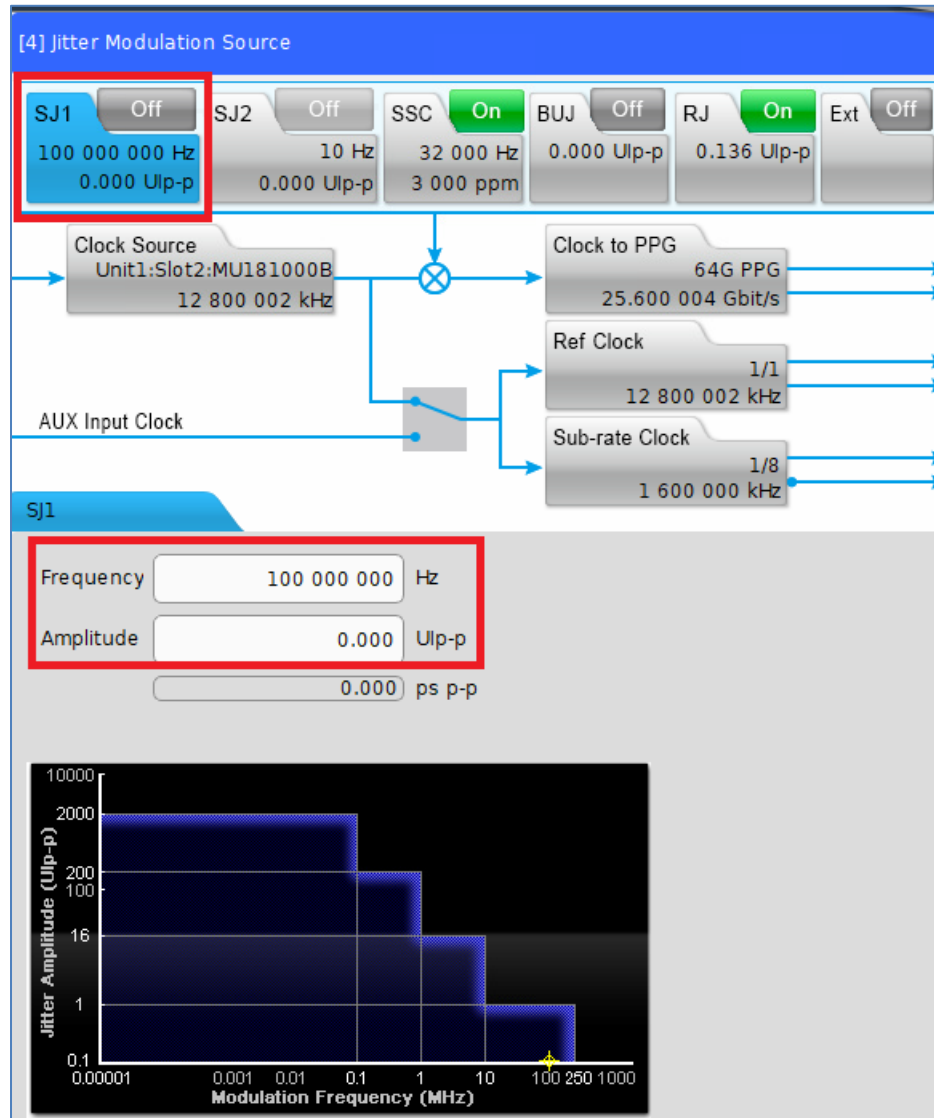


FIGURE 61. SJ1 SETTING

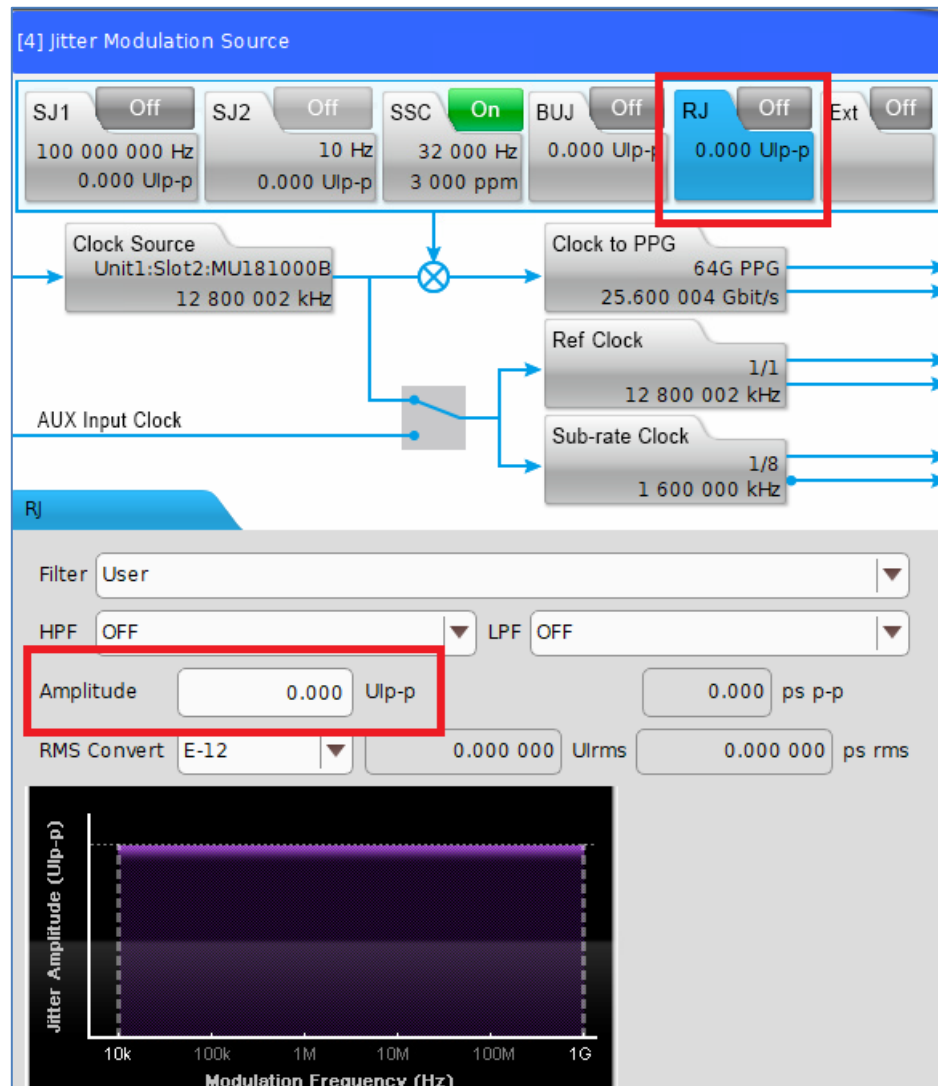


FIGURE 62. RJ SETTING

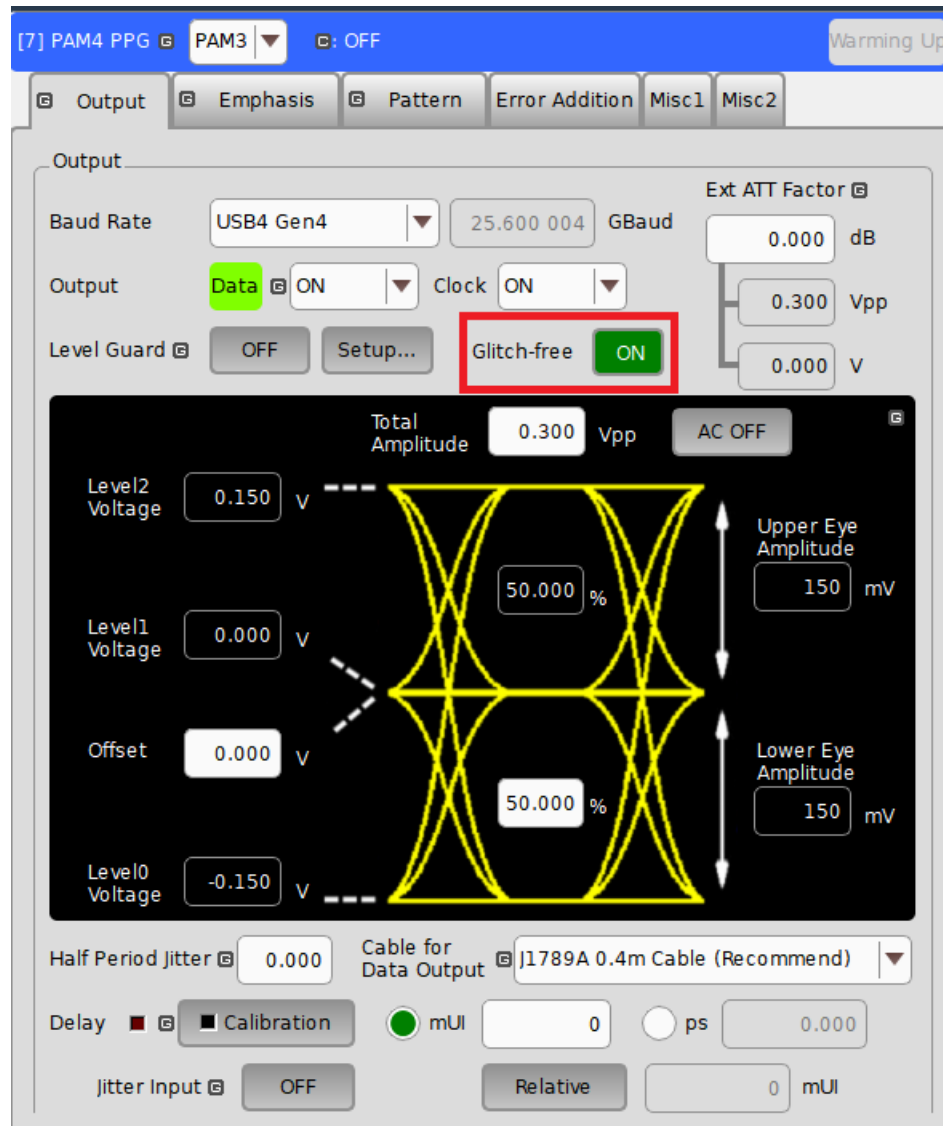


FIGURE 63. TURN ON GLITCH-FREE

9.1.2 Set Up Oscilloscope

9.1.2.1 Oscilloscope Vertical and Horizontal Setup for Waveform Capture

Set up the Scope as listed in Table 7.

TABLE 7. OSCILLOSCOPE VERTICAL AND HORIZONTAL SETUP

Setting	Setup
Vertical	Ch1-Ch3 (using the full range of the Scope's D/A)
Record Length	64M for Keysight UXR scope and 40M for other vendor scope in a single acquisition
Sample Rate	128 Gs/s for Keysight UXR scope and 80 Gs/s for other vendor scope
Averaging	OFF

Setting	Setup
Sample Mode	Real Time
Bandwidth	25GHz (which allows for 3 rd harmonic capture at 25.6GBaud/s)
Vertical Scale	Set to full screen without clipping
Sin x/x	OFF



FIGURE 64. OSCILLOSCOPE VERTICAL AND HORIZONTAL SETUP

9.1.2.2 Oscilloscope AC Common Mode (ACCM) Setup

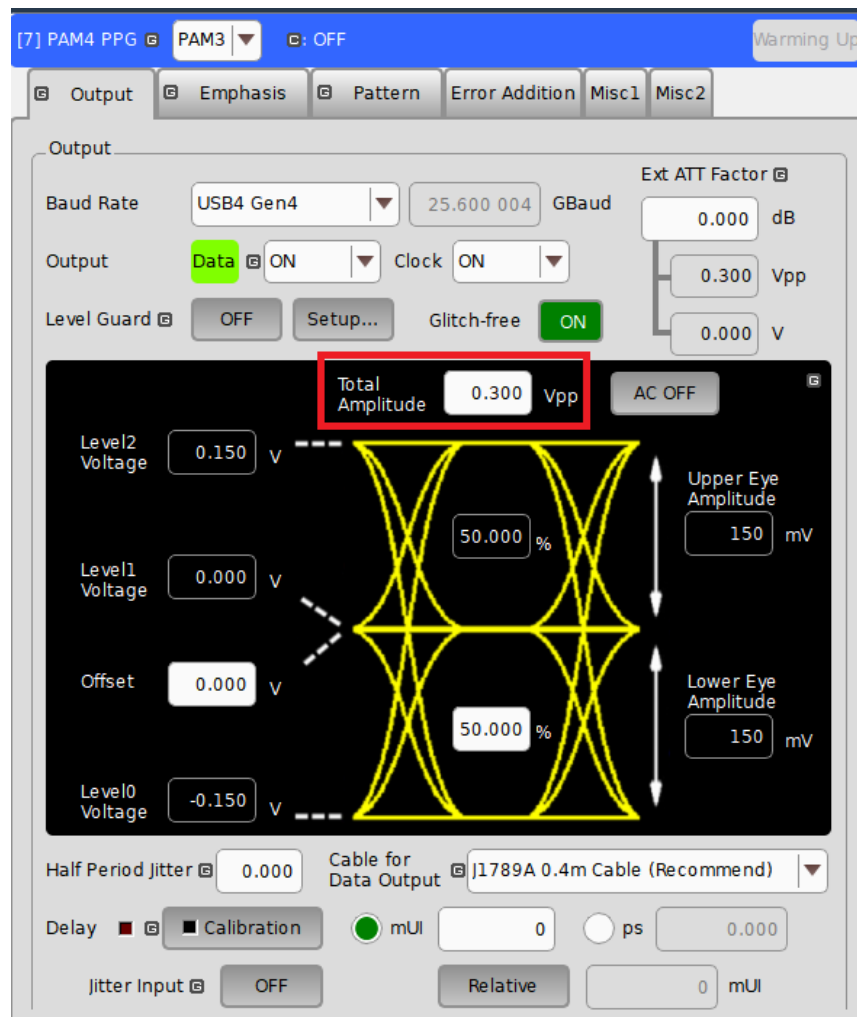
Set up the Scope as listed in Table 8.

TABLE 8. OSCILLOSCOPE ACCM SETUP

Setting	Setup
Sample Rate	128 Gs/s for Keysight UXR scope and 80 Gs/s for other vendor scope
Record Length	64M for Keysight UXR scope and 40M for other vendor scope in a single acquisition
Bandwidth	25 GHz
Vertical Scale	Set to full screen without clipping
CDR	OFF
Averaging	OFF
Sin x/x	OFF

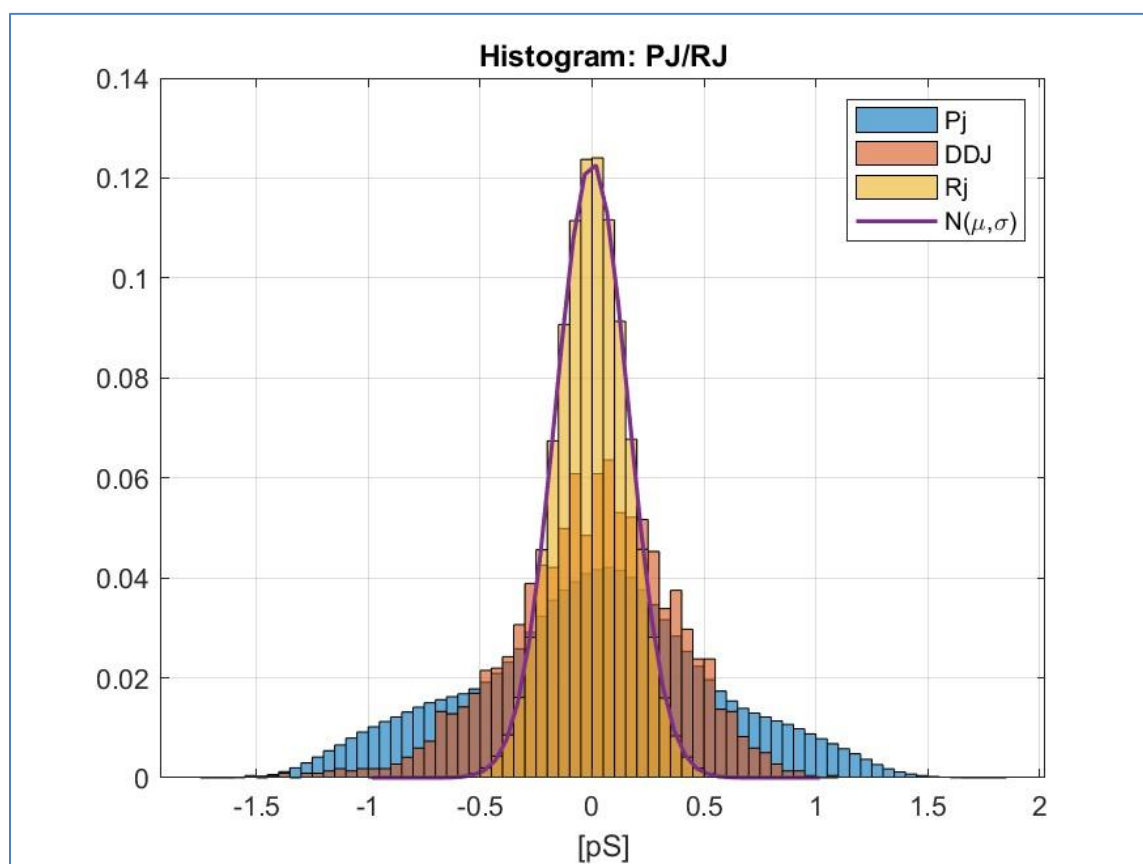
9.2 Voltage Swing Calibration for Case 1

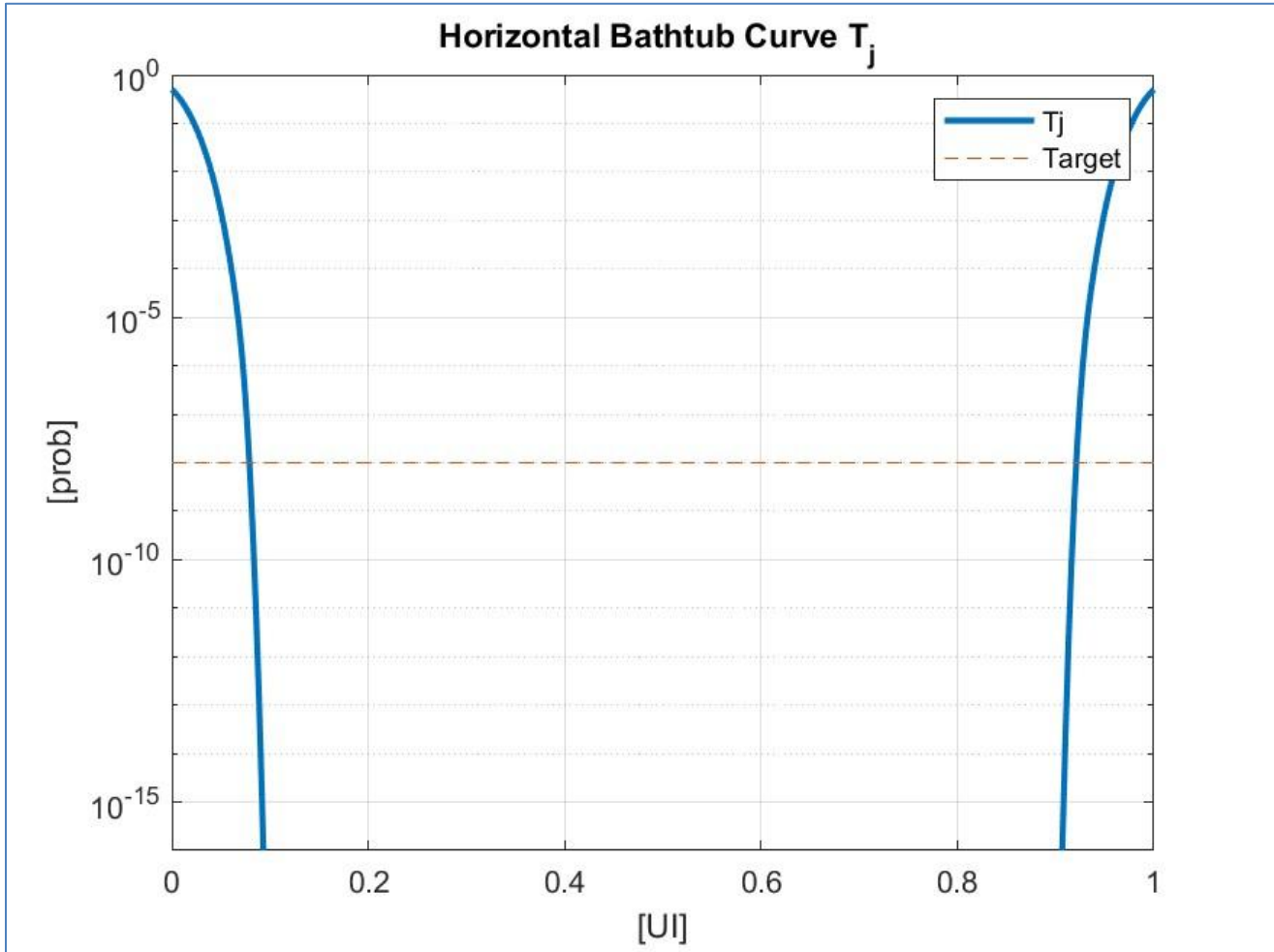
1. Turn off SJ1, RJ, DM and CM on the BERT.
2. Adjust the signal amplitude to achieve 1090 mV.
3. Set up the scope so that Channel 1 and Channel 3 scale to 80% of screen.
4. Capture a single-ended pair of signal waveform on the scope.
5. Run the SigTest tool according to section 8.3.1 of the SigTest User Manual documentation.



6. For SigTest measurement, use the following template:
 - Test Point: tp3_prime
 - CTS Test Template: calibration
 - Command example:
`.\USB4_SigTest.exe gen4 rx tp3_prime calibration C:\SigTest\Waveforms\p_prts7_preset_0.bin n_prts7_preset_0.bin calibration_report none`
7. Retrieve the Voltage Swing measurement.

Electrical Compliance Test Specification for GEN4			
Date:	5-Mar-24		
DIR:	C:\GRL\Rx Test Solution\Applications\USB4_V2_AN_RxTest\W		
Files:	p_TempWaveform0_preset_0.bin	n_TempWaveform0_preset_0.bi	
AC CM Measurement:	AC CM: Vac [mVp2p]	32.4	
PJ Jitter Measurement mUIp-p:	PJ-p-p	39.52967	
RJ Jitter Measurement mUIrms:	RJ-rms	3.728786	
Informative:	Symbol Rate [GHz]	25.5565	Drift [PPM] -1699.37
Vertical Analysis Test:			
TX_SNR Measurement [dB]:	TX_SNR [dB]	42.00339	
TX_LEVELS_MISMATCH Measurement:	TX_LEVELS_MISMATCH	0.999655	
V_SWING Measurement [mVp-p]:	V_SWING-p-p	1096.8	

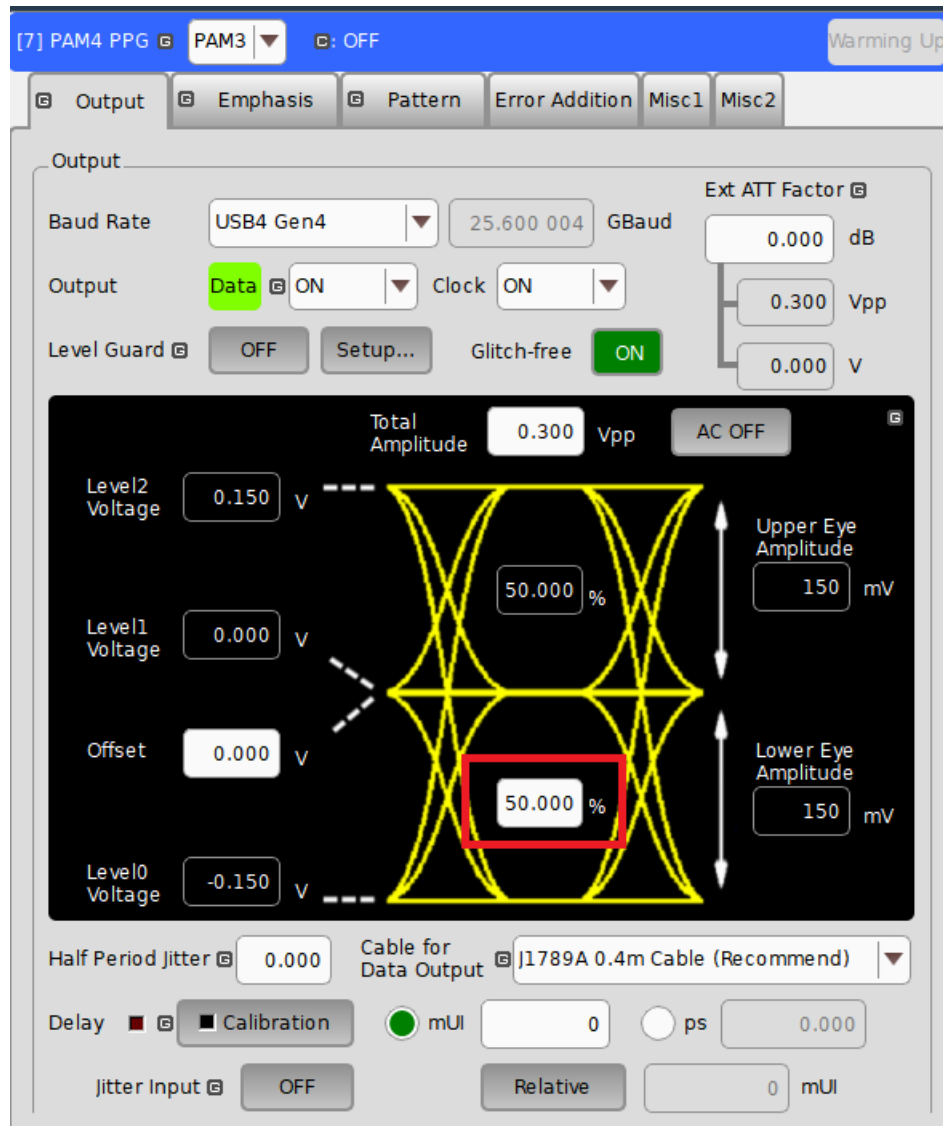




8. Adjust the BERT voltage swing setting and repeat Steps 2 to 7 until the desired result is achieved.

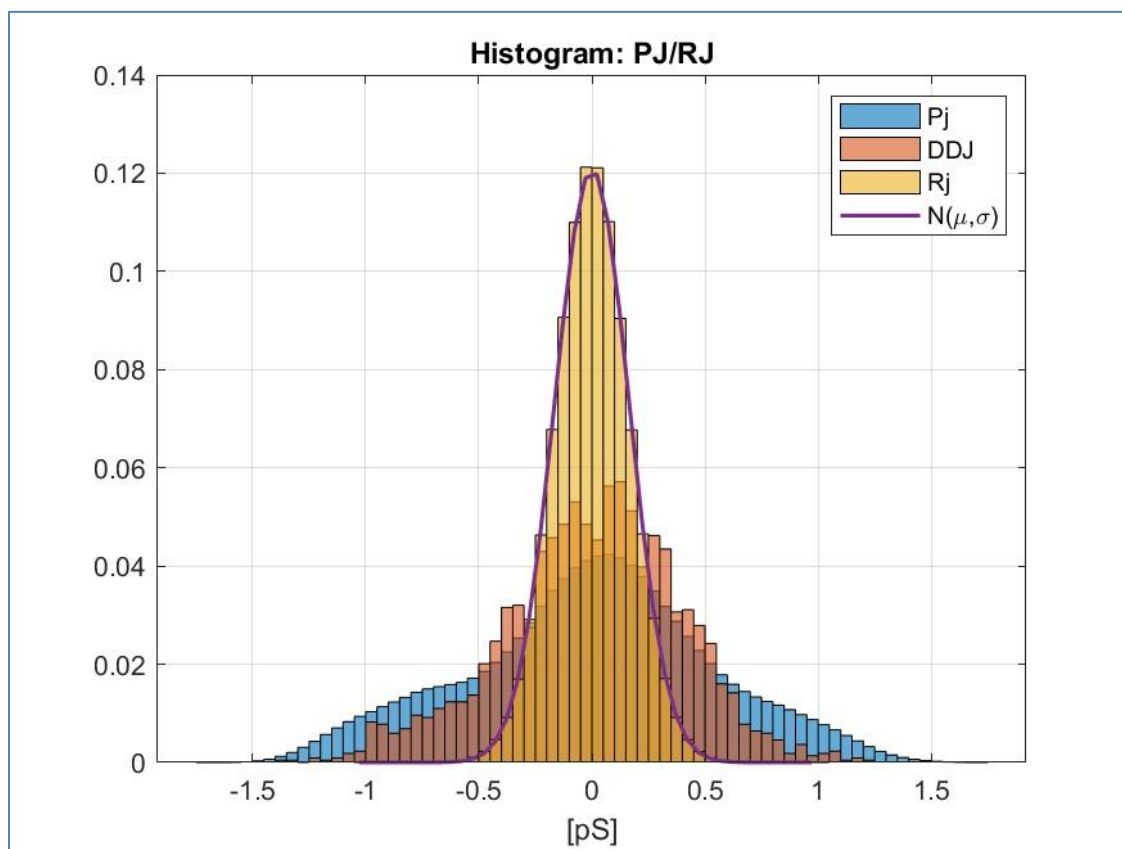
9.3 Level Mismatch Calibration for Case 1

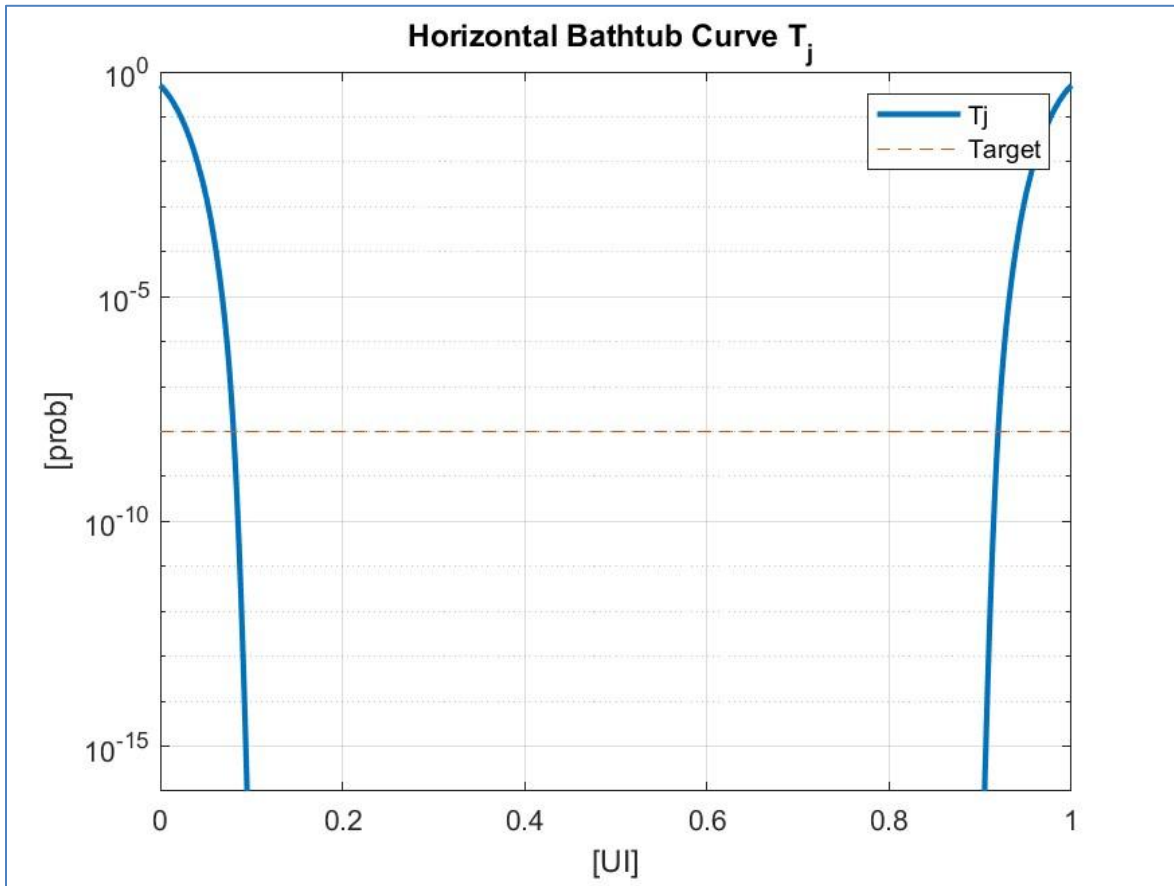
1. Keep the Voltage Swing as calibrated in the previous step.
2. Turn off SJ1, RJ, DM and CM on the BERT.
3. Adjust the Lower Eye Percentage on the BERT to achieve 0.975.
4. Capture a single-ended pair of signal waveform on the scope.



5. Run the SigTest tool according to section 8.3.1 of the SigTest User Manual documentation.
6. For SigTest measurement, use the following template:
 - Test Point: tp3_prime
 - CTS Test Template: calibration
 - Command example:
`.\USB4_SigTest.exe gen4 rx tp3_prime calibration C:\SigTest\Waveforms\p_prts7_preset_0.bin n_prts7_preset_0.bin calibration_report none`
7. Retrieve Level Mismatch measurement.

Electrical Compliance Test Specification for GEN4			
Date:	5-Mar-24		
DIR:	C:\GRL\Rx Test Solution\Applications\USB4_V2_AN_RxTest\AppData\Waveforms\		
Files:	p_TempWaveform0_preset_0.bin n_TempWaveform0_preset_0.bin		
AC CM Measurement:	AC CM: Vac [mVp2p]	31.4	
PJ Jitter Measurement mUIp-p:	PJ-p-p	39.213	
RJ Jitter Measurement mUIrms:	RJ-rms	3.69517	
Informative:	Symbol Rate [GHz]	25.5565	Drift [PPM] -1699.31
Vertical Analysis Test:			
TX_SNR Measurement [dB]:	TX_SNR [dB]	41.46291	
TX_LEVELS_MISMATCH Measurement:	TX_LEVELS_MISMATCH	0.97054	
V_SWING Measurement [mVp-p]:	V_SWING-p-p	1095.2	

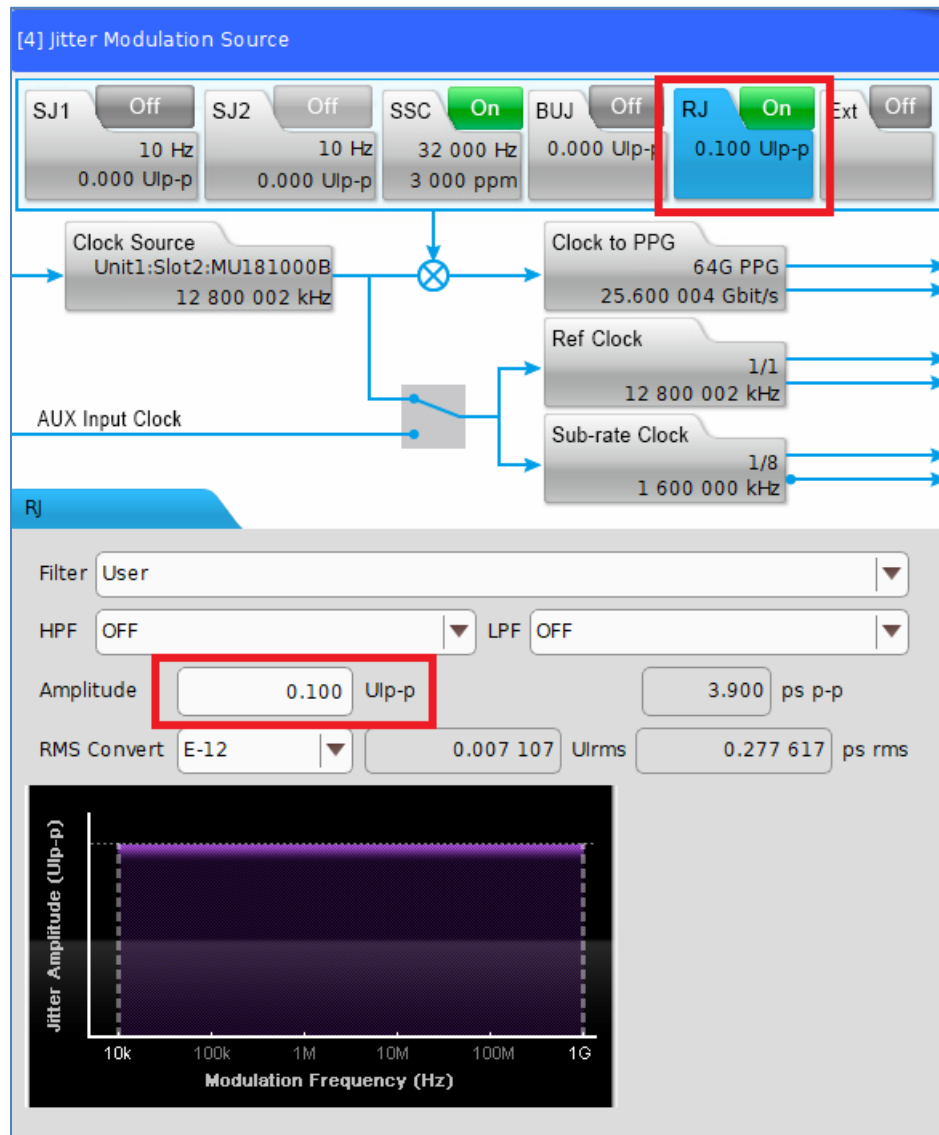




8. Adjust the BERT Level2 Voltage setting and repeat Steps 3 to 7 until the desired result is achieved.

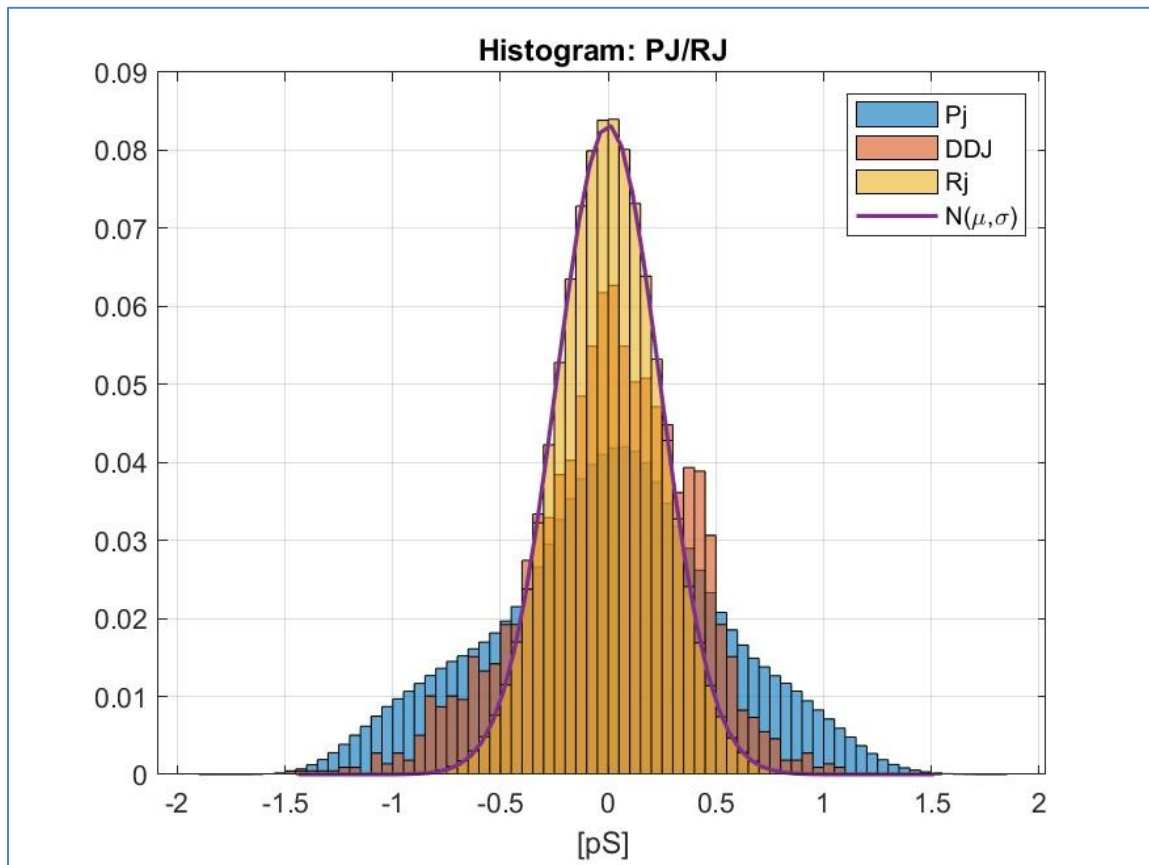
9.4 RJ Calibration for Case 1

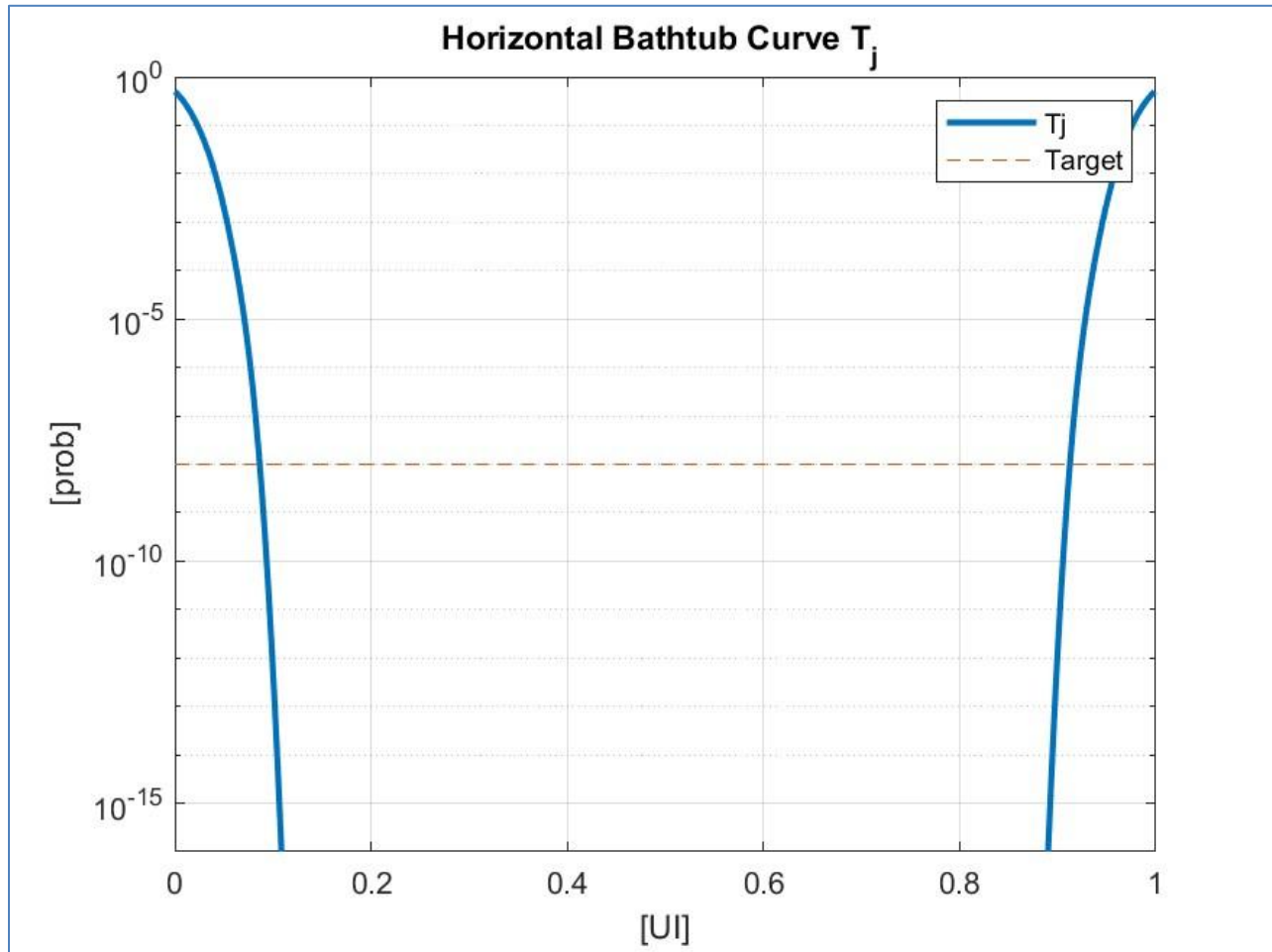
1. Keep the Voltage Swing and Level Mismatch as calibrated in the previous step.
2. Turn off SJ1, DM and CM on the BERT.
3. Adjust RJ on the BERT to achieve 0.0085 UIrms.
4. Capture a single-ended pair of signal waveform on the scope.



5. Run the SigTest tool according to section 8.3.1 of the SigTest User Manual documentation.
6. For the SigTest measurement, use the following template:
 - Test Point: tp3_prime
 - CTS Test Template: calibration
 - Command example:
`.\USB4_SigTest.exe gen4 rx tp3_prime calibration C:\SigTest\Waveforms\p_prts7_preset_0.bin n_prts7_preset_0.bin calibration_report none`
7. Retrieve the RJ measurement.
8. Adjust the BERT RJ setting and repeat Steps 3 to 7 until the desired result is achieved.

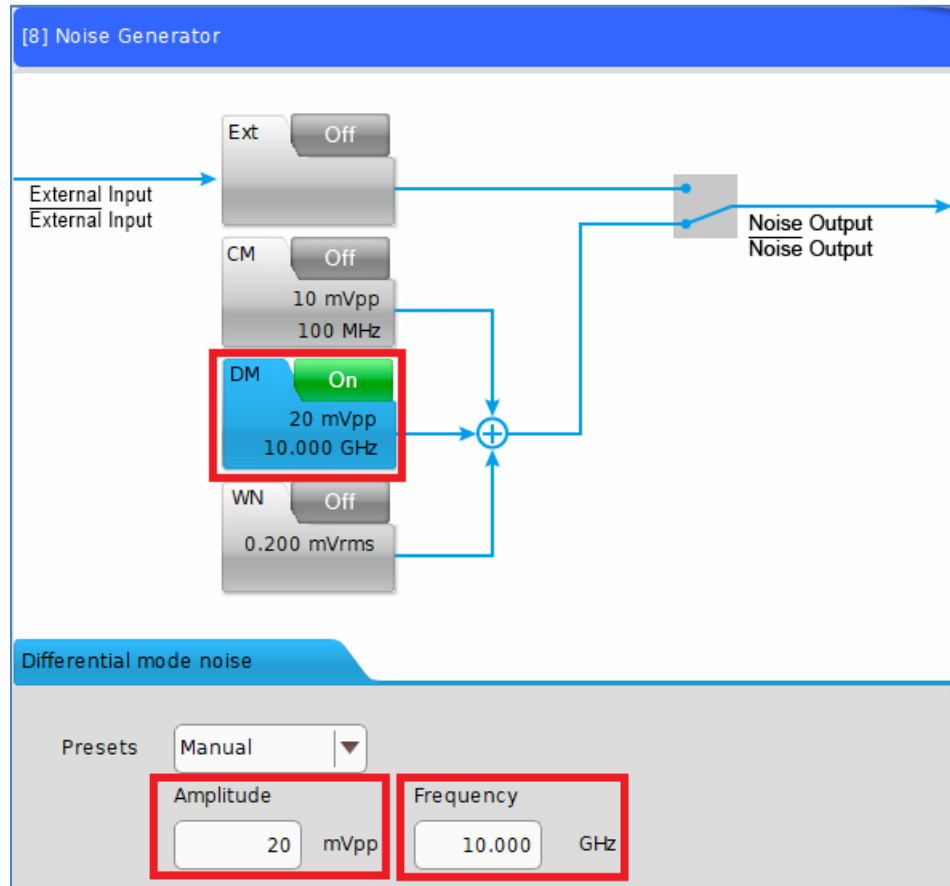
Electrical Compliance Test Specification for GEN4			
Date:	5-Mar-24		
DIR:	C:\GRL\Rx Test Solution\Applications\USB4_V2_AN_RxTest\AppData\Waveforms\		
Files:	p_TempWaveform0_preset_0.tn_TempWaveform0_preset_0.bin		
AC CM Measurement:	AC CM: Vac [mVp2p]	31.1	
PJ Jitter Measurement mUIp-p:	PJ-p-p	38.208906	
RJ Jitter Measurement mUIrms:	RJ-rms	8.42817	
Informative:	Symbol Rate [GHz]	25.556481	Drift [PPM] -1699.96
Vertical Analysis Test:			
TX_SNR Measurement [dB]:	TX_SNR [dB]	41.468619	
TX_LEVELS_MISMATCH Measurement:	TX_LEVELS_MISMATCH	0.97055	
V_SWING Measurement [mVp-p]:	V_SWING-p-p	1093.9	





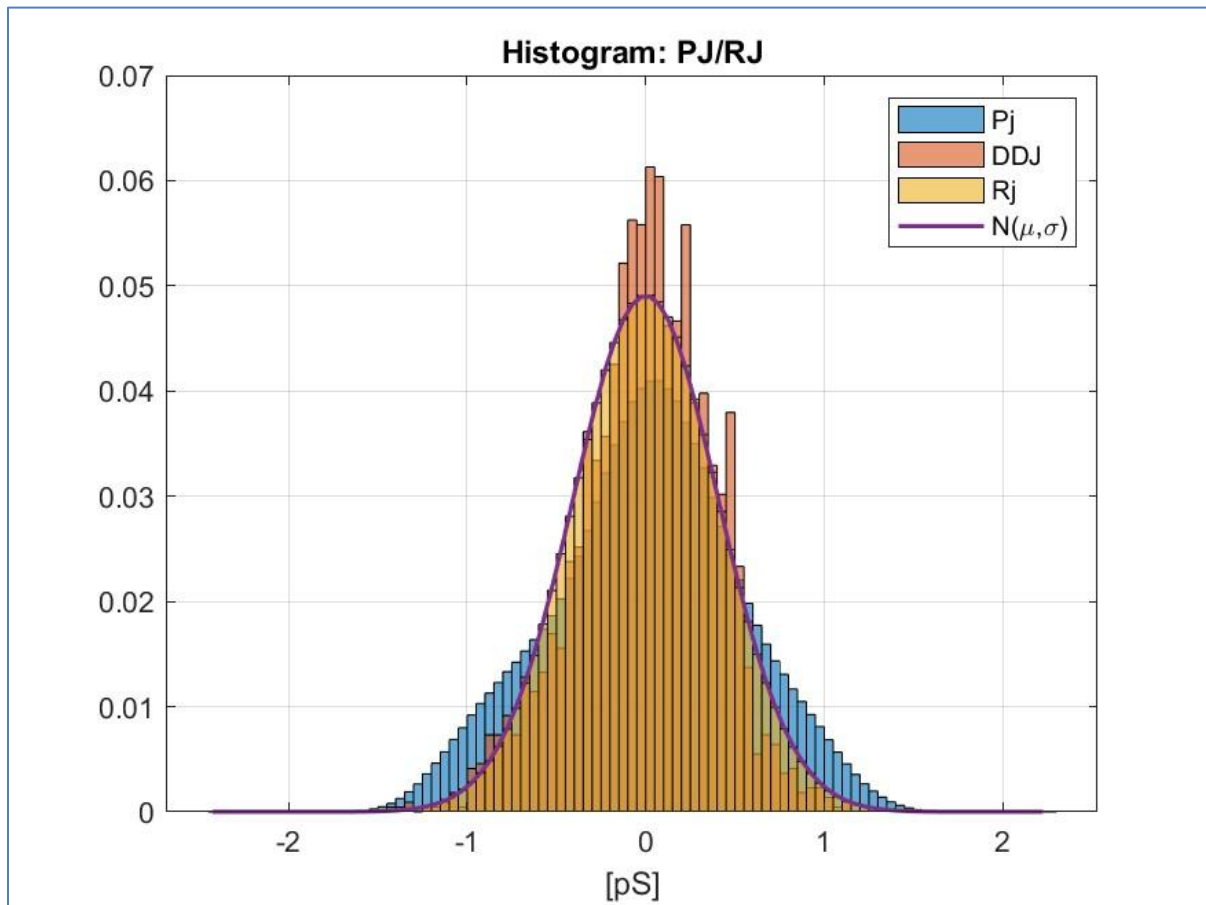
9.5 SNDR Calibration for Case 1

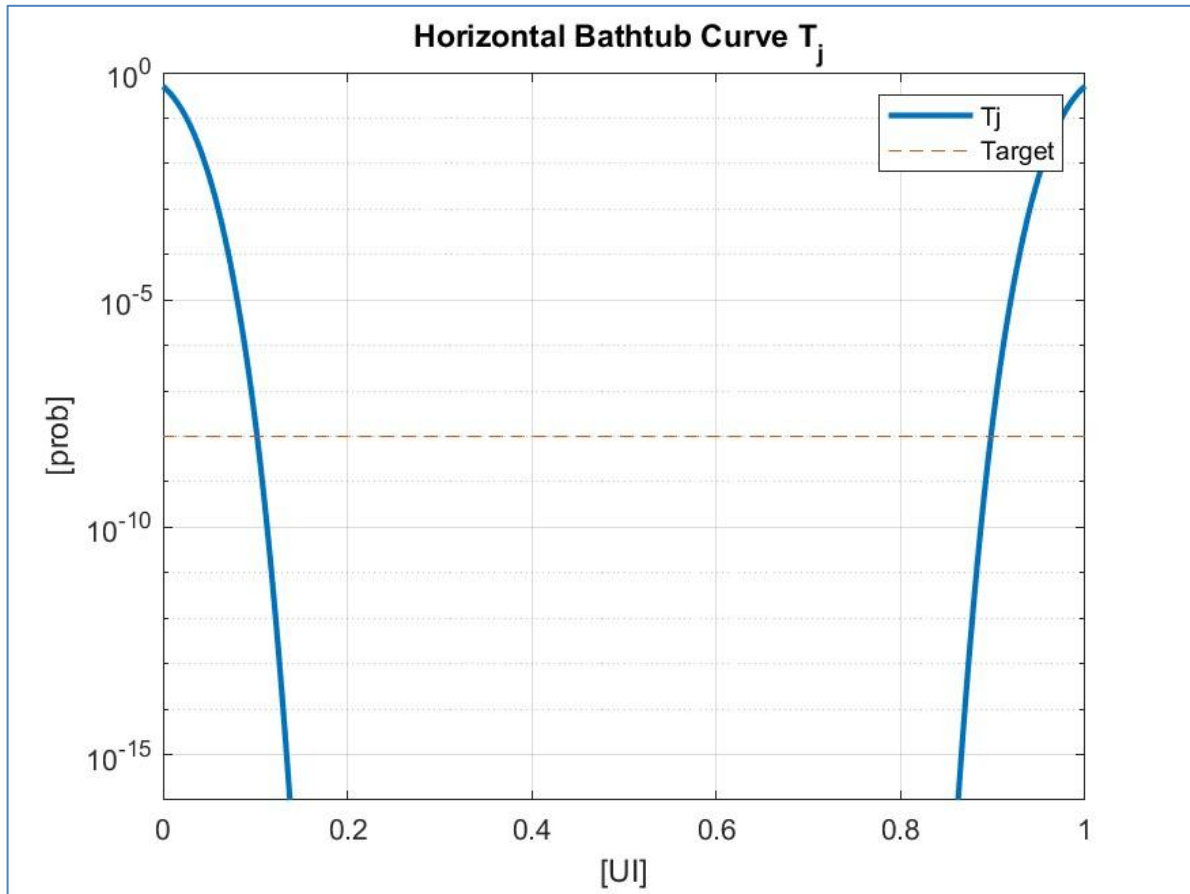
1. Keep the Voltage Swing, Level Mismatch and RJ as calibrated in the previous step.
2. Turn off SJ1 and CM on the BERT.
3. Set the DM frequency setting on the BERT to 10 GHz.
4. Adjust the DM amplitude to achieve 32.5 dB.



5. Run the SigTest tool according to section 8.3.1 of the SigTest User Manual documentation.
6. For the SigTest measurement, use the following template:
 - Test Point: tp3_prime
 - CTS Test Template: calibration
 - Command example:
`.\USB4_SigTest.exe gen4 rx tp3_prime calibration C:\SigTest\Waveforms\p_prt7_preset_0.bin n_prt7_preset_0.bin calibration_report none`
7. Retrieve the SNDR measurement.
8. Adjust the BERT DM amplitude setting and repeat Steps 4 to 7 until the desired result is achieved.

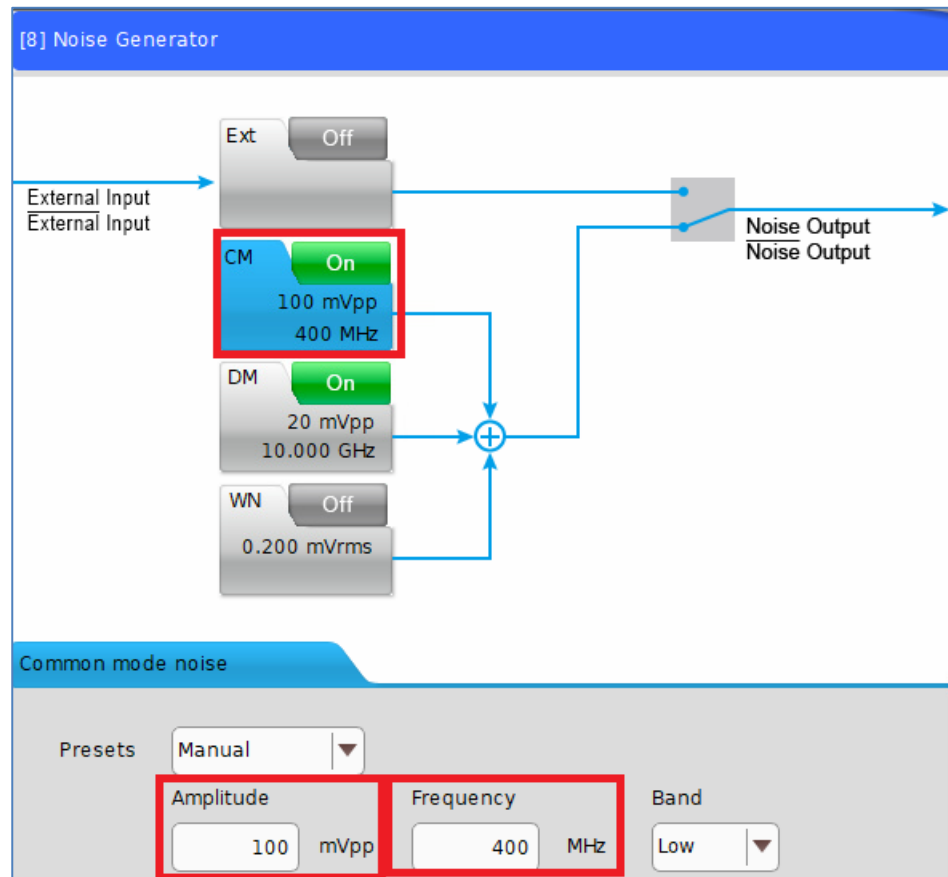
Electrical Compliance Test Specification for GEN4			
Date:	6-Mar-24		
DIR:	C:\GRL\Rx Test Solution\Applications\USB4_V2_AN_RxTest\AppData\Waveforms\		
Files:	p_TempWaveform0_preset_(n_TempWaveform0_preset_0.bin		
AC CM Measurement:	AC CM: Vac [mVp2p]	33	
PJ Jitter Measurement mUIp-p:	PJ-p-p	38.438592	
RJ Jitter Measurement mUIrms:	RJ-rms	10.204135	
Informative:	Symbol Rate [GHz]	25.556492	Drift [PPM] -1699.53
Vertical Analysis Test:			
TX_SNR Measurement [dB]:	TX_SNR [dB]	32.521909	
TX_LEVELS_MISMATCH Measurement:	TX_LEVELS_MISMATCH	0.97053	
V_SWING Measurement [mVp-p]:	V_SWING-p-p	1094.3	





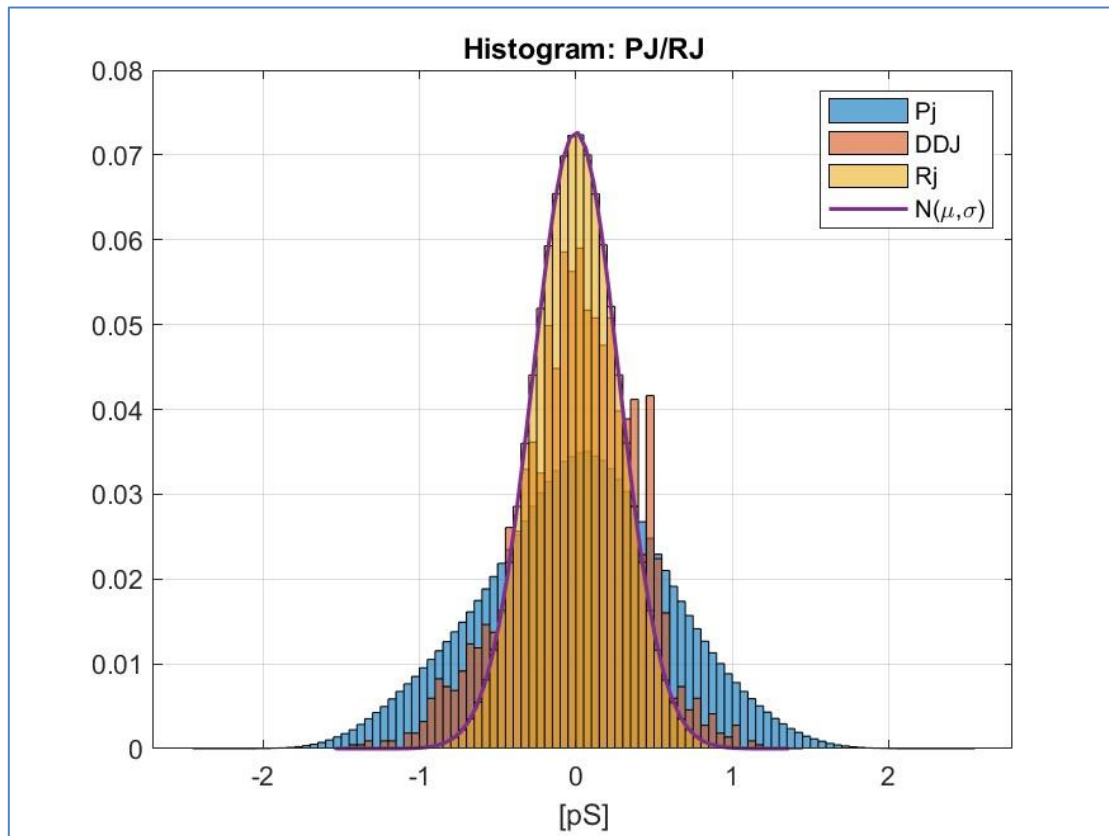
9.6 ACCM Calibration for Case 1

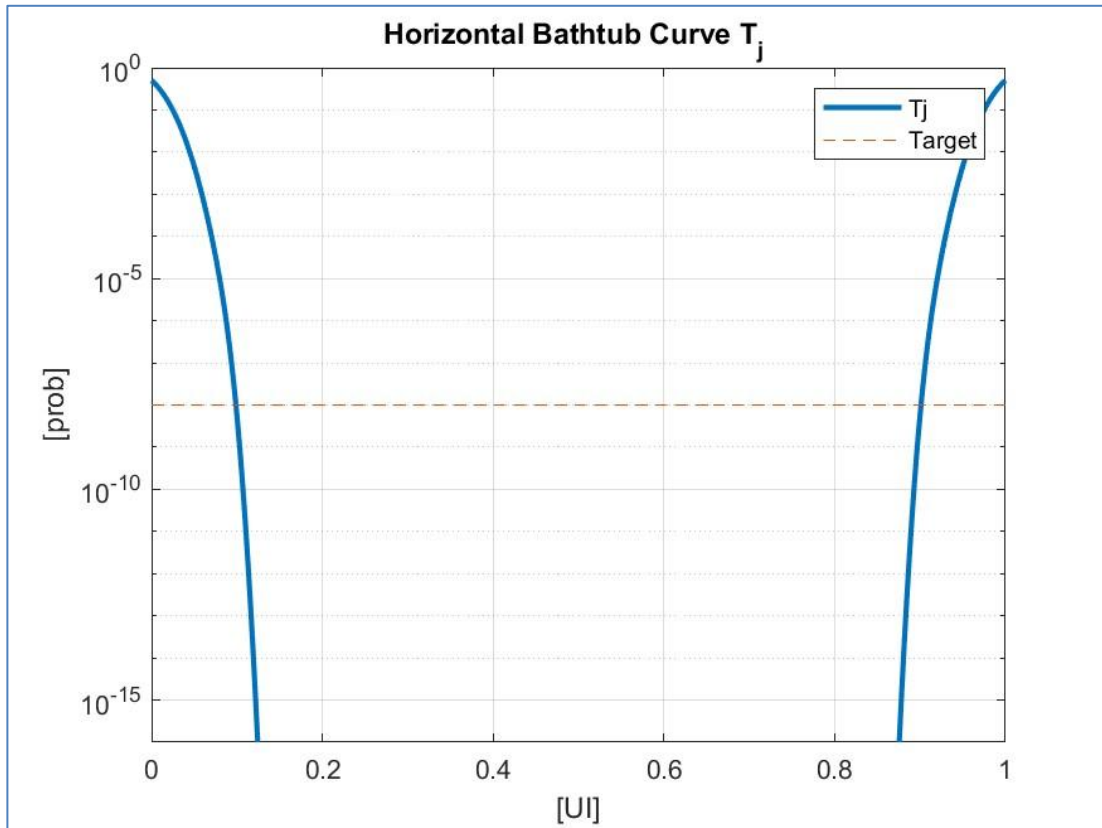
1. Keep the Voltage Swing, Level Mismatch, RJ and SNDR as calibrated in the previous step.
2. Turn off SJ on the BERT.
3. Set the CM frequency setting on the BERT to 400 MHz.
4. Adjust the CM amplitude to achieve 100 mV.



5. Run the SigTest tool according to section 8.3.1 of the SigTest User Manual documentation.
6. For the SigTest measurement, use the following template:
 - Test Point: tp3_prime
 - CTS Test Template: calibration
 - Command example:
`.\USB4_SigTest.exe gen4 rx tp3_prime calibration C:\SigTest\Waveforms\p_prts7_preset_0.bin n_prts7_preset_0.bin calibration_report none`
7. Retrieve the SNDR measurement.
8. Adjust the BERT CM amplitude setting and repeat Steps 4 to 7 until the desired result is achieved.

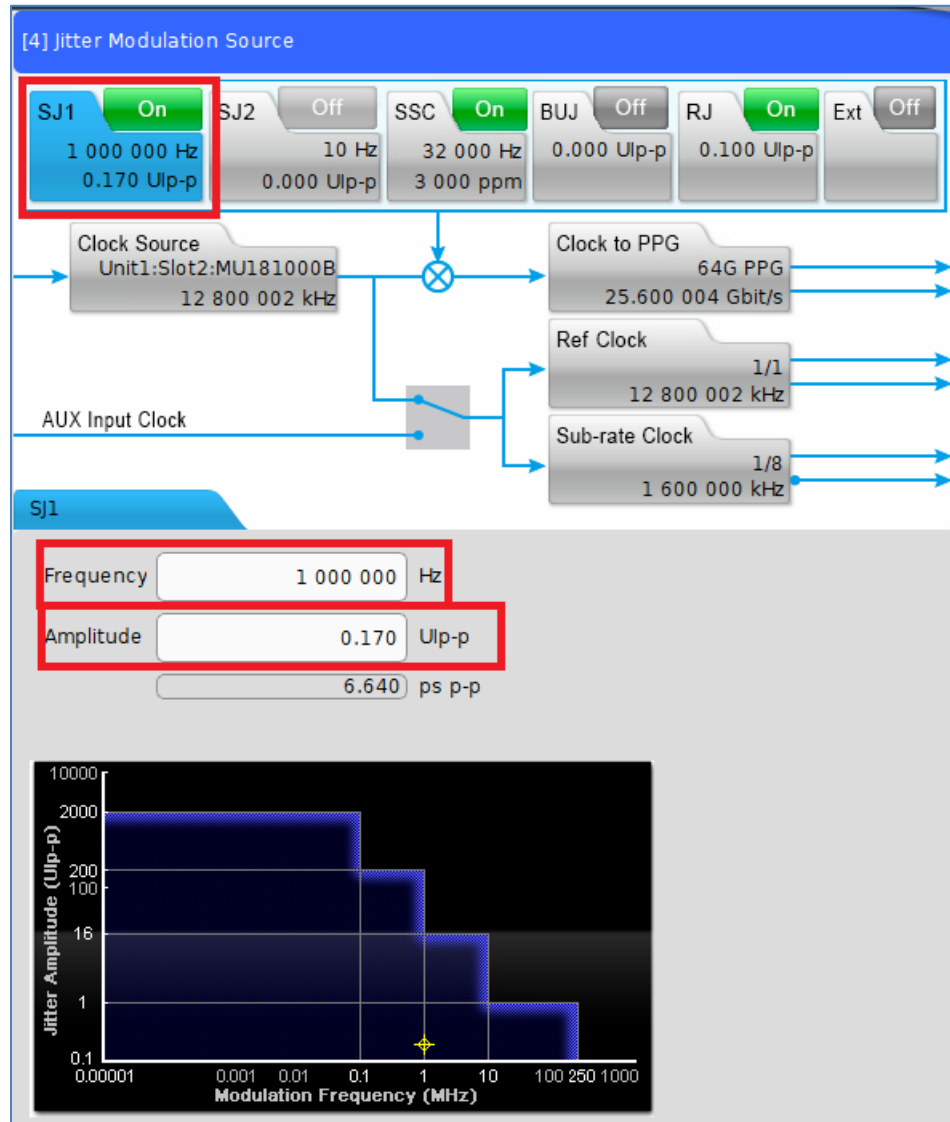
Electrical Compliance Test Specification for GEN4			
Date:	6-Mar-24		
DIR:	C:\GRL\Rx Test Solution\Applications\USB4_V2_AN_RxTest\AppData\Waveforms\		
Files:	p_TempWaveform0_preset_0.in TempWaveform0_preset_0.bin		
AC CM Measurement:	AC CM: Vac [mVp2p]	108	
PJ Jitter Measurement mUIp-p:	PJ-p-p	43.00221	
RJ Jitter Measurement mUIrms:	RJ-rms	6.714589	
Informative:	Symbol Rate [GHz]	25.5565	Drift [PPM] -1699.35
Vertical Analysis Test:			
TX_SNR Measurement [dB]:	TX_SNR [dB]	29.81099	
TX_LEVELS_MISMATCH Measurement:	TX_LEVELS_MISMATCH	0.970545	
V_SWING Measurement [mVp-p]:	V_SWING-p-p	1094.5	





9.7 PJ Calibration for Case 1

1. Keep the Voltage Swing, Level Mismatch, RJ, SNDR and ACCM as calibrated in the previous step.
2. Set the SJ1 frequency setting on the BERT to 1 MHz.
3. Adjust the SJ1 amplitude to achieve 0.085 UIpp.
4. Run the SigTest tool according to section 8.3.1 of the SigTest User Manual documentation.

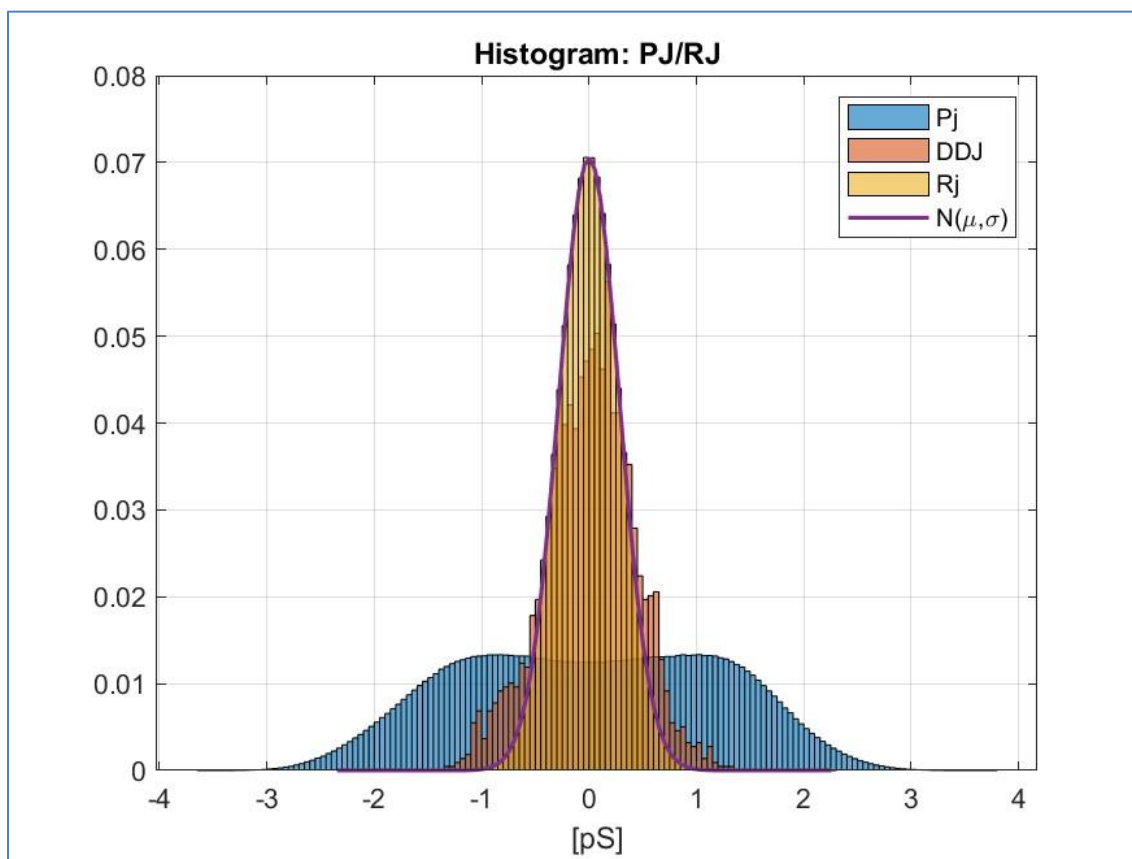


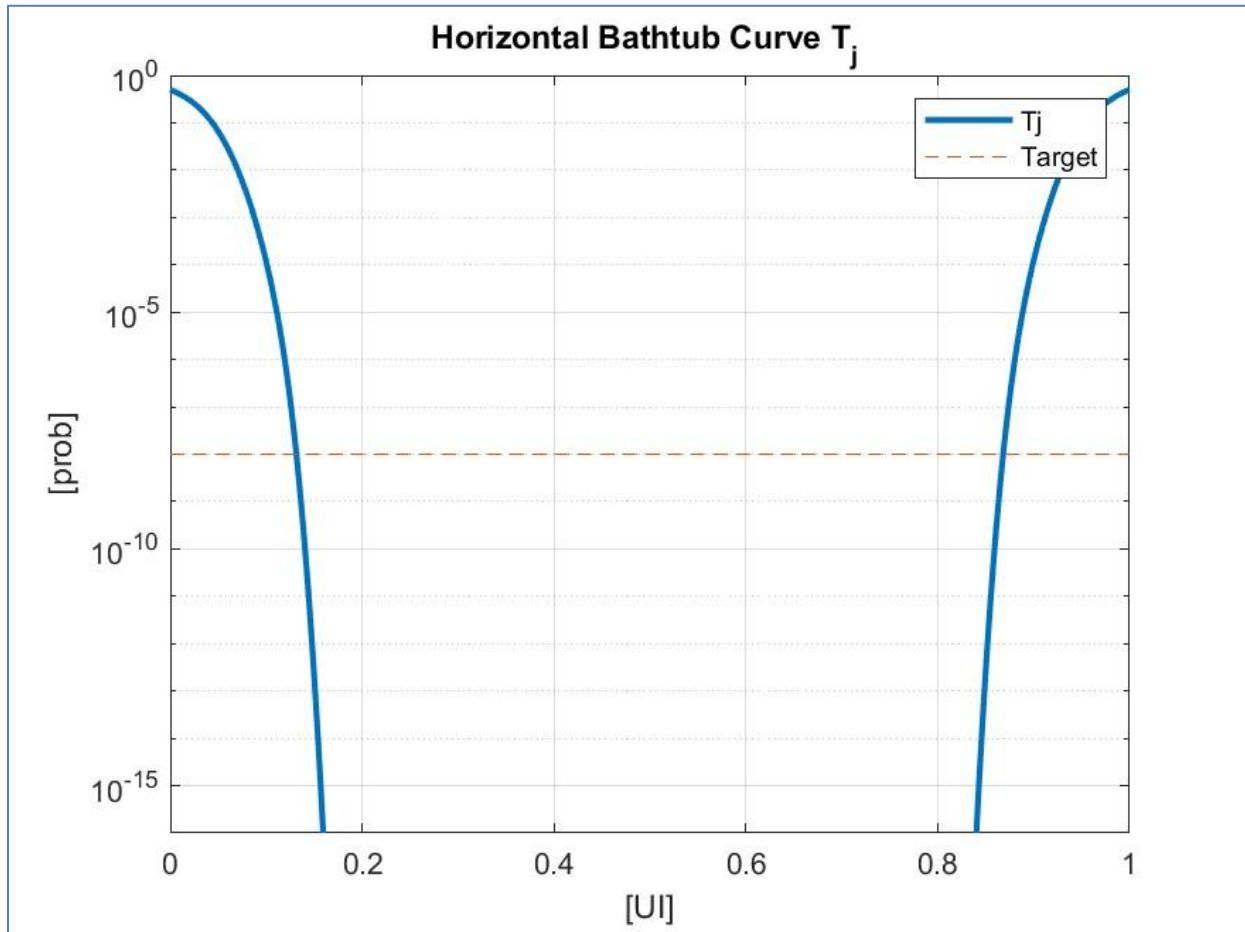
5. For the SigTest measurement, use the following template:

- Test Point: tp3_prime
- CTS Test Template: calibration
- Command example:
`.\USB4_SigTest.exe gen4 rx tp3_prime calibration C:\SigTest\Waveforms\p_prt7_preset_0.bin n_prt7_preset_0.bin calibration_report none`

6. Retrieve PJ measurement.

Electrical Compliance Test Specification for GEN4			
Date:	6-Mar-24		
DIR:	C:\GRL\Rx Test Solution\Applications\USB4_V2_AN_RxTest\AppData\Waveforms\		
Files:	p_TempWaveform0_preset_0.bin	n_TempWaveform0_preset_0.bin	
AC CM Measurement:	AC CM: Vac [mVp2p]	107.9	
PJ Jitter Measurement mUIp-p:	PJ-p-p	86.63197	
RJ Jitter Measurement mUIrms:	RJ-rms	6.923409	
Informative:	Symbol Rate [GHz]	25.5565	Drift [PPM] -1699.21
Vertical Analysis Test:			
TX_SNR Measurement [dB]:	TX_SNR [dB]	29.91998	
TX_LEVELS_MISMATCH Measurement:	TX_LEVELS_MISMATCH	0.970551	
V_SWING Measurement [mVp-p]:	V_SWING-p-p	1095.1	





7. Adjust BERT SJ1 amplitude setting and repeat steps 3-7 until desired result is achieved.
8. Repeat step 2-7 for remaining PJ frequencies(2 Mhz, 10 MHz, 50 MHz, 100 MHz).
9. Save BERT setup as Test Case 1 for each PJ frequency.

9.8 Initialize Setting of BERT and Scope for Calibrate Receiver Stressed Eye for Case 2

Set up the physical equipment connections without the ISI channel, as per Figure 10.

9.8.1 Set up the MP1900A BERT as follows:

- i. Go to Menu Bar → File → Initialize.
- ii. Switch modulation type to “PAM3”. See Figure 65.
- iii. Go to Jitter tab and set Clock Source to “Unit1:Slot2:MU181000B”. See Figure 66.
- iv. Go to PPG → Misc2.
- v. Set Clock Source to “Unit1:Slot4:MU181500B”. See Figure 67.
- vi. Set Bit Rate to 25.6 Gbit/s. See Figure 67.
- vii. Set Offset (ppm) to 0 ppm.
- viii. Set Output Clock Rate to “Halfrate”. See Figure 67.
- ix. Set Test Pattern on PPG to “PRTS” and Length to “3⁷-1” bits. See Figure 68.
- x. Turn on PPG Data Output.
- xi. Go to PPG → Emphasis tab and turn on “Manual Setting”. See Figure 69.
- xii. Turn on “SSC”, with settings of 32kHz with 3000ppm triangle down spread. (SSC will remain on for all of the following steps.) See Figure 70.
- xiii. Adjust Total Amplitude on the BERT. A differential amplitude just over the 820mV voltage swing should show as an initial value.
- xiv. Set initial CM frequency to 400MHz and amplitude to 0 mVpp. Turn off CM output. See Figure 71.
- xv. Set initial DM frequency to 10GHz and amplitude to 0 mVpp. Turn off DM output. See Figure 71.
- xvi. Set SJ1 frequency to 100 MHz and amplitude to 0 U1pp. Turn off SJ1 output. See Figure 72.
- xvii. Set RJ amplitude to 0 U1pp and turn off RJ output. See Figure 73.
- xviii. Go to PPG → Output.
- xix. Turn on Glitch-free. See Figure 74.

[7] PAM4 PPG PAM3 ▼ Q: OFF Warming Up

Output Emphasis Pattern Error Addition Misc1 Misc2

Clock Setting

Clock Source Unit1:Slot4:MU181500B ▼

Bit Rate USB4 Gen4 ▼ 25.600 004 GBaud

Offset 0 ppm

Output Clock Rate Halfrate ▼ Max: 64.200G

Reference Clock Internal ▼

FIGURE 65. MODULATION TYPE “PAM3” SETTING

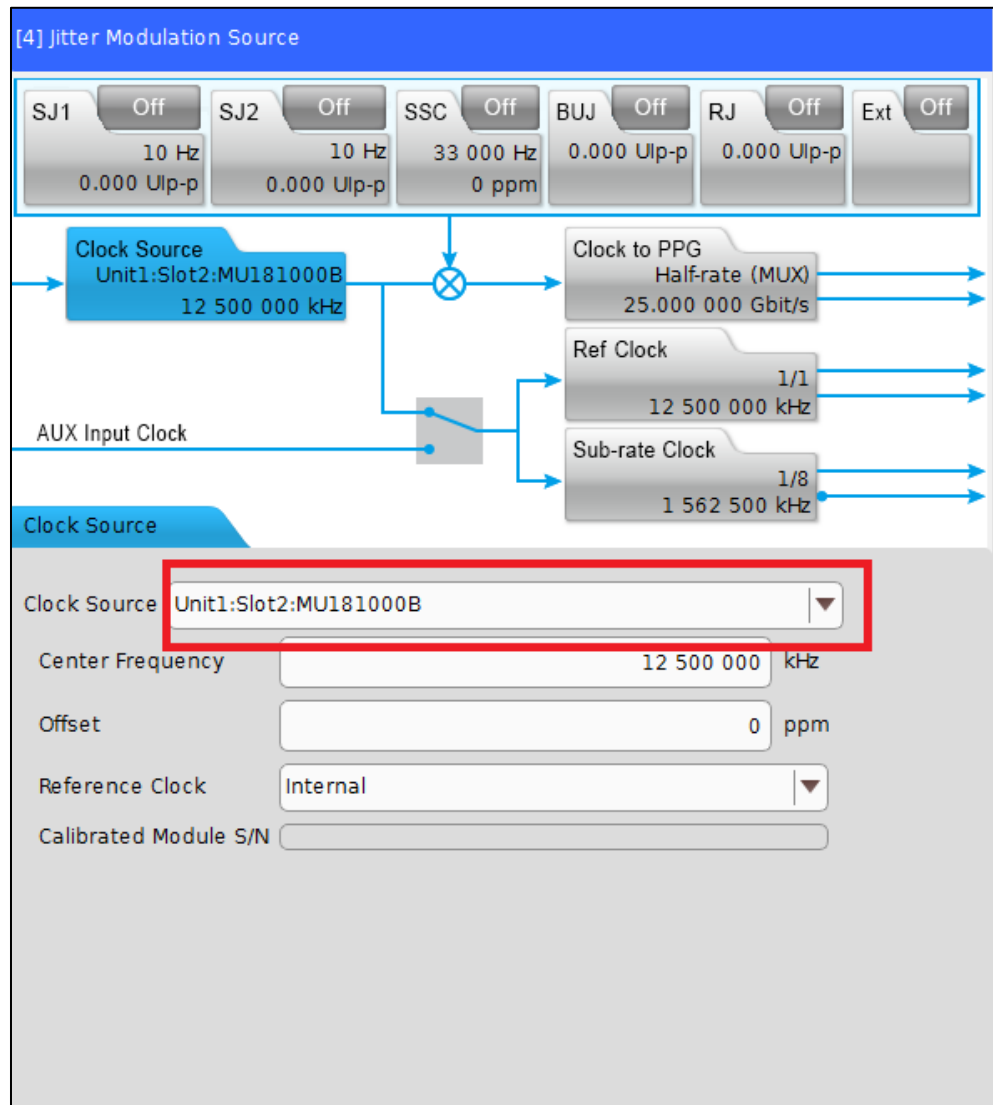


FIGURE 66. JITTER CLOCK SOURCE SETTING

[7] PAM4 PPG
PAM3
C: OFF
Warming Up

Output

Emphasis

Pattern

Error Addition

Misc1

Misc2

Clock Setting

Clock Source Unit1:Slot4:MU181500B

Bit Rate USB4 Gen4 25.600 004 GBaud

Offset 0 ppm

Output Clock Rate Halfrate Max: 64.200G

Reference Clock Internal

FIGURE 67. PPG MISC2 SETTINGS

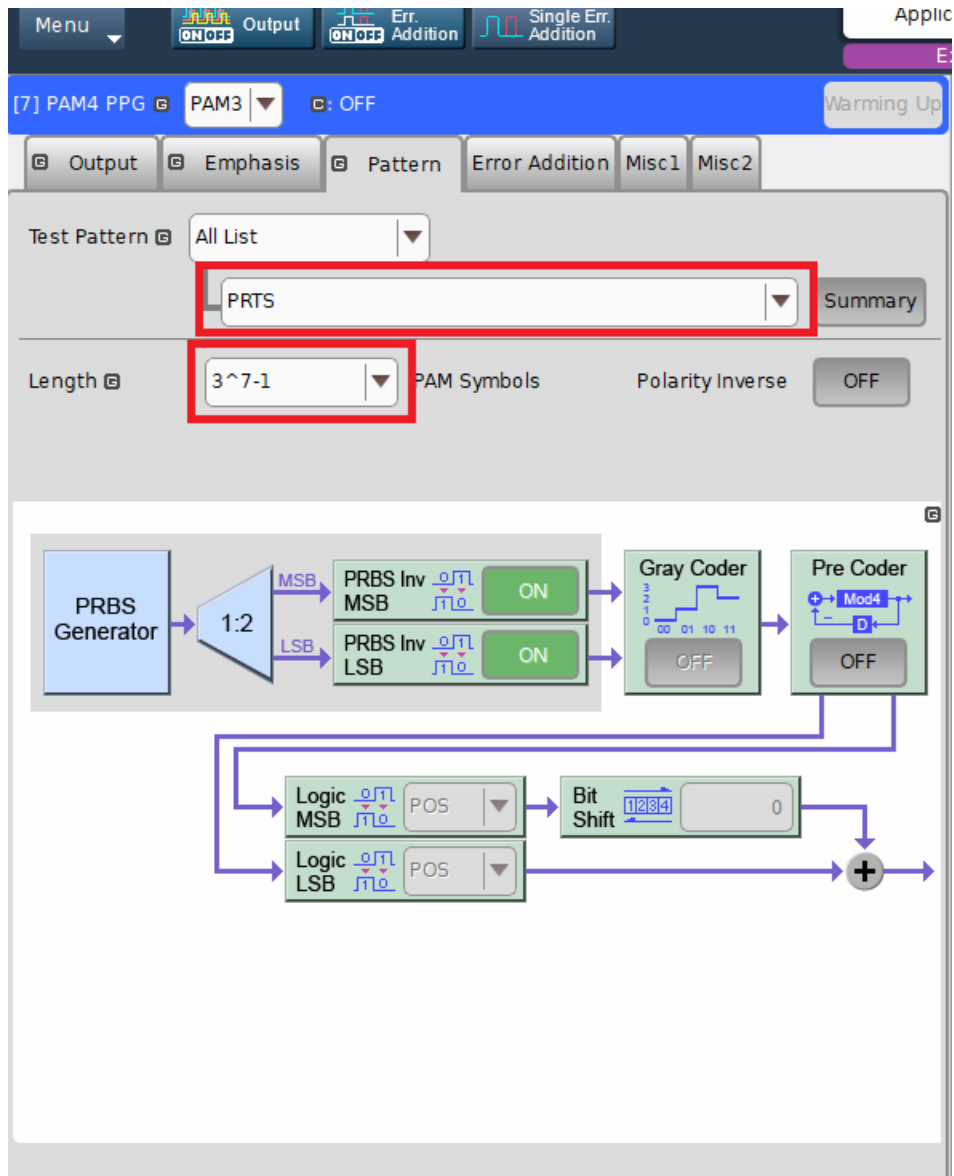


FIGURE 68. PATTERN SETTING

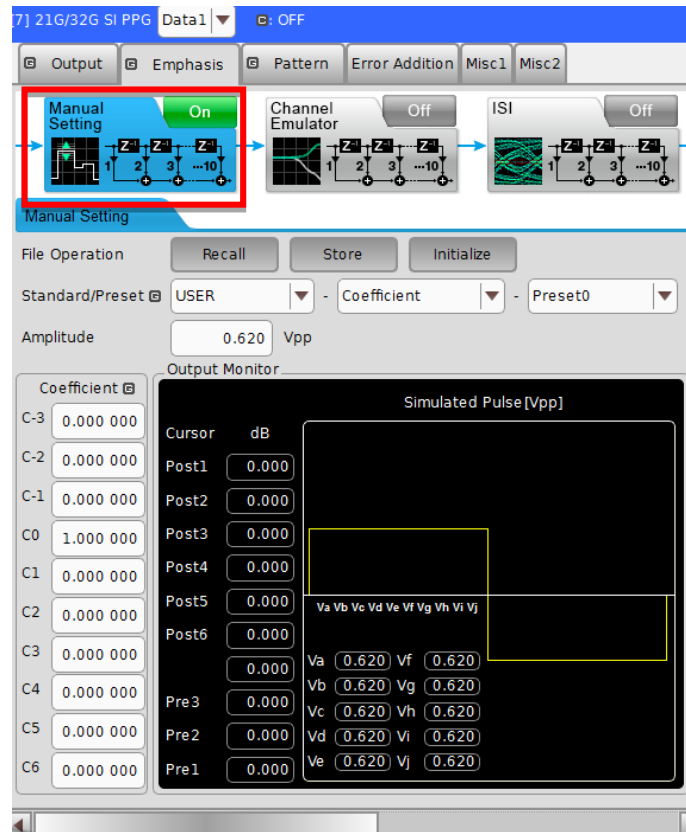


FIGURE 69. PPG EMPHASIS SETTING

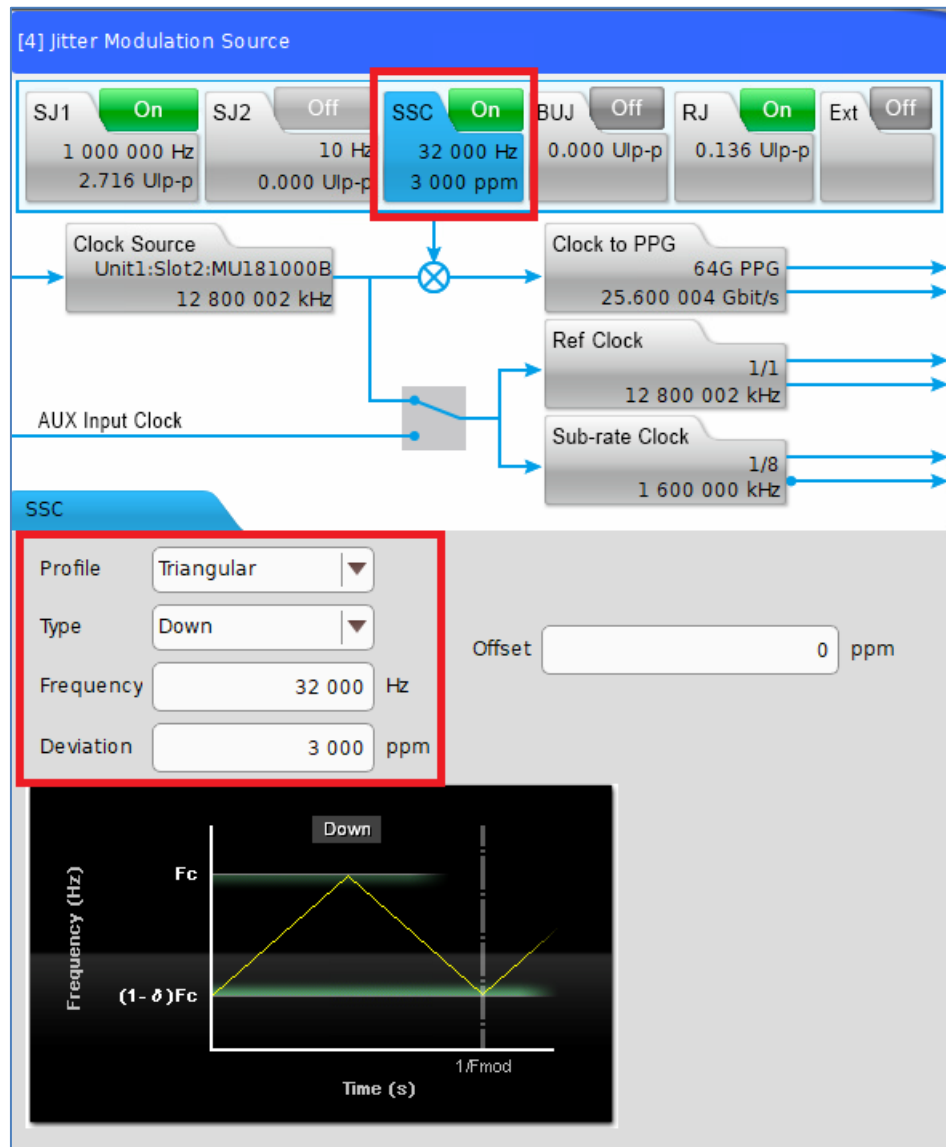


FIGURE 70. SSC SETTING FOR TEST CASE 2

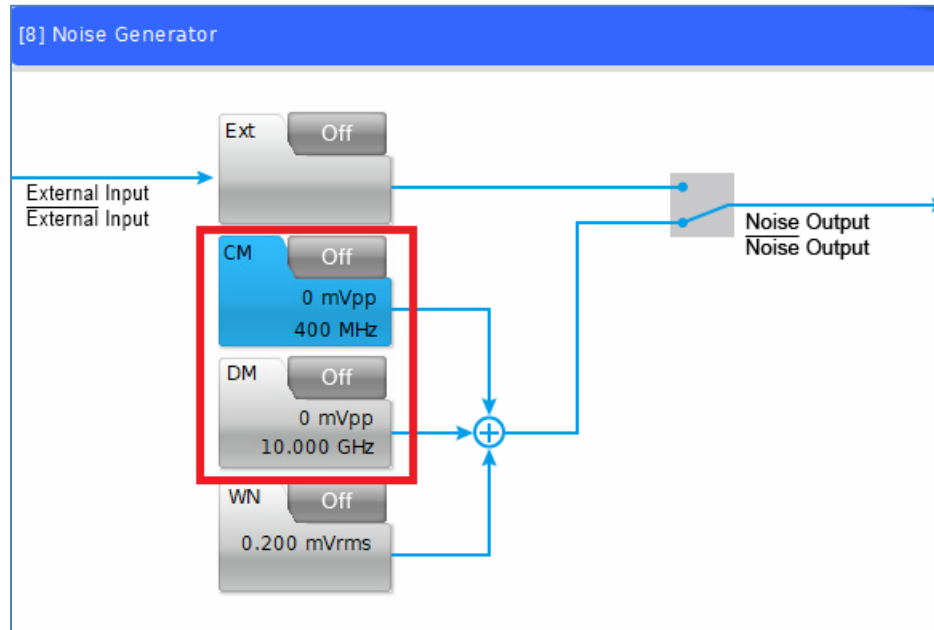


FIGURE 71. CM AND DM SETTING

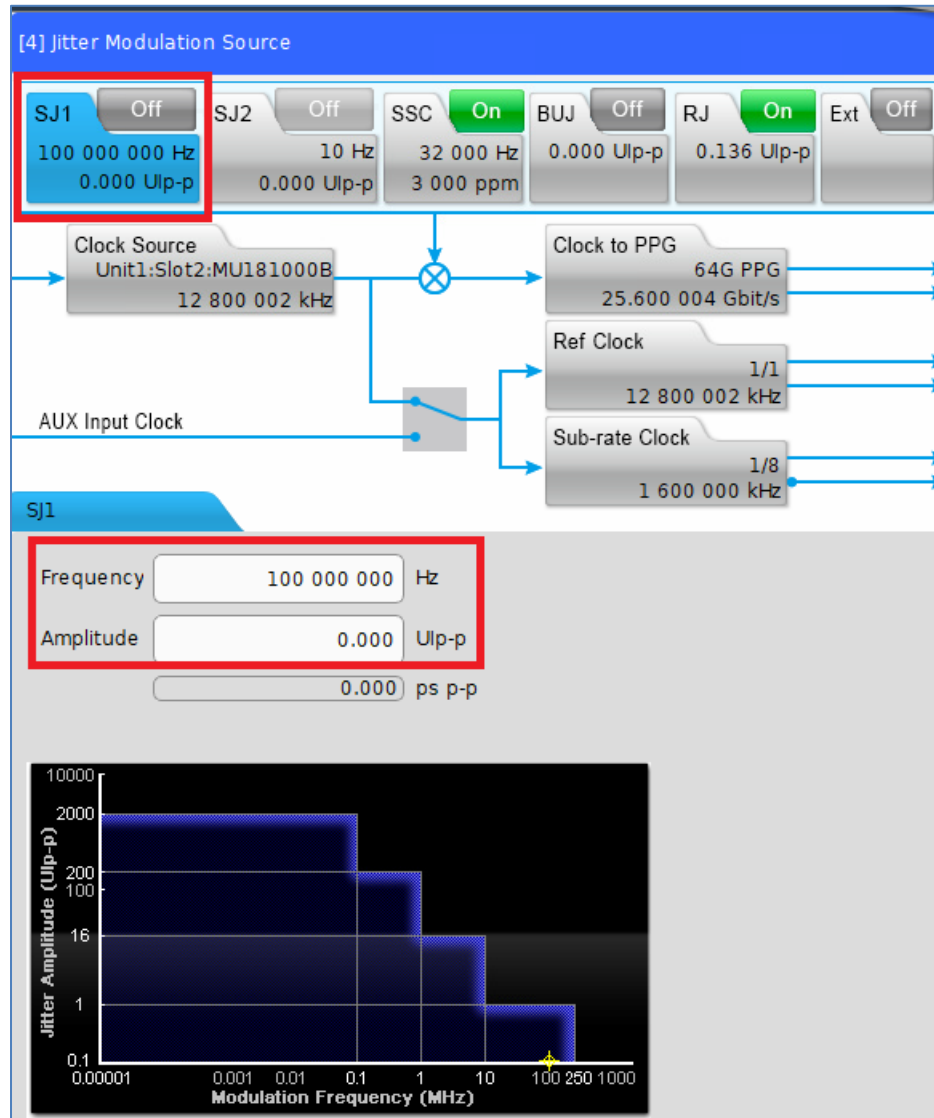


FIGURE 72. SJ1 SETTING

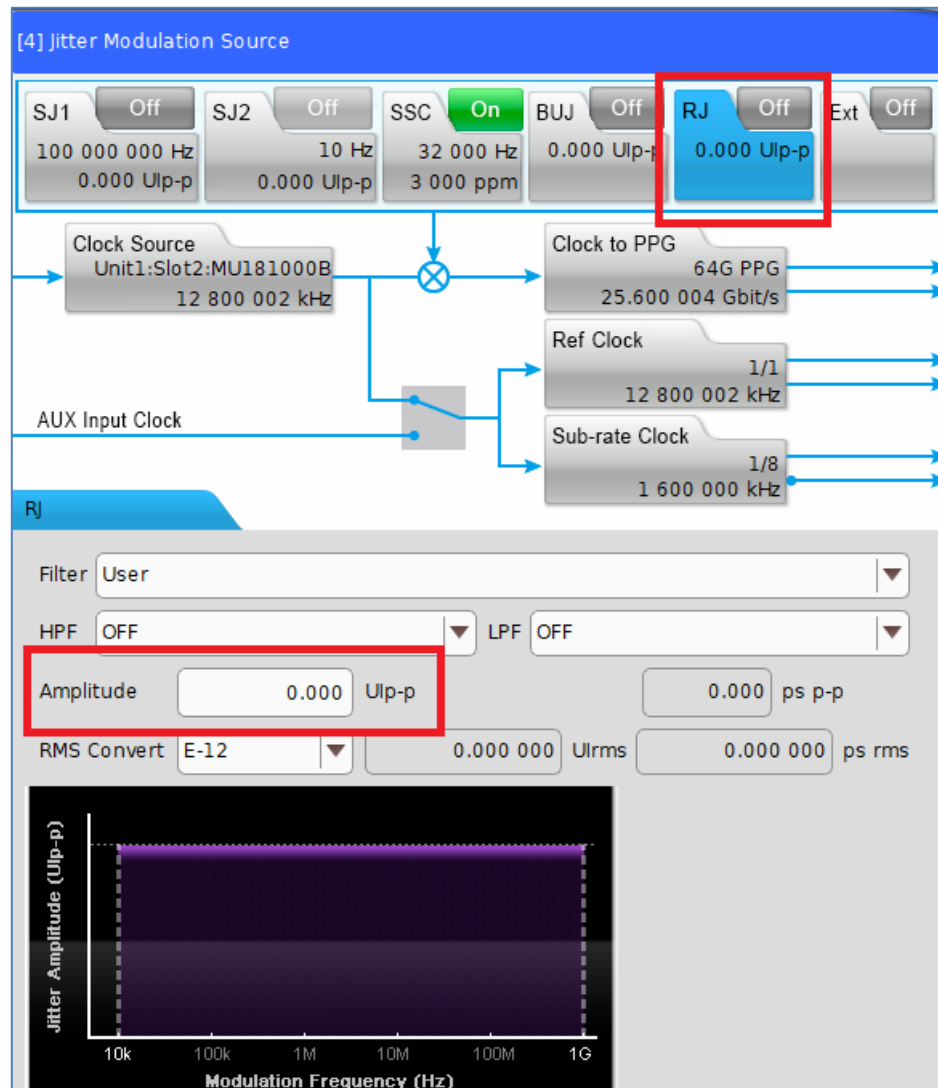


FIGURE 73. RJ SETTING

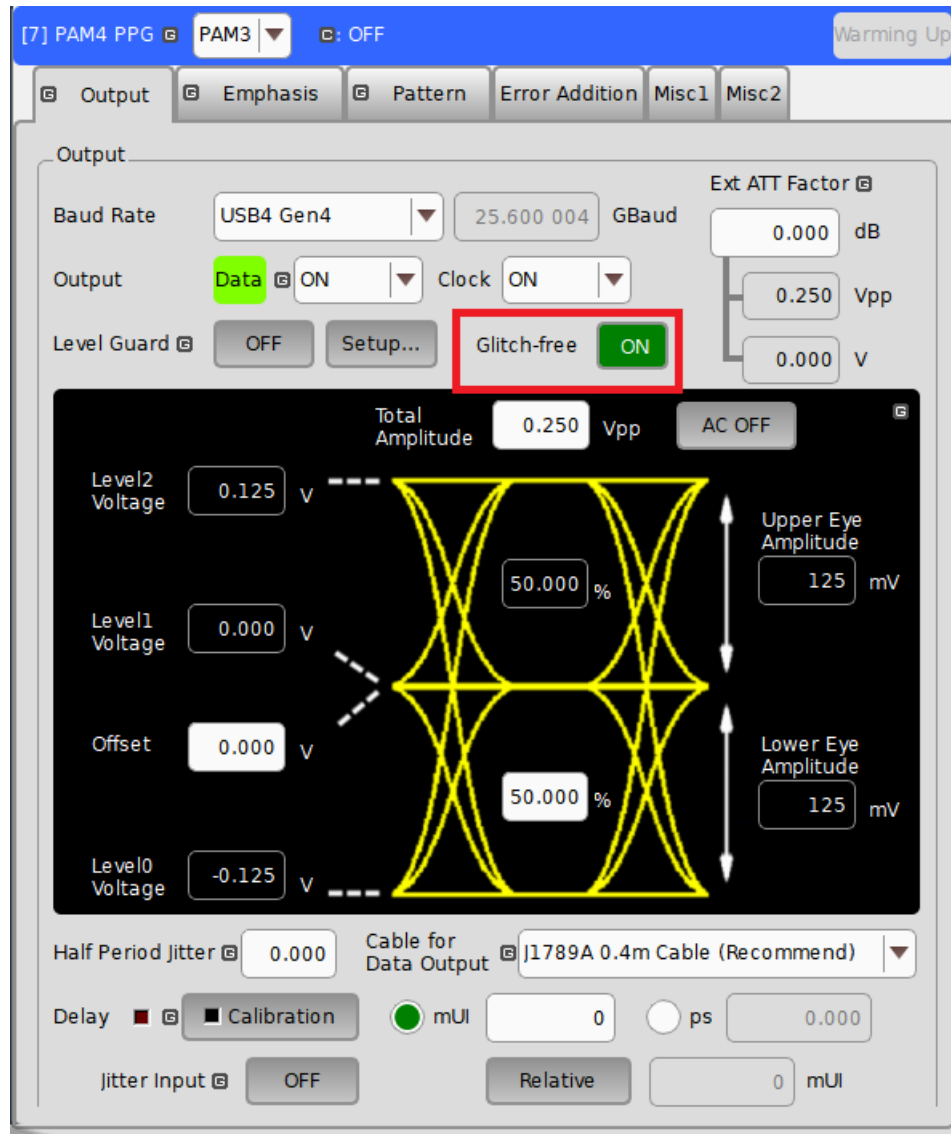


FIGURE 74. TURN ON GLITCH-FREE

9.8.2 Set Up Oscilloscope

9.8.2.1 Oscilloscope Vertical and Horizontal Setup for Waveform Capture

Set up the Scope as listed in Table 9.

TABLE 9. OSCILLOSCOPE VERTICAL AND HORIZONTAL SETUP

Setting	Setup
Vertical	Ch1-Ch3 (using the full range of the Scope's D/A)
Record Length	64M for Keysight UXR scope and 40M for other vendor scope in a single acquisition
Sample Rate	128 Gs/s for Keysight UXR scope and 80 Gs/s for other vendor scope
Averaging	OFF

Setting	Setup
Sample Mode	Real Time
Bandwidth	25GHz (which allows for 3 rd harmonic capture at 25.6GBaud/s)
Vertical Scale	Set to full screen without clipping
Sin x/x	OFF



FIGURE 75. OSCILLOSCOPE VERTICAL AND HORIZONTAL SETUP

9.8.2.2 Oscilloscope AC Common Mode (ACCM) Setup

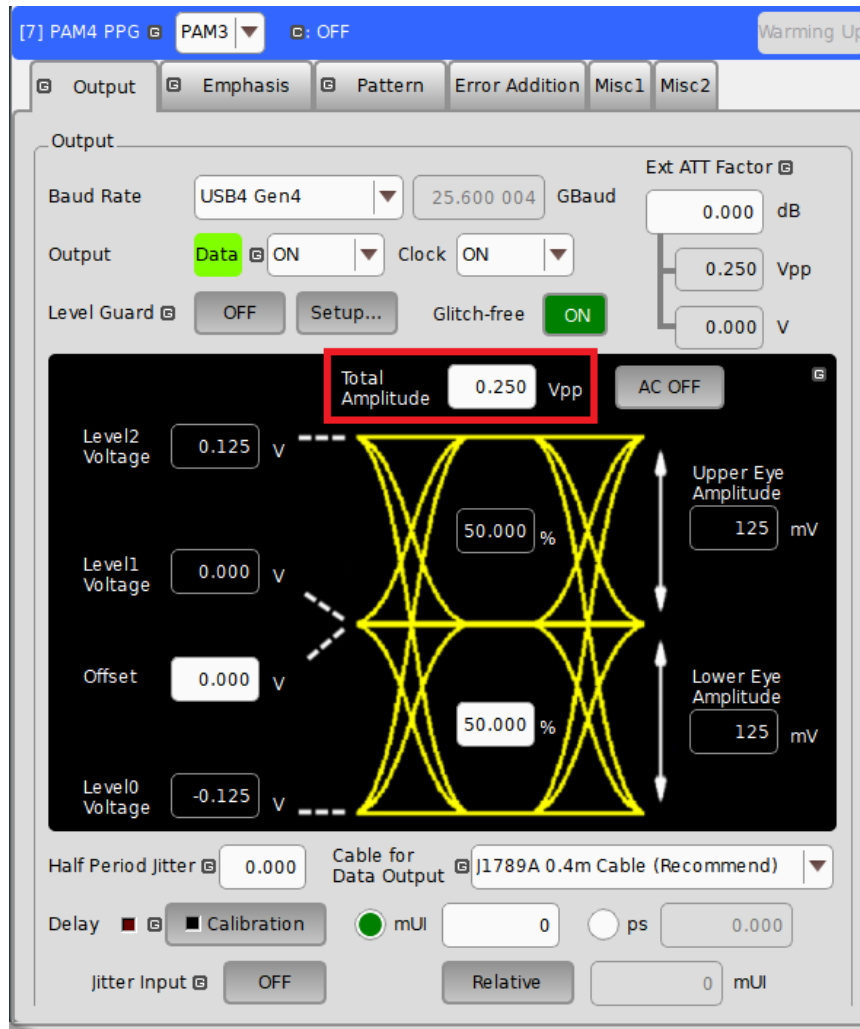
Set up the Scope as listed in Table 10.

TABLE 10. OSCILLOSCOPE ACCM SETUP

Setting	Setup
Sample Rate	128 Gs/s for Keysight UXR scope and 80 Gs/s for other vendor scope
Record Length	64M for Keysight UXR scope and 40M for other vendor scope in a single acquisition
Bandwidth	25GHz
Vertical Scale	Set to full screen without clipping
CDR	OFF
Averaging	OFF
Sin x/x	OFF

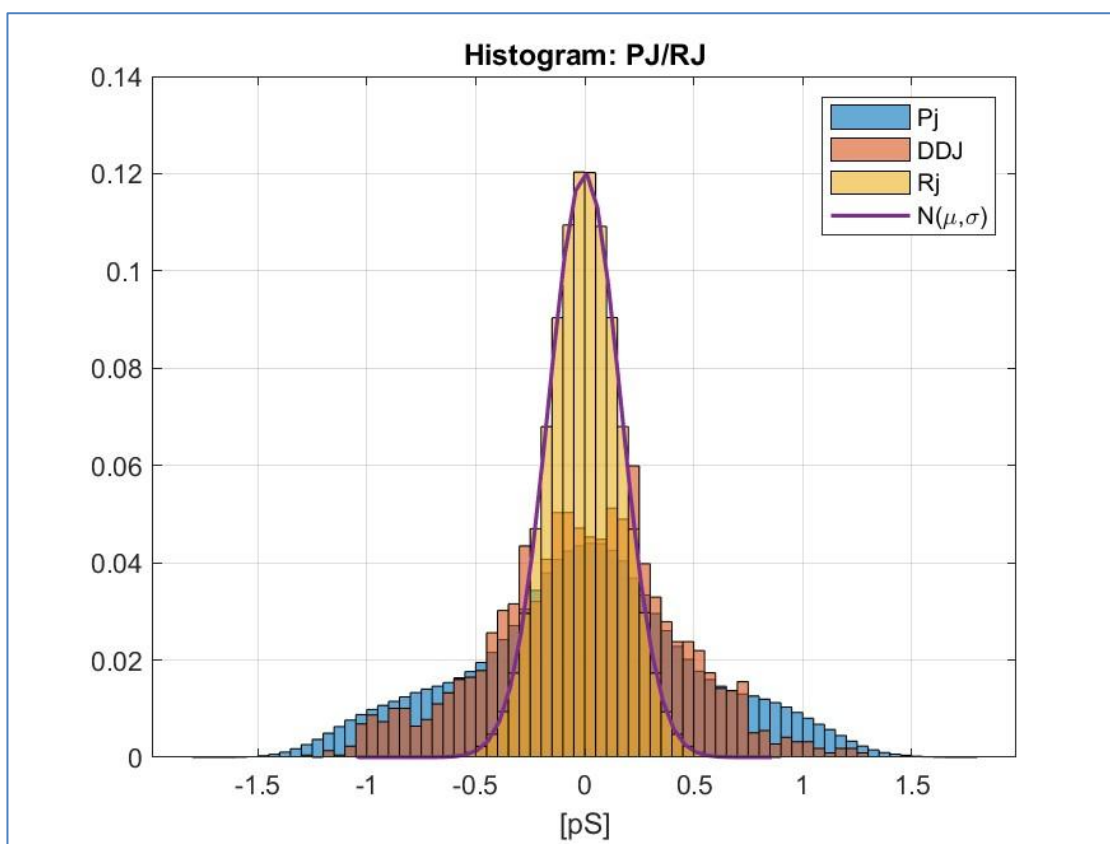
9.9 Voltage Swing Calibration for Case 2

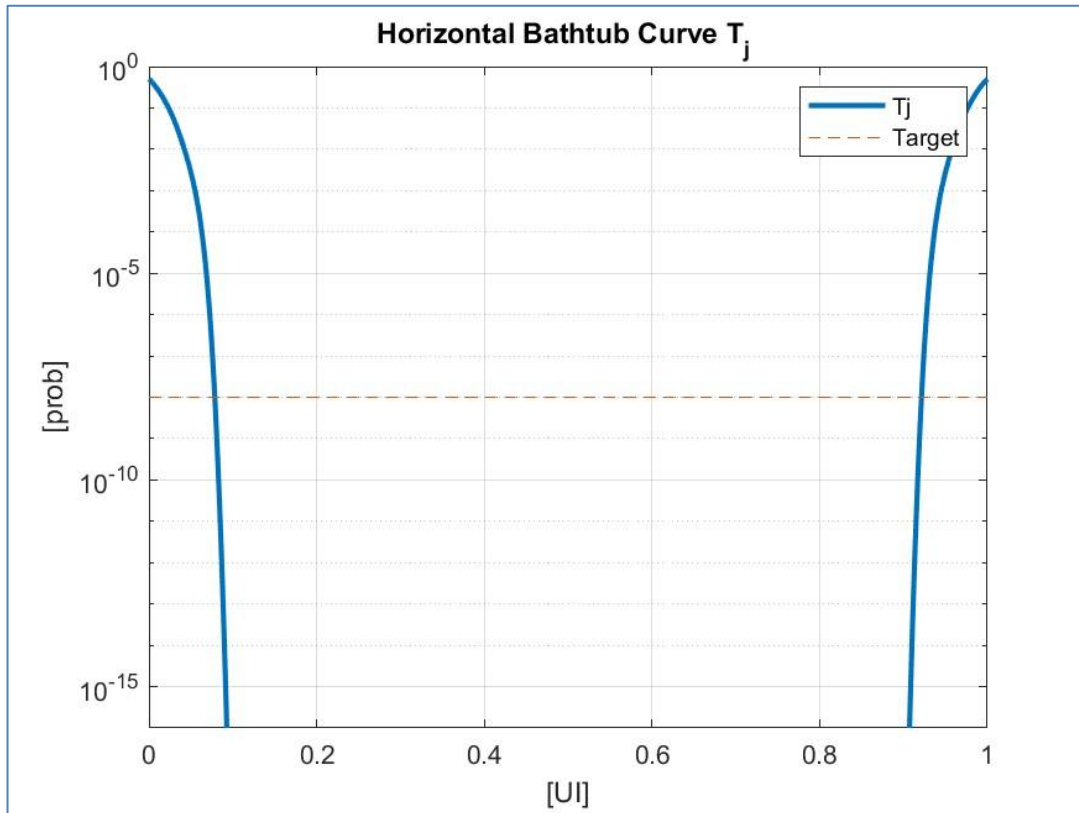
1. Turn off SJ1, RJ, DM and CM on the BERT.
2. Adjust the signal amplitude to achieve 820 mV.
3. Set up the scope so that Channel 1 and Channel 3 scale to 80% of screen.
4. Capture a single-ended pair of signal waveform on the scope.
5. Run the SigTest tool according to section 8.3.1 of the SigTest User Manual documentation.



6. For SigTest measurement, use the following template:
 - Test Point: tp3_prime
 - CTS Test Template: calibration
 - Command example:
`.\USB4_SigTest.exe gen4 rx tp3_prime calibration C:\SigTest\Waveforms\p_prt7_preset_0.bin n_prt7_preset_0.bin calibration_report none`
7. Retrieve Voltage Swing measurement.

Electrical Compliance Test Specification for GEN4			
Date:	7-Mar-24		
DIR:	C:\GRL\Rx Test Solution\Applications\USB4_V2_AN_RxTest\AppData\Waveforms\		
Files:	p_TempWaveform0_preset_0.bin n_TempWaveform0_preset_0.bin		
AC CM Measurement:	AC CM: Vac [mVp2p]	27.5	
PJ Jitter Measurement mUIp-p:	PJ-p-p	38.6214	
RJ Jitter Measurement mUIrms:	RJ-rms	3.578655	
Informative:	Symbol Rate [GHz]	25.56162	Drift [PPM] -1499.24
Vertical Analysis Test:			
TX_SNR Measurement [dB]:	TX_SNR [dB]	41.81246	
TX_LEVELS_MISMATCH Measurement:	TX_LEVELS_MISMATCH	0.980531	
V_SWING Measurement [mVp-p]:	V_SWING-p-p	833.8	

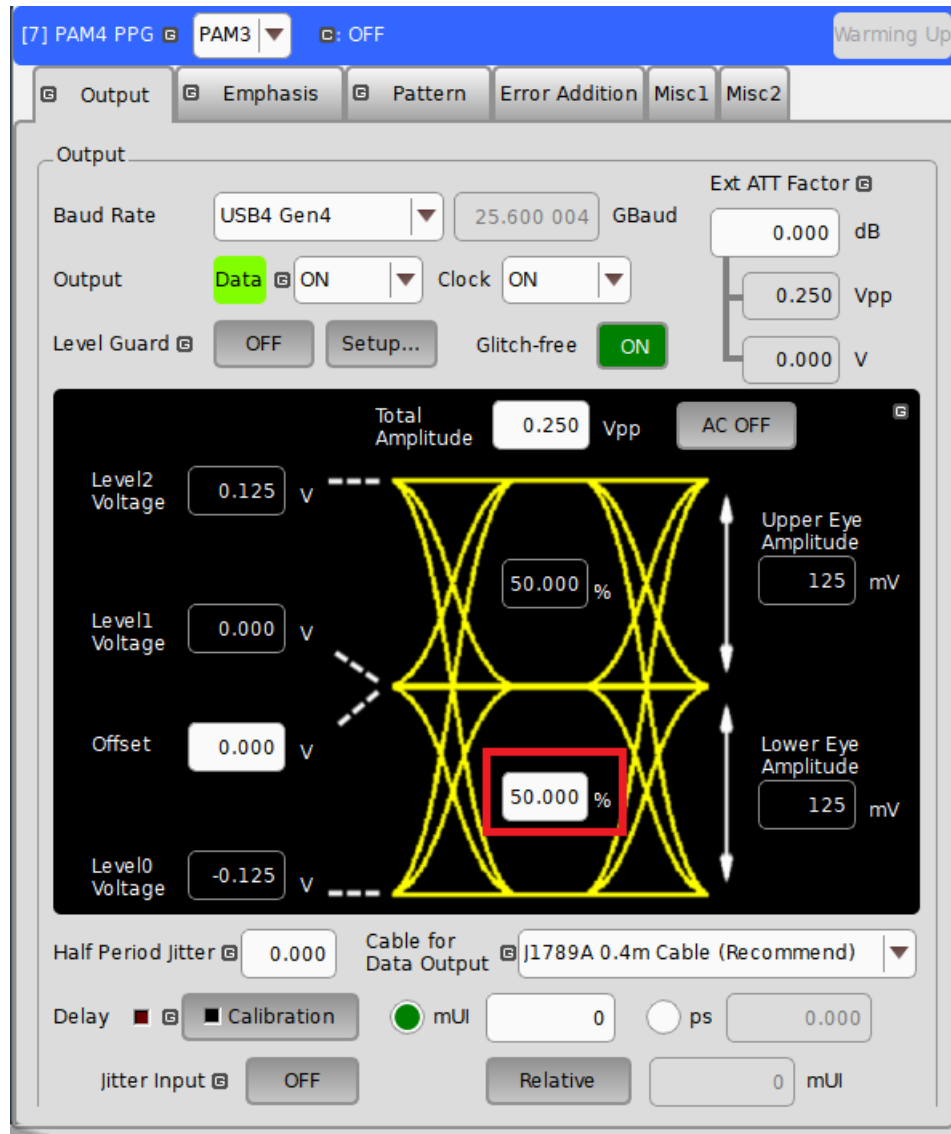




8. Adjust the BERT voltage swing setting and repeat steps 2-7 until the desired result is achieved.

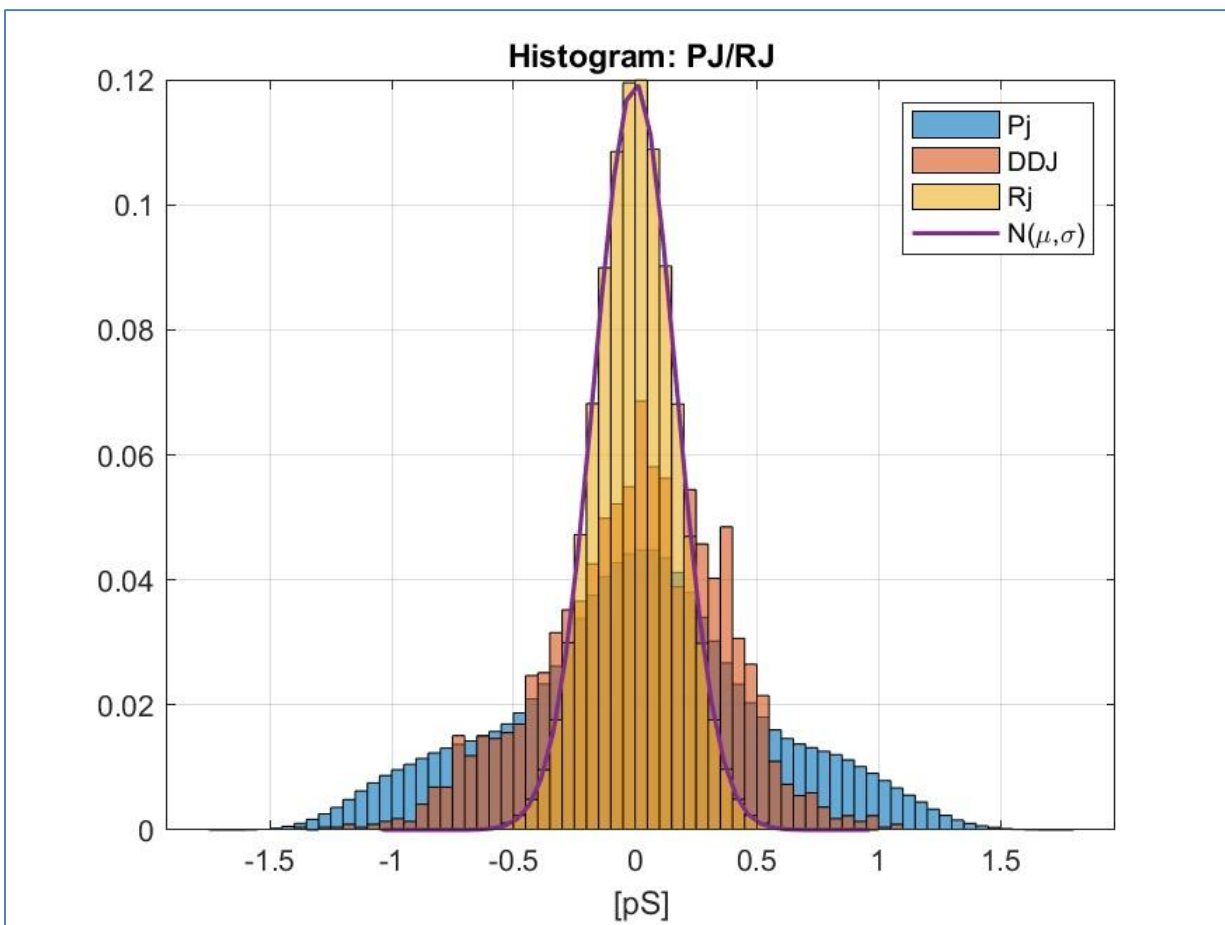
9.10 Level Mismatch Calibration for Case 2

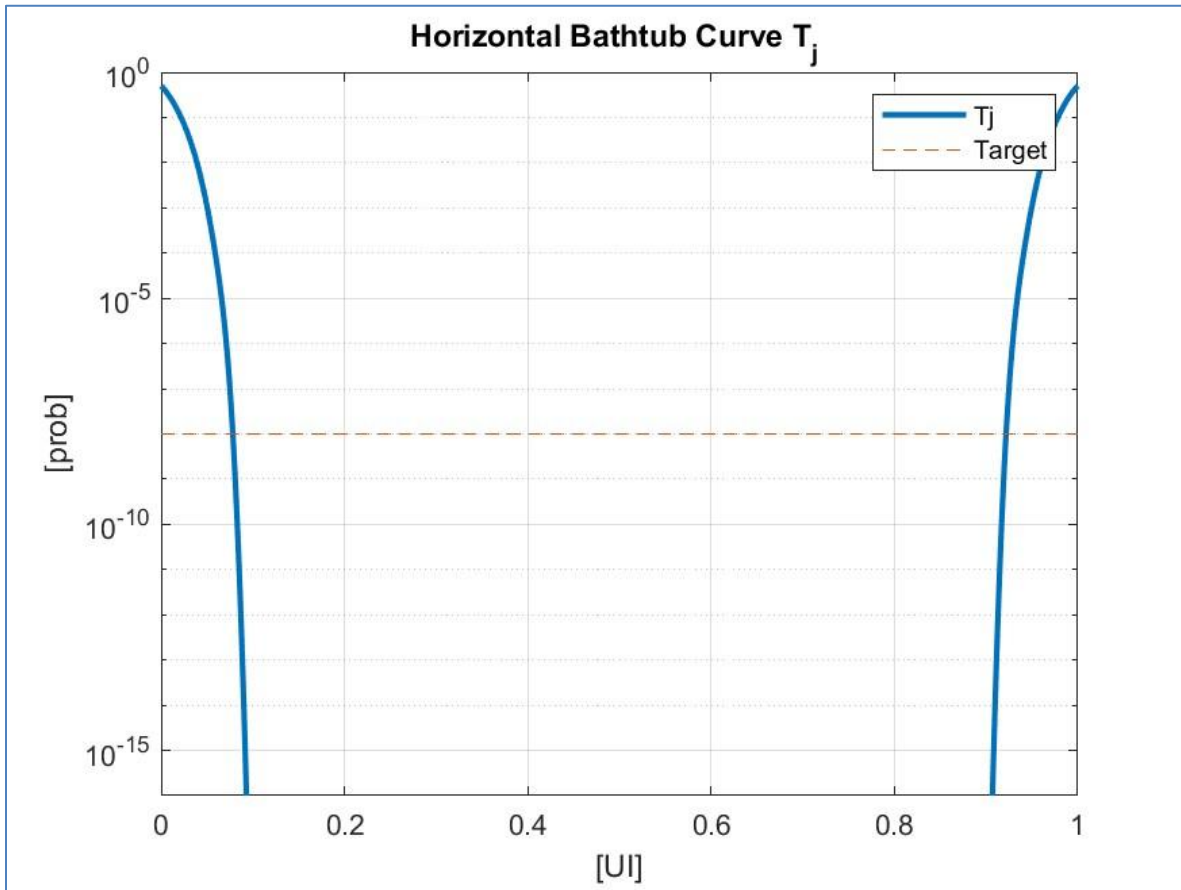
1. Keep Voltage Swing as calibrated in previous step.
2. Turn off SJ1, RJ, DM and CM on the BERT.
3. Adjust the Lower Eye Percentage on the BERT to achieve 0.975.
4. Capture a single-ended pair of signal waveform on the scope.



5. Run the SigTest tool according to section 8.3.1 of the SigTest User Manual documentation.
6. For SigTest measurement, use the following template:
 - Test Point: tp3_prime
 - CTS Test Template: calibration
 - Command example:
`.\USB4_SigTest.exe gen4 rx tp3_prime calibration C:\SigTest\Waveforms\p_prts7_preset_0.bin n_prts7_preset_0.bin calibration_report none`
7. Retrieve the Level Mismatch measurement.

Electrical Compliance Test Specification for GEN4			
Date:	7-Mar-24		
DIR:	C:\GRL\Rx Test Solution\Applications\USB4_V2_AN_RxTest\AppData\Waveforms\		
Files:	p_TempWaveform0_preset_0.bin	n_TempWaveform0_preset_0.bin	
AC CM Measurement:	AC CM: Vac [mVp2p]	27	
PJ Jitter Measurement mUIp-p:	PJ-p-p	38.38484	
RJ Jitter Measurement mUIrms:	RJ-rms	3.749269	
Informative:	Symbol Rate [GHz]	25.5616	Drift [PPM] -1499.97
Vertical Analysis Test:			
TX_SNR Measurement [dB]:	TX_SNR [dB]	41.48415	
TX_LEVELS_MISMATCH Measurement:	TX_LEVELS_MISMATCH	0.973955	
V_SWING Measurement [mVp-p]:	V_SWING-p-p	826.6	

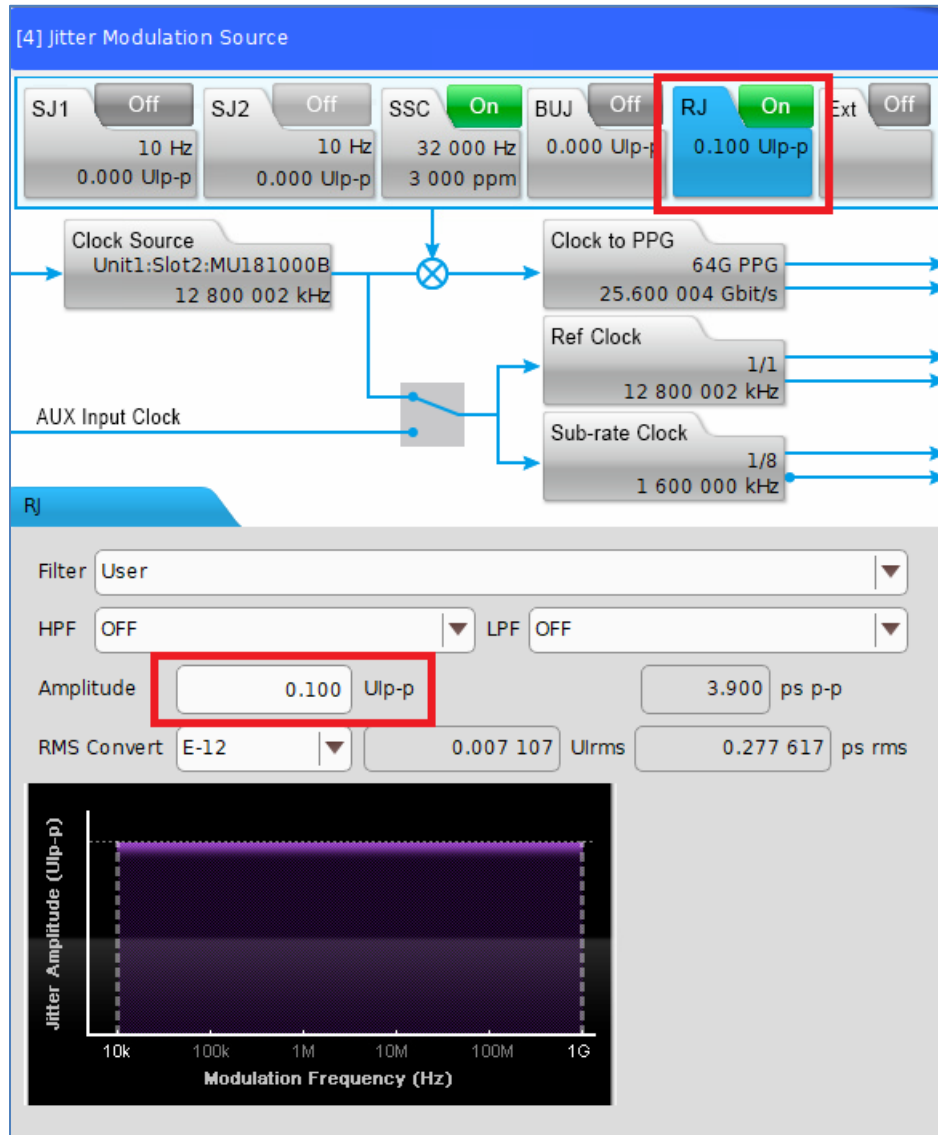




8. Adjust the BERT Level2 Voltage setting and repeat steps 3-7 until the desired result is achieved.

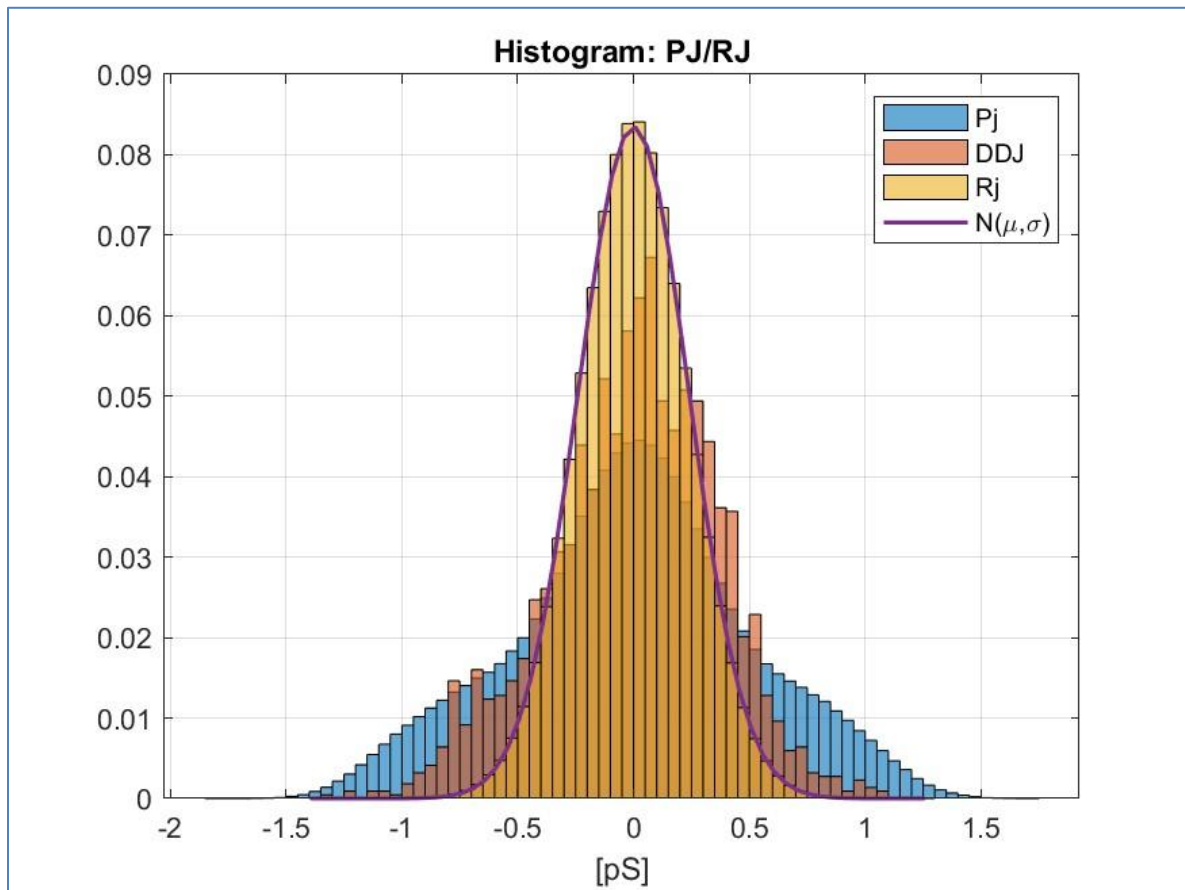
9.11 RJ Calibration for Case 2

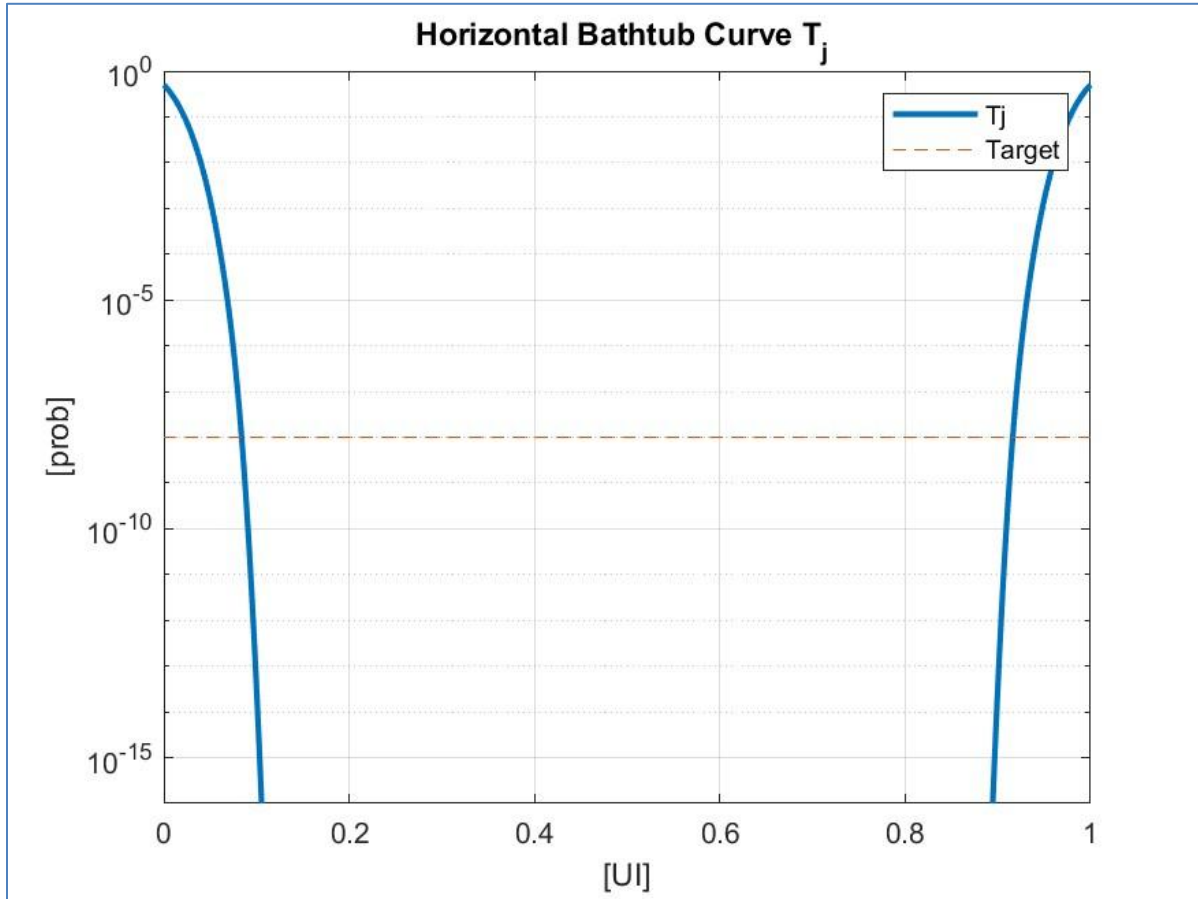
1. Keep the Voltage Swing and Level Mismatch as calibrated in the previous step.
2. Turn off SJ1, DM and CM on the BERT.
3. Adjust RJ on the BERT to achieve 0.0085 UIrms.
4. Capture a single-ended pair of signal waveform on the scope.



5. Run the SigTest tool according to section 8.3.1 of the SigTest User Manual documentation.
6. For SigTest measurement, use the following template:
 - Test Point: tp3_prime
 - CTS Test Template: calibration
 - Command example:
`.\USB4_SigTest.exe gen4 rx tp3_prime calibration C:\SigTest\Waveforms\p_prts7_preset_0.bin n_prts7_preset_0.bin calibration_report none`
7. Retrieve the RJ measurement.
8. Adjust the BERT RJ setting and repeat steps 3-7 until the desired result is achieved.

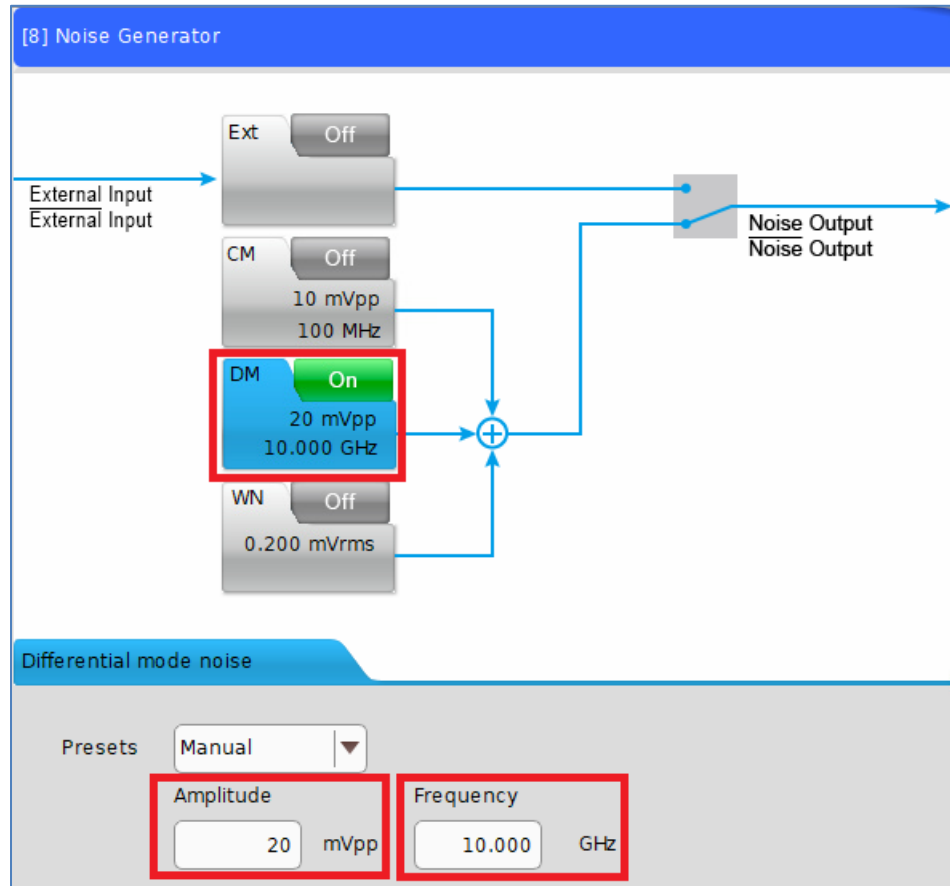
Electrical Compliance Test Specification for GEN4			
Date:	7-Mar-24		
DIR:	C:\GRL\Rx Test Solution\Applications\USB4_V2_AN_RxTest\AppData\Waveforms\		
Files:	p_TempWaveform0_preset_0.bin	n_TempWaveform0_preset_0.bin	
AC CM Measurement:	AC CM: Vac [mVp2p]	27.5	
PJ Jitter Measurement mUIp-p:	PJ-p-p	37.40819	
RJ Jitter Measurement mUIrms:	RJ-rms	8.475799	
Informative:	Symbol Rate [GHz]	25.5616	Drift [PPM] -1500.02
Vertical Analysis Test:			
TX_SNR Measurement [dB]:	TX_SNR [dB]	41.42645	
TX_LEVELS_MISMATCH Measurement:	TX_LEVELS_MISMATCH	0.973981	
V_SWING Measurement [mVp-p]:	V_SWING-p-p	826.4	





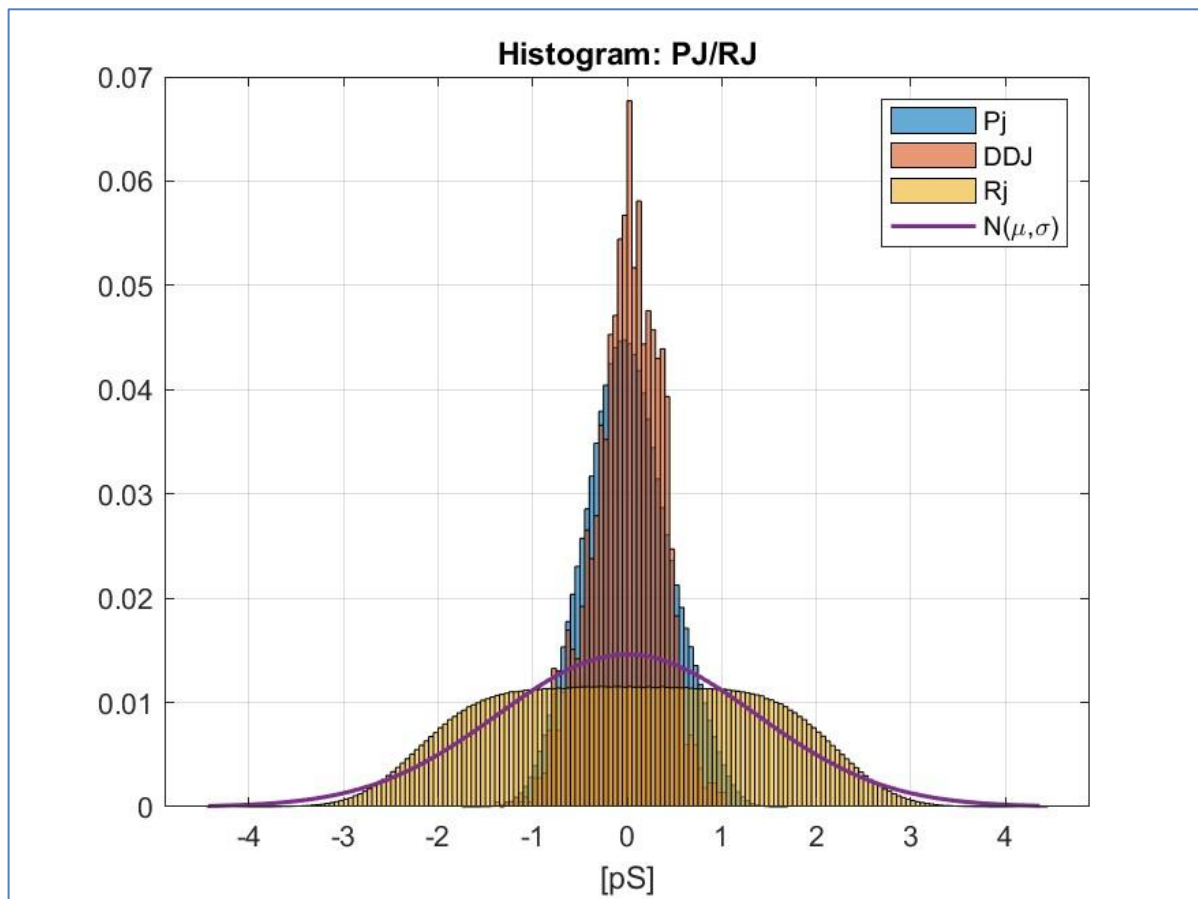
9.12 SNDR Calibration for Case 2

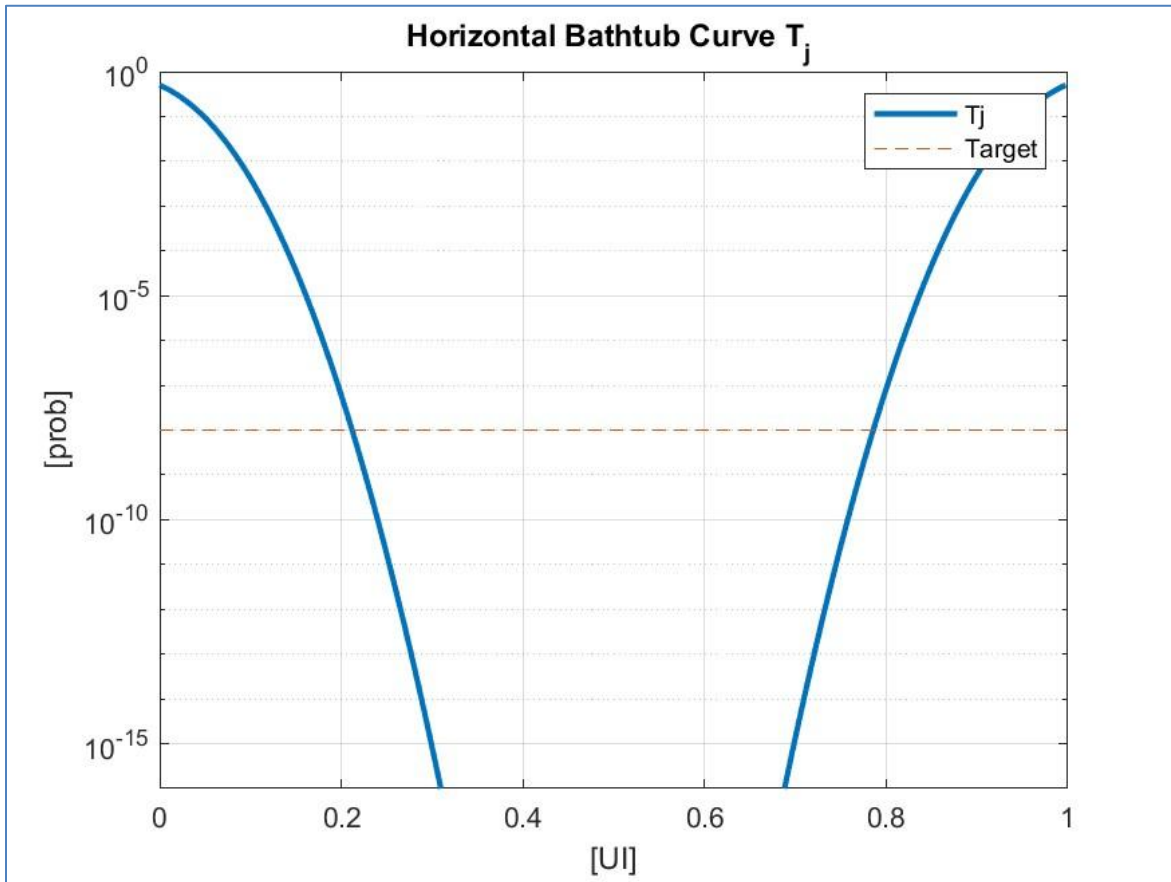
1. Keep the Voltage Swing, Level Mismatch and RJ as calibrated in the previous step.
2. Turn off SJ1 and CM on the BERT.
3. Set the DM frequency setting on the BERT to 10 GHz.
4. Adjust the DM amplitude to achieve 32.5 dB.



5. Run the SigTest tool according to section 8.3.1 of the SigTest User Manual documentation.
6. For SigTest measurement, use the following template:
 - Test Point: tp3_prime
 - CTS Test Template: calibration
 - Command example:
`.\USB4_SigTest.exe gen4 rx tp3_prime calibration C:\SigTest\Waveforms\p_prt7_preset_0.bin n_prt7_preset_0.bin calibration_report none`
7. Retrieve the SNDR measurement.
8. Adjust the BERT DM amplitude setting and repeat steps 4-7 until the desired result is achieved.

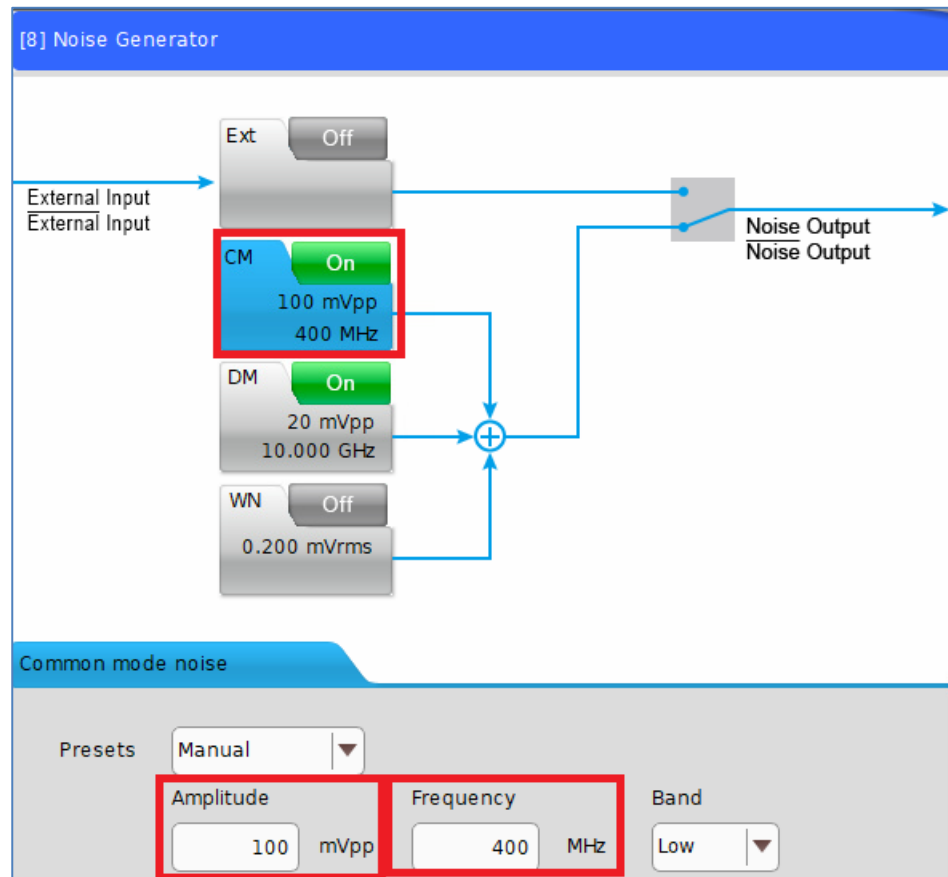
Electrical Compliance Test Specification for GEN4				
Date:	7-Mar-24			
DIR:	C:\GRL\Rx Test Solution\Applications\USB4_V2_AN_RxTest\AppData\Waveforms\			
Files:	p_TempWaveform0_preset_0.bin	n_TempWaveform0_preset_0.bin		
AC CM Measurement:	AC CM: Vac [mVp2p]	27.9		
PJ Jitter Measurement mUIp-p:	PJ-p-p	37.37844		
RJ Jitter Measurement mUIrms:	RJ-rms	10.02875		
Informative:	Symbol Rate [GHz]	25.56162	Drift [PPM]	-1499.42
Vertical Analysis Test:				
TX_SNR Measurement [dB]:	TX_SNR [dB]	33.23645		
TX_LEVELS_MISMATCH Measurement:	TX_LEVELS_MISMATCH	0.973983		
V_SWING Measurement [mVp-p]:	V_SWING-p-p	828.4		





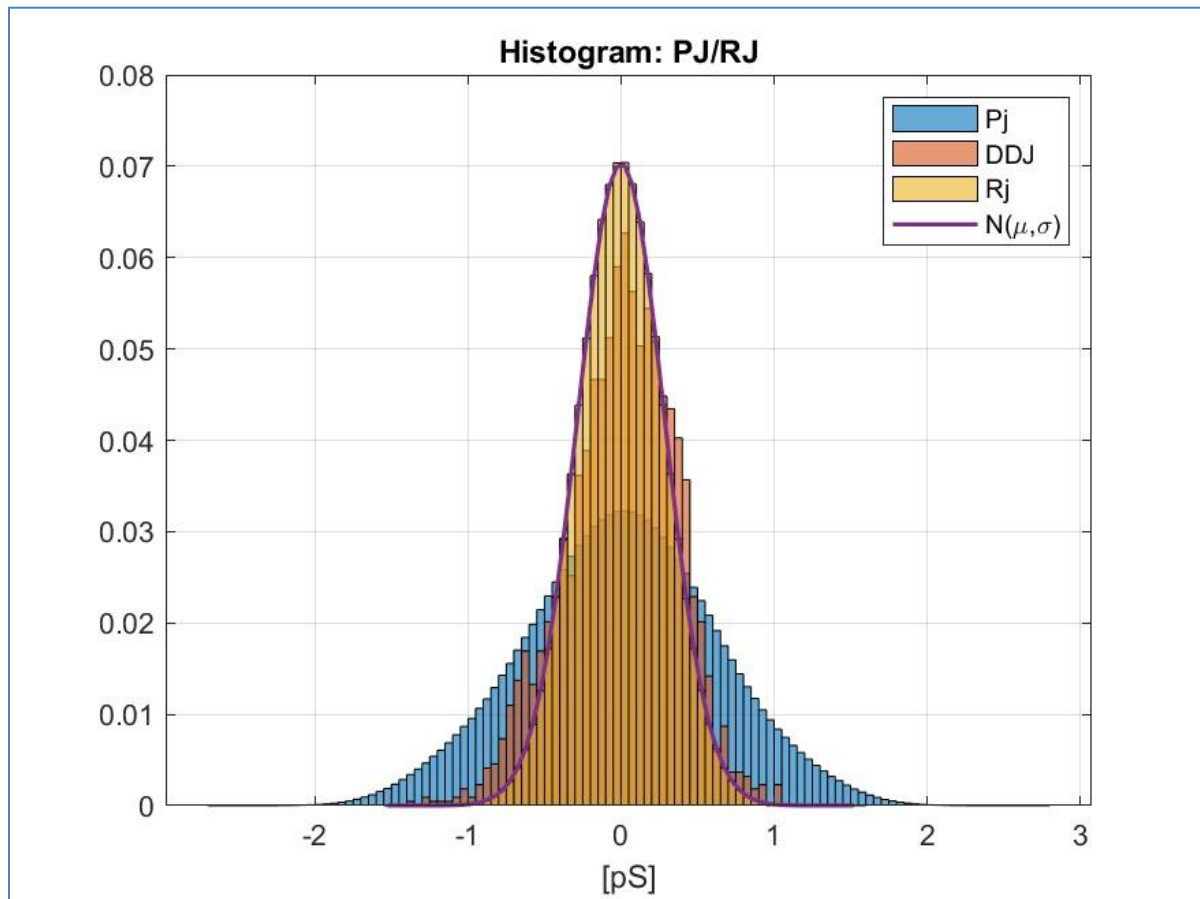
9.13 ACCM Calibration for Case 2

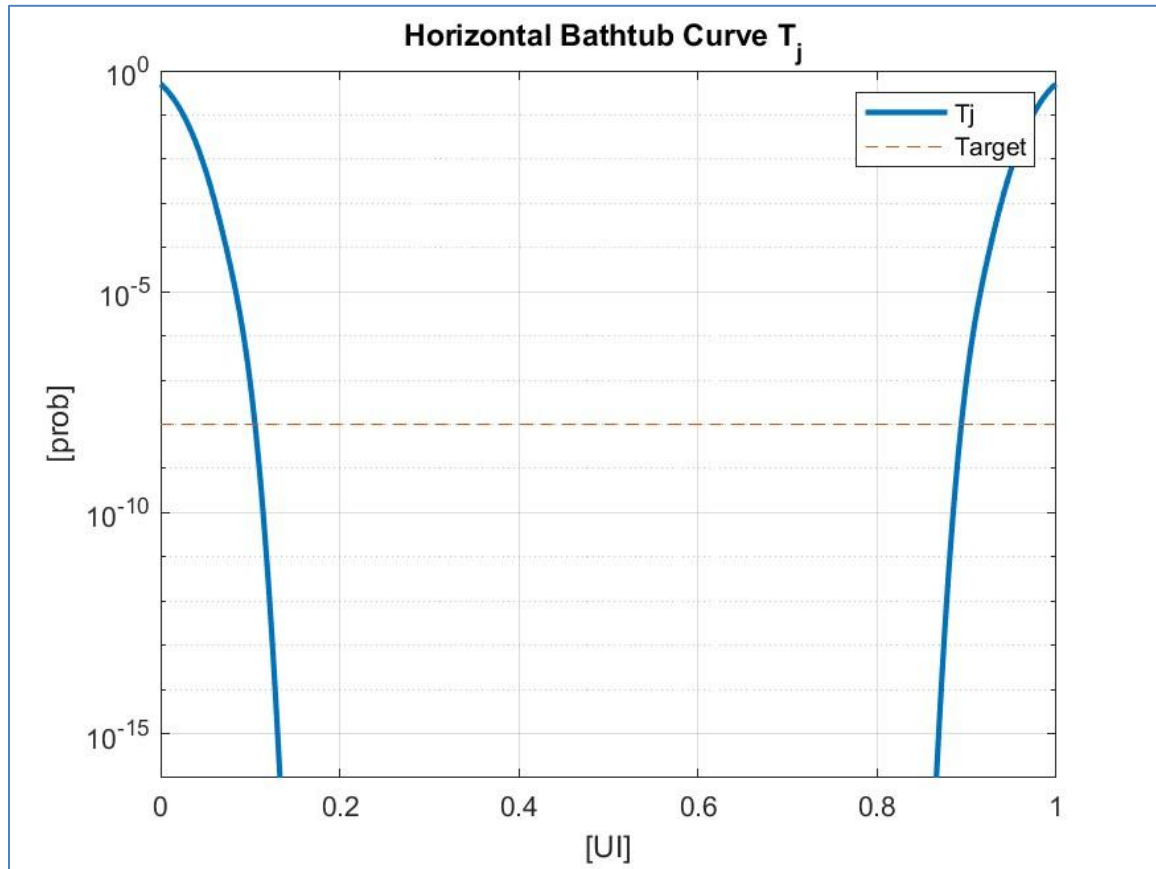
1. Keep the Voltage Swing, Level Mismatch, RJ and SNDR as calibrated in the previous step.
2. Turn off SJ on the BERT.
3. Set the CM frequency setting on the BERT to 400 MHz.
4. Adjust the CM amplitude to achieve 100 mV.



5. Run the SigTest tool according to section 8.3.1 of the SigTest User Manual documentation.
6. For SigTest measurement, use the following template:
 - Test Point: tp3_prime
 - CTS Test Template: calibration
 - Command example:
`.\USB4_SigTest.exe gen4 rx tp3_prime calibration C:\SigTest\Waveforms\p_prts7_preset_0.bin n_prts7_preset_0.bin calibration_report none`
7. Retrieve the ACCM measurement.
8. Adjust the BERT CM amplitude setting and repeat steps 4-7 until the desired result is achieved.

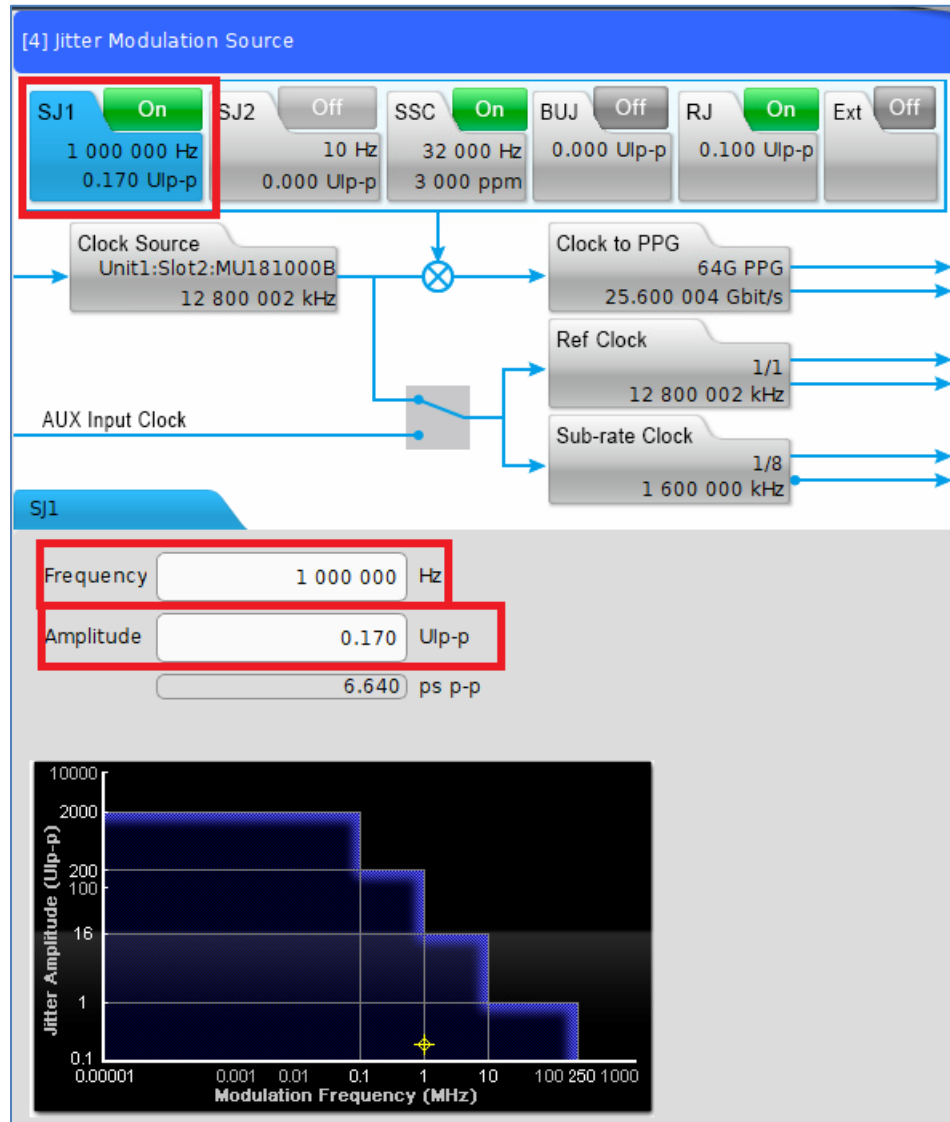
Electrical Compliance Test Specification for GEN4			
Date:	7-Mar-24		
DIR:	C:\GRL\Rx Test Solution\Applications\USB4_V2_AN_RxTest\AppData\Waveforms\		
Files:	p_TempWaveform0_preset_0.bin	n_TempWaveform0_preset_0.bin	
AC CM Measurement:	AC CM: Vac [mVp2p]	106.7	
PJ Jitter Measurement mUIp-p:	PJ-p-p	45.52237	
RJ Jitter Measurement mUIrms:	RJ-rms	6.964004	
Informative:	Symbol Rate [GHz]	25.56162	Drift [PPM] -1499.25
Vertical Analysis Test:			
TX_SNR Measurement [dB]:	TX_SNR [dB]	28.3622	
TX_LEVELS_MISMATCH Measurement:	TX_LEVELS_MISMATCH	0.973946	
V_SWING Measurement [mVp-p]:	V_SWING-p-p	827.3	





9.14 PJ Calibration for Case 2

1. Keep the Voltage Swing, Level Mismatch, RJ, SNDR and ACCM as calibrated in the previous step.
2. Set the SJ1 frequency setting on the BERT to 1 MHz.
3. Adjust the SJ1 amplitude to achieve 0.075 UIpp.
4. Run the SigTest tool according to section 8.3.1 of the SigTest User Manual documentation.

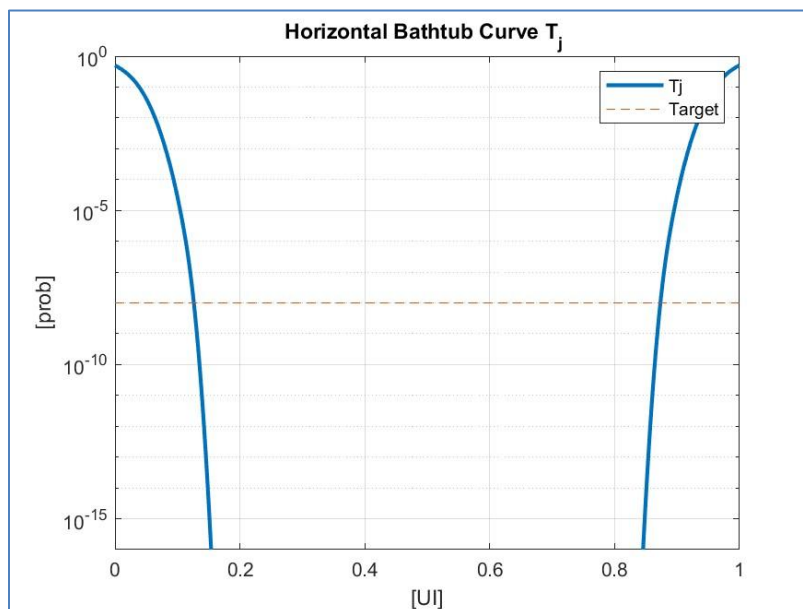
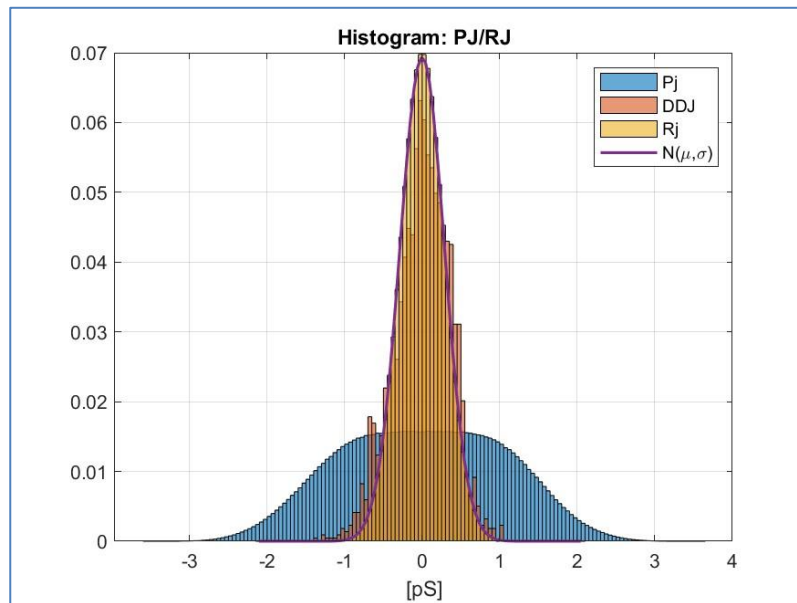


5. For SigTest measurement, use the following template:

- Test Point: tp3_prime
- CTS Test Template: calibration
- Command example:
`.\USB4_SigTest.exe gen4 rx tp3_prime calibration C:\SigTest\Waveforms\p_prts7_preset_0.bin n_prts7_preset_0.bin calibration_report none`

6. Retrieve the PJ measurement.

Electrical Compliance Test Specification for GEN4			
Date:	7-Mar-24		
DIR:	C:\GRL\Rx Test Solution\Applications\USB4_V2_AN_RxTest\AppData\Waveforms\		
Files:	p_TempWaveform0_preset_0.bin	n_TempWaveform0_preset_0.bin	
AC CM Measurement:	AC CM: Vac [mVp2p]	106.4	
PJ Jitter Measurement mUIp-p:	PJ-p-p	75.95034	
RJ Jitter Measurement mUIrms:	RJ-rms	7.051537	
Informative:	Symbol Rate [GHz]	25.5616	Drift [PPM] -1499.92
Vertical Analysis Test:			
TX_SNR Measurement [dB]:	TX_SNR [dB]	28.20769	
TX_LEVELS_MISMATCH Measurement:	TX_LEVELS_MISMATCH	0.973865	
V_SWING Measurement [mVp-p]:	V_SWING-p-p	828.1	



- Adjust the BERT SJ1 amplitude setting and repeat steps 3-7 until the desired result is achieved.

8. Repeat steps 2-7 for the remaining PJ frequencies (2 MHz, 10 MHz, 50 MHz, 100 MHz).
9. Save the BERT setup as Test Case 2 for each PJ frequency.

9.15 BERT Model Extraction for Case 2

Extract the BERT assembly model by measuring:

- a. Differential Return Loss measured at the BERT assembly output.
- b. Differential Insertion Loss of the BERT assembly extracted by measuring step response at its output.

Set up the network analyzer as listed in Table 11.

TABLE 11. NETWORK ANALYZER SETUP

Setting	Setup
Standard Class	Single Ended
Frequency Range	10 MHz to 20 GHz
IF Bandwidth	1 KHz
Points	At least 2000 points
S-Parameter File Mode	Single Ended
4-Port System Port Mapping	1 -> 2, 3 -> 4

9.15.1 Differential Return Loss Measurement at BERT Assembly Output

1. Calibrate the Network Analyzer and test cables using a proper calibration kit.
2. Connect the test setup as shown in Figure 76 below.
3. Configure the BERT to transmit PAM2 SQ256 (128 Level2 and 128 Level0) with Swing of 800mV pp.
 - SQ256 pattern file location on the BERT: "C:\UserPatterns\Anritsu USB4 V2 Rx Test\SQ256.ptn"
4. Turn off all impairments (RJ, PJ, Differential Interference, Level Mismatch, SSC).
5. Capture and save the S-parameter to a file in the s2p format as "BERT_Sdd22.s2p" on the network analyzer. (It will be used later on in the Link Operating Margin Evaluation stages.)

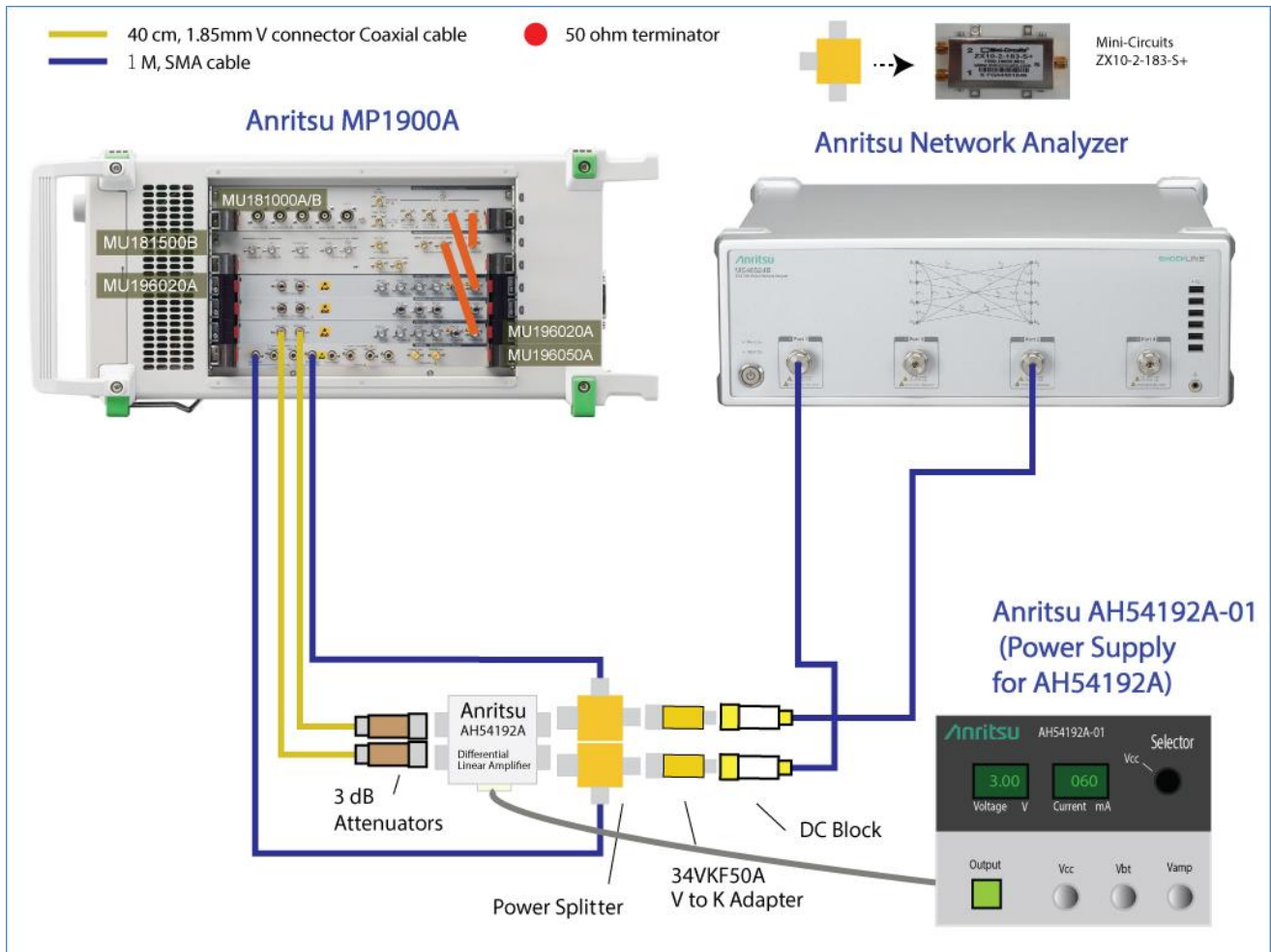
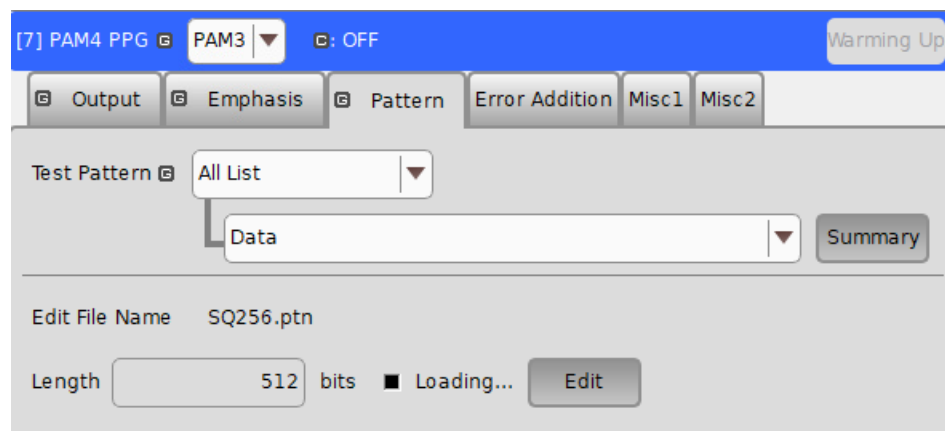


FIGURE 76. TEST SETUP FOR BERT ASSEMBLY RETURN LOSS EXTRACTION



9.15.2 BERT Assembly Step Response Extraction

Set up the oscilloscope as listed in Table 12 below.

TABLE 12. OSCILLOSCOPE SETUP FOR BERT ASSEMBLY STEP RESPONSE EXTRACTION

Setting	Setup
Sample Rate	128 Gs/s for Keysight UXR scope and 80 Gs/s for other vendor scope
Record Length	64M for Keysight UXR scope and 40M for other vendor scope in a single acquisition
Bandwidth	25GHz
Vertical Scale	Set to full screen without clipping
CDR	OFF
Averaging	OFF
Sin x/x	OFF

1. Connect the test setup as shown in Figure 77 below.
2. Configure the BERT to transmit PAM2 SQ256 (128 Level2 and 128 Level0) with Swing of 800mV pp.
 - SQ256 pattern file location on the BERT: “C:\UserPatterns\Anritsu USB4 V2 Rx Test\SQ256.ptn”
3. Turn off all impairments (RJ, PJ, Differential Interference, Level Mismatch, SSC).
4. Capture the differential output signal waveform and save it to a file as “BERT_Sdd21.[scope format]”. (It will be used later on in the Differential Insertion Loss of the BERT assembly extraction and Link Operating Margin Evaluation stages.)

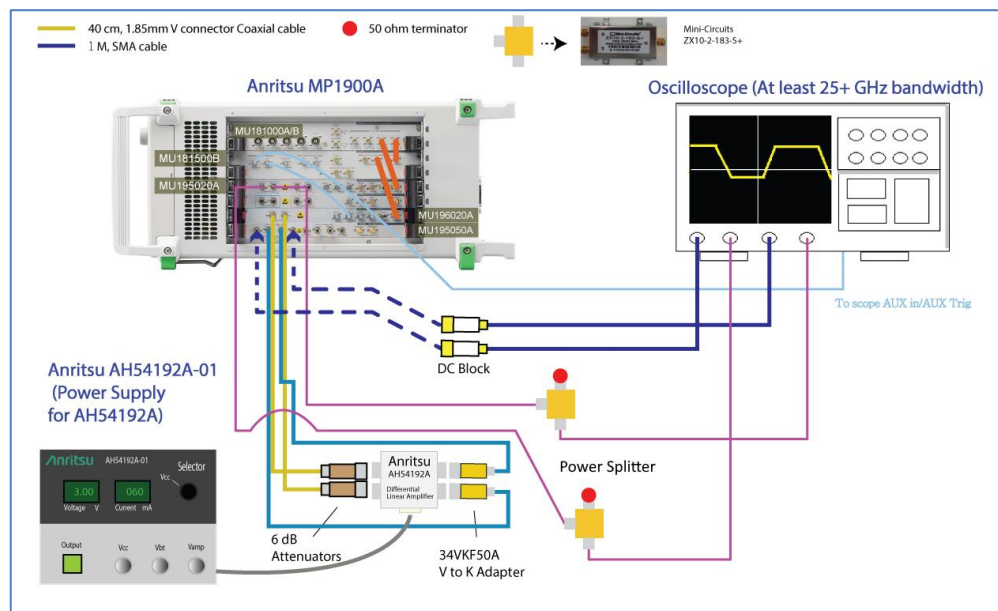


FIGURE 77. TEST SETUP FOR BERT ASSEMBLY STEP RESPONSE EXTRACTION

9.15.3 Differential Insertion Loss of the BERT Assembly Extraction

1. Run the SigTest tool according to section 8.3.2 of the SigTest User Manual documentation.
 - Input file is 'BERT_Sdd21.[scope format]' captured in Section 9.15.2.
2. Acquire the BERT assembly insertion loss (**BERT_IL**) @ 12.8dB result from SigTest. *[Note: This will be used in the next section.]*
3. For SigTest measurement, use the following template:
 - Test Point: tp3
 - CTS Test Template: calibration_bert_il_extraction
 - Command example:

```
. \USB4_SigTest.exe gen4 rx tp3 calibration_bert_il_extraction
C:\SigTest\Waveforms\ BERT_Sdd21.bin none bert_il_extraction.csv none
```

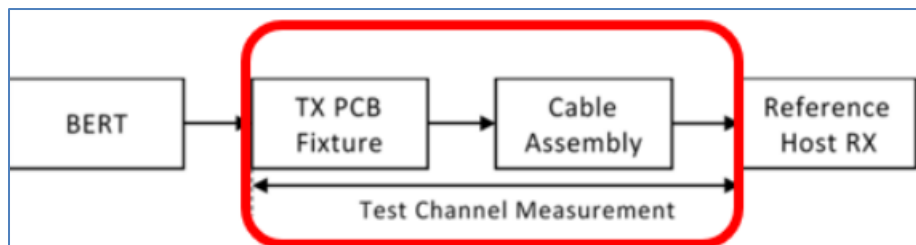
9.15.4 Test Channel Measurement

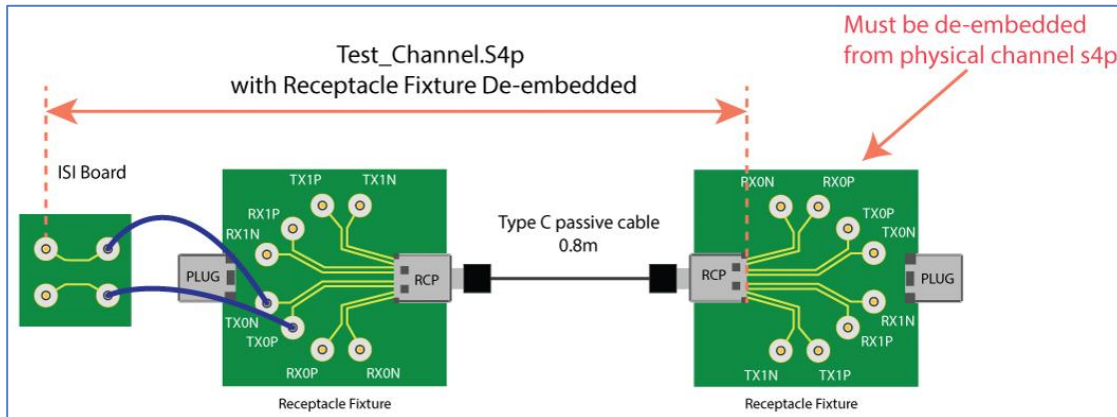
Set up the network analyzer as listed in Table 13 below.

TABLE 13. NETWORK ANALYZER SETUP FOR TEST CHANNEL MEASUREMENT

Setting	Setup
Standard Class	Differential
Frequency Range	10 MHz to 20 GHz
IF Bandwidth	1 kHz
Points	At least 2000 points
S-Parameter File Mode	Differential
4-Port System Port Mapping	1 -> 2, 3 -> 4

1. Measure the S-parameters of the Test channel defined by the Tx PCB fixture and cable assembly.

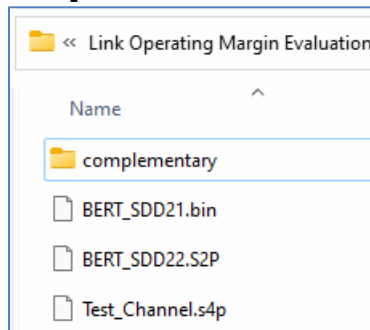




2. The test channel with receptacle fixture de-embedded insertion loss target should be $(-19\text{dB} - \text{BERT_IL}) @ 12.8\text{GHz} \pm 0.5\text{dB}$.
3. If the Insertion Loss target is not achieved, adjust the PCB fixture Insertion Loss.
4. If the Insertion Loss target is achieved, save the test channel with receptacle fixture trace de-embedded S-parameters to a file in the s4p format as “Test_Channel.s4p” (it will be used later on in the link operating margin evaluation stage).

9.15.5 Link operating margin evaluation

1. For SigTest measurement, use the following template:
 - Test Point: tp3
 - CTS Test Template: calibration
 - Command example:
`.\USB4_SigTest.exe gen4 rx tp3 calibration C:\SigTest\Waveforms\ BERT_Sdd21.bin none channel_calibration_to_worst_case_condition_result_result.csv none none`
2. Run the SigTest tool according to section 8.3.2 of the SigTest User Manual documentation.
 - Input files are as follows:
 - Test_Channel.s4p
 - BERT_Sdd22.s2p
 - BERT_Sdd21.[scope format]



- ‘complementary’ folder and other files can be found in the SigTest package
- Output parameters are as follows:
 - The extracted end-to-end channel ILfit at Nyquist.

- The amount of BERT SJ magnitude which shall be adjusted (the amount is relative number for addition/reduction, the amount is after applying reference CDR mask). Single value for all SJ frequencies.
- ECOM convergence values

```

LinkOperatingMarginEvaluationRX  x  +
File Edit View

Electrical Compliance Test Specification for GEN4
Date:,08-Jul-2024
DIR:.,C:\20240705_USB4V2_Case2a_Test_channel\RX0\
File:, BERT_Sdd21.bin
Calibration:,End-to-End Channel ILfit at Nyquist,-28.1,[dB],CTS: Min , -29,CTS: Max, -28
Calibrate to:.,TX_SJ_increase [mUIp-p],-10.000000,CTS: Min,-10,CTS: Max,+10
Calibration:,ECOM Convergence init value,-0.291000
Calibration:,ECOM Convergence final value,-0.011800,CTS: Min,-.1,CTS: Max,+.1
Informative:,Symbol Rate [GHz],25.600004,Drift [PPM],0.160000
  
```

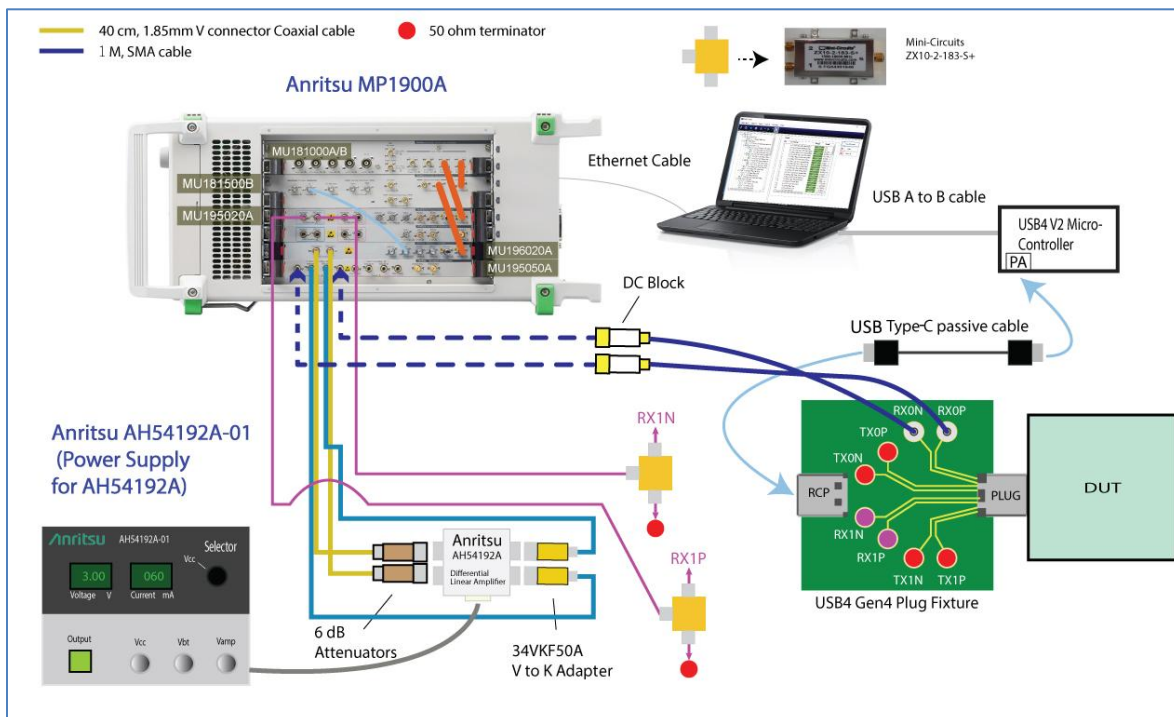
3. Perform the following required adjustments:

- Recall the BERT calibration setup for Test Case 2.
- Adjust the SJ magnitude for every SJ frequency.

9.16 USB4 Gen 4 TER Test Case 1

After completing the Case 1 calibration, proceed to perform the test as follows:

1. Set up the physical equipment connections, as shown below.



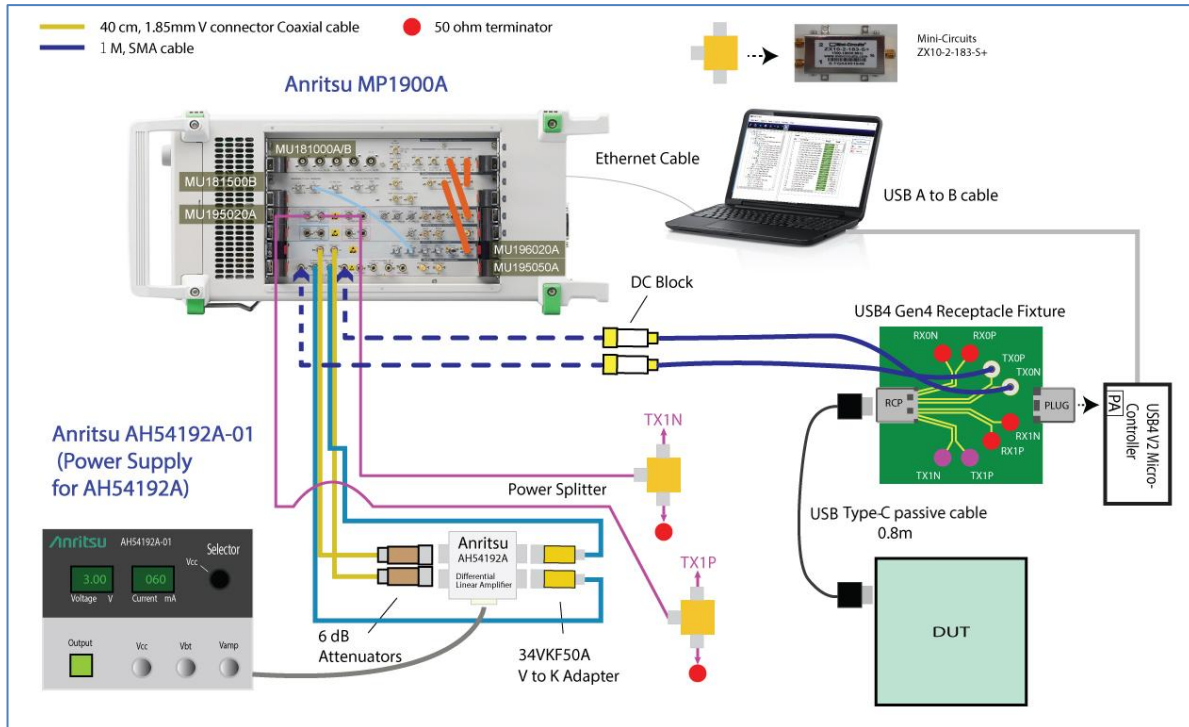
2. Recall the BERT test Case 1 calibrated setup.
3. Activate the Receiver under test with maximum number of aggressor lanes configured as transmitters generating PRTS19 with preset#0 to 50Ω termination. Activate the remaining Receivers, incoming signal detection is not required (refer to the CTS Appendix A.1 for correct Lane configuration and CTS Appendix A.2 for correct Aggressors setup activation).

4. Initiate negotiation with the preset chosen in calibration.
5. Perform the following error counter check phase (skip this section if already performed for this Lane):
 - Run and follow the ETT procedure to change the preset and pattern of the BERT as requested by the ETT.
 - Initiate continuous random error stream injection targeting TER ratio of $1\text{E-}6$ using the BERT.
 - Start the TER test for 3 seconds.
 - Read the TER ratio as reported by the ETT.
 - If the TER ratio result is $1\text{E-}6 \pm 1.5\text{E-}7$ then the test is considered as Passed, or otherwise Failed.
 - Error injection with reduced/disabled jitter impairments is acceptable.
 - Error counter check shall be performed once per lane.
6. Perform the following TER test phase:
 - Run and follow the ETT procedure to change the preset and pattern of the BERT as requested by the ETT.
 - Start the TER test for 30 seconds.
 - Read the TER ratio as reported by the ETT.
 - If the TER ratio is $< 1\text{E-}8$ then the test is considered as Passed, or otherwise Failed.
7. Repeat all steps above including equalization training for each PJ frequency: 1MHz, 2MHz, 10MHz, 50MHz and 100MHz.
8. Repeat all steps above for each Receiver Lane.

9.17 USB4 Gen 4 TER Test Case 2

After completing the Case 2 calibration, proceed to perform the test as follows:

1. Set up the physical equipment connections, as shown below.



2. Recall the BERT test Case 2 calibrated setup.
3. Activate the Receiver under test with maximum number of aggressor lanes configured as transmitters generating PRTS19 with preset#0 to 50Ω termination. Activate the remaining Receivers, incoming signal detection is not required (refer to the CTS Appendix A.1 for correct Lane configuration and CTS Appendix A.2 for correct Aggressors setup activation).
4. Initiate negotiation with the preset chosen in calibration.
5. Perform the following error counter check phase (skip this section if already performed for this Lane):
 - Run and follow the ETT procedure to change the preset and pattern of the BERT as requested by the ETT.
 - Initiate continuous random error stream injection targeting TER ratio of 1E-6 using the BERT.
 - Start the TER test for 3 seconds.
 - Read the TER ratio as reported by the ETT.
 - If the TER ratio result is $1E-6 \pm 1.5E-7$ then the test is considered as Passed, or otherwise Failed.
 - Error injection with reduced/disabled jitter impairments is acceptable.
 - Error counter check shall be performed once per lane.
6. Perform the following TER test phase:

- Run and follow the ETT procedure to change the preset and pattern of the BERT as requested by the ETT.
 - Start the TER test for 30 seconds.
 - Read the TER ratio as reported by the ETT.
 - If the TER ratio is $< 1E-8$ then the test is considered as Passed, or otherwise Failed.
7. Repeat all steps above including equalization training for each PJ frequency: 1MHz, 2MHz, 10MHz, 50MHz and 100MHz.
 8. Repeat all steps above for each Receiver Lane.

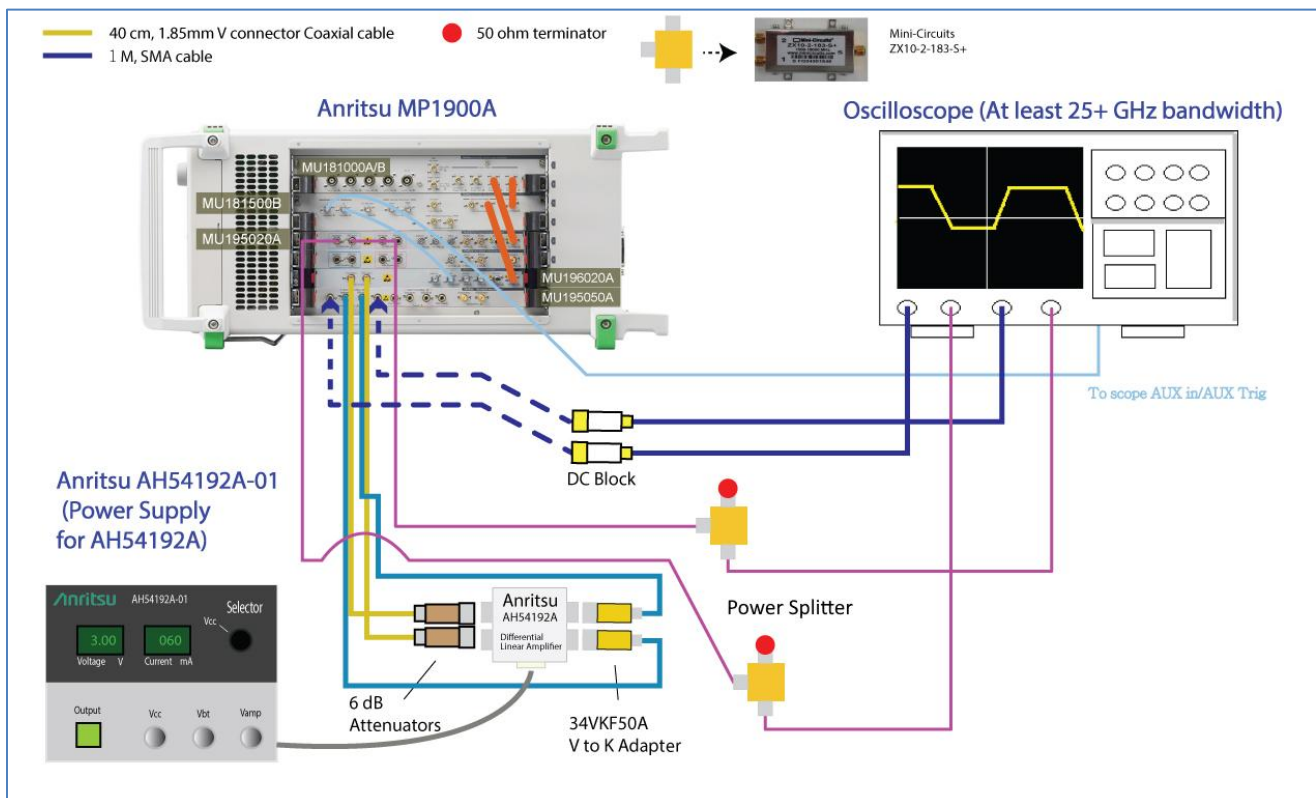
9.18 Receiver Frequency Variation Calibration for Case 1

After completing the Case 1 calibration, proceed to perform the receiver frequency variation calibration for Case 1 as follows:

TABLE 14. OSCILLOSCOPE SETUP FOR RECEIVER FREQUENCY VARIATION CALIBRATION FOR CASE 1

Setting	Setup
Sample Rate	128 Gs/s for Keysight UXR scope and 80 Gs/s for other vendor scope
Record Length	64M for Keysight UXR scope and 40M for other vendor scope in a single acquisition
Bandwidth	25GHz
Vertical Scale	Set to full screen without clipping
CDR	OFF
Averaging	OFF
Sin x/x	OFF

1. Set up the physical equipment connections, as shown below.



2. Recall the BERT test Case 1 calibrated setup for PJ 100MHz.
3. Configure BERT to output PRTS7 with SSC down-spreading disabled.
4. Construct the frequency variation dynamics as shown in Figure 78 below. Refer to USB4 Version 2.0 Specification Table 3-26. Tolerance is ± 25 ppm with respect to USB4 Version 2.0 Specification targets.

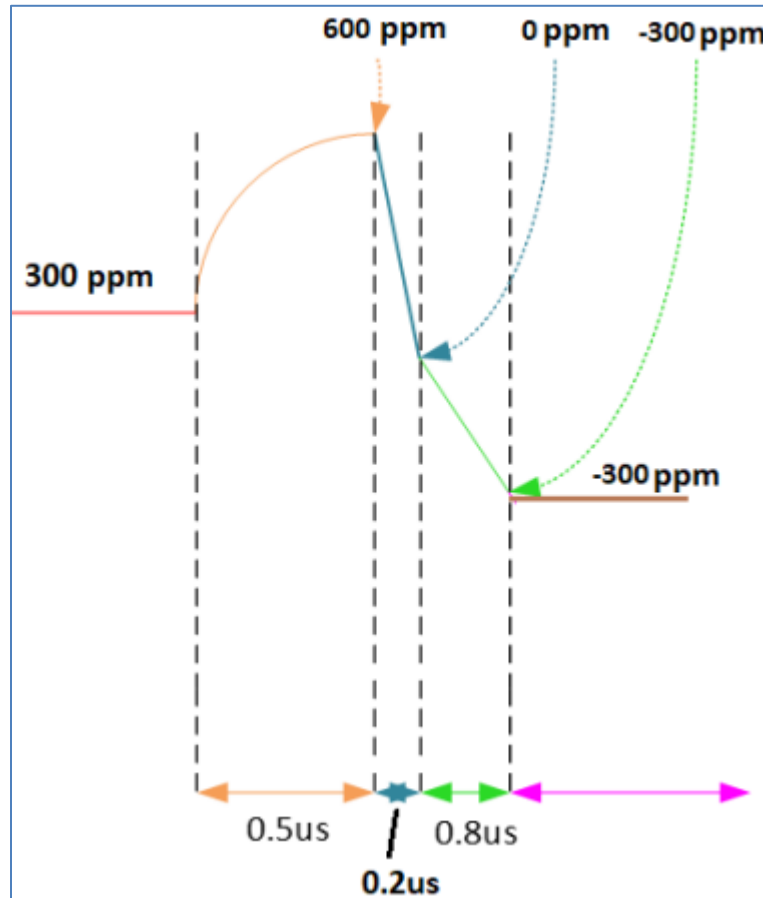
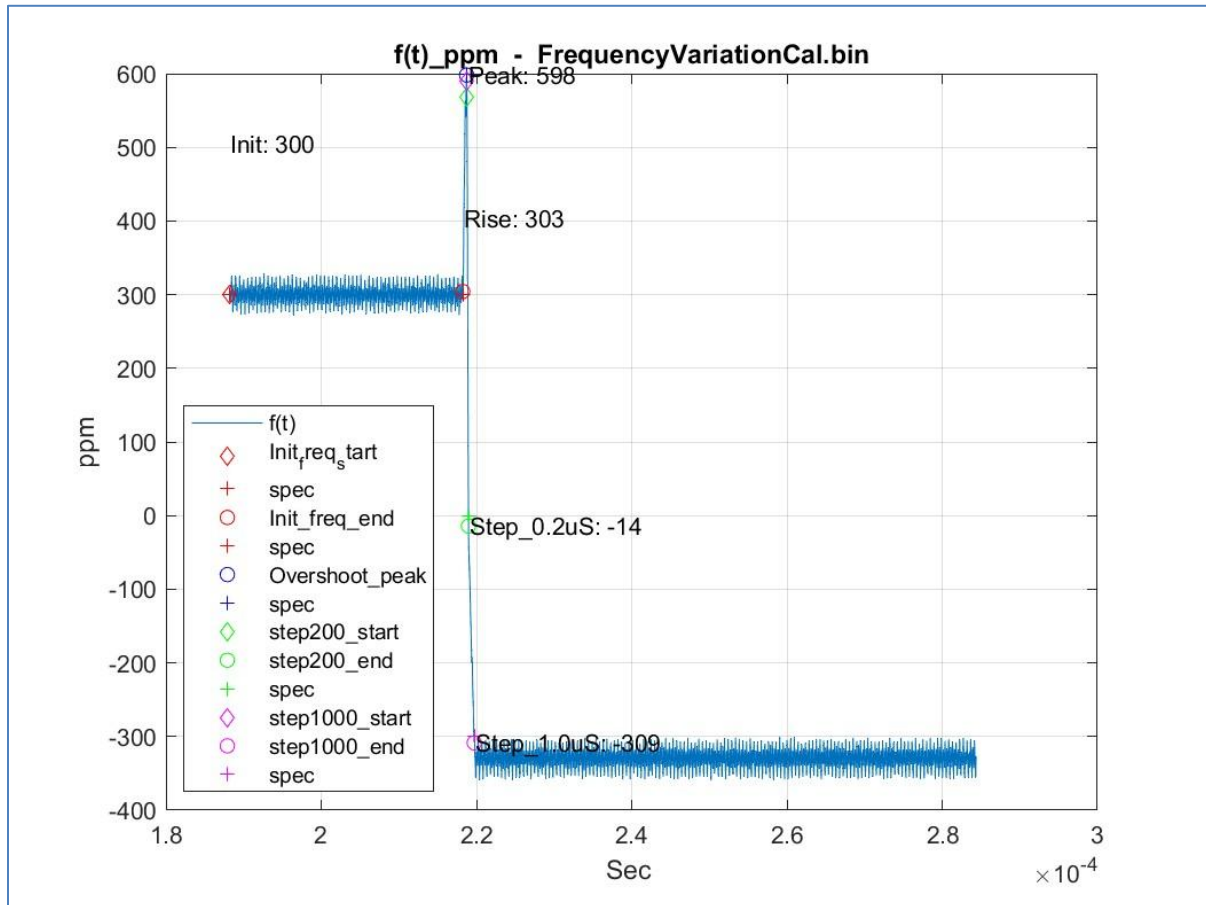


FIGURE 78. FREQUENCY VARIATION DYNAMICS FOR CASE 1

5. Capture the differential output signal with frequency variation dynamics waveform on the scope.
6. Run the SigTest tool according to section 8.4.1 of the SigTest User Manual documentation.
7. Check the SigTest report for the frequency variation parameters if all Passed.
8. If Failed, adjust the frequency variation parameters on the BERT setting and repeat steps 5-8 until all desired results are achieved.

Electrical Compliance Test Specification for GEN4						
Date:	#####					
DIR:	C:\GRL\Rx Test Solution\Applications\USB4_V2_AN_RxTest\AppData\Wav					
File:	FrequencyVariationCal.bin					
RX Frequency Variation Training Measurement:						
INIT_FREQ_VARIATION:	PASS	RX_INIT	300.285 CTS: Min	275 CTS: Max	325	
DELTA_FREQ_200ns:	PASS	RX_DEL	581.563 CTS: Min	575 CTS: Max	625	
DELTA_FREQ_1000ns:	PASS	RX_DEL	898.92 CTS: Min	875 CTS: Max	925	
FREQ_OVERSHOOT:	PASS	RX_FREQ	598.155 CTS: Min	575 CTS: Max	625	
STEADY_STATE_FREQ_VARIATION:	PASS	RX_STEA	-320.73 CTS: Min	-325 CTS: Max	-275	
Informative:	Symbol R 25.5983 Drift [PPM] -65.28					



9. For the SigTest measurement, use the following template:

- Test Point: tp3_prime
- CTS Test Template: frequency_variation_training
- Command example:

```
. \USB4_SigTest.exe gen4 rx tp3_prime frequency_variation_training
C:\SigTest_USB4_CTS\Waveforms\ rx_frequency_variation_gen4_tp3_prime.bin
none rx_frequency_variation_calibration_tp3_prime none
```

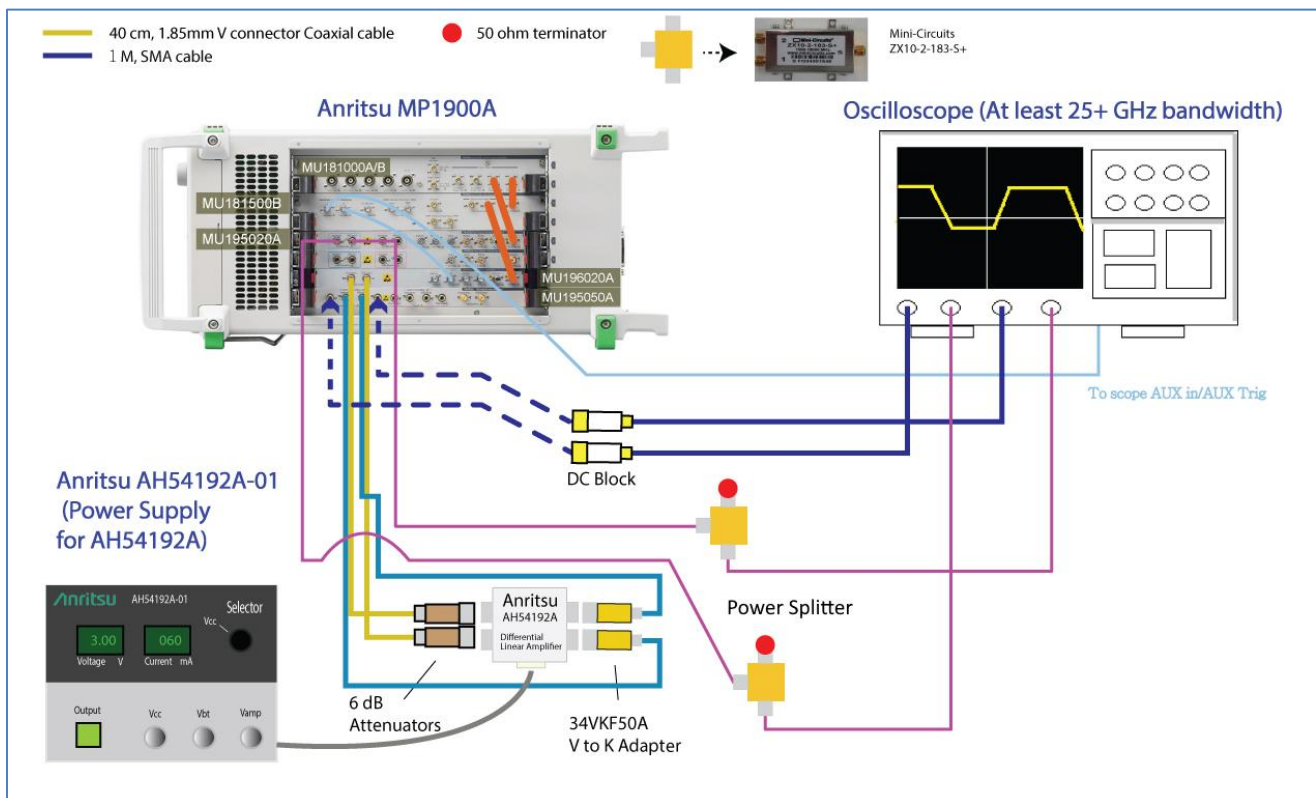
9.19 Receiver Frequency Variation Calibration for Case 2

After completing the Case 2 calibration, proceed to perform the receiver frequency variation calibration for Case 2 as follows:

TABLE 15. OSCILLOSCOPE SETUP FOR RECEIVER FREQUENCY VARIATION CALIBRATION FOR CASE 2

Setting	Setup
Sample Rate	128 Gs/s for Keysight UXR scope and 80 Gs/s for other vendor scope
Record Length	64M for Keysight UXR scope and 40M for other vendor scope in a single acquisition
Bandwidth	25GHz
Vertical Scale	Set to full screen without clipping
CDR	OFF
Averaging	OFF
Sin x/x	OFF

1. Set up the physical equipment connections, as shown below.



2. Recall the BERT test Case 2 calibrated setup for PJ 100MHz.
3. Configure the BERT to output PRTS7 with SSC down-spreading disabled.
4. Construct the frequency variation dynamics as shown in Figure 79 below. Refer to the USB4 Version 2.0 Specification Table 3-26. Tolerance is ± 25 ppm with respect to the USB4 Version 2.0 Specification targets.

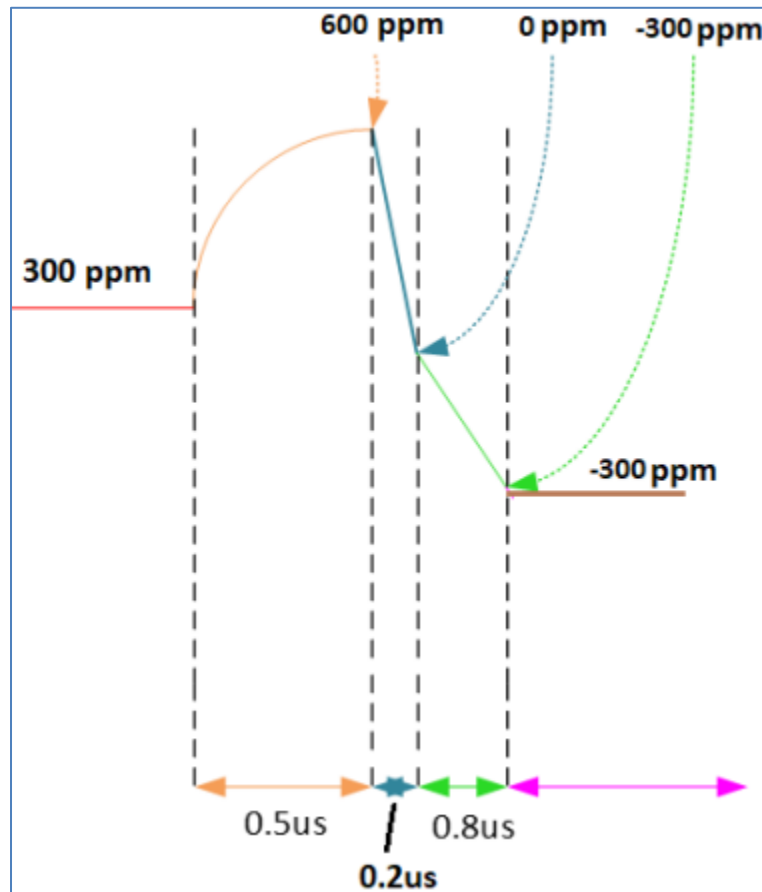
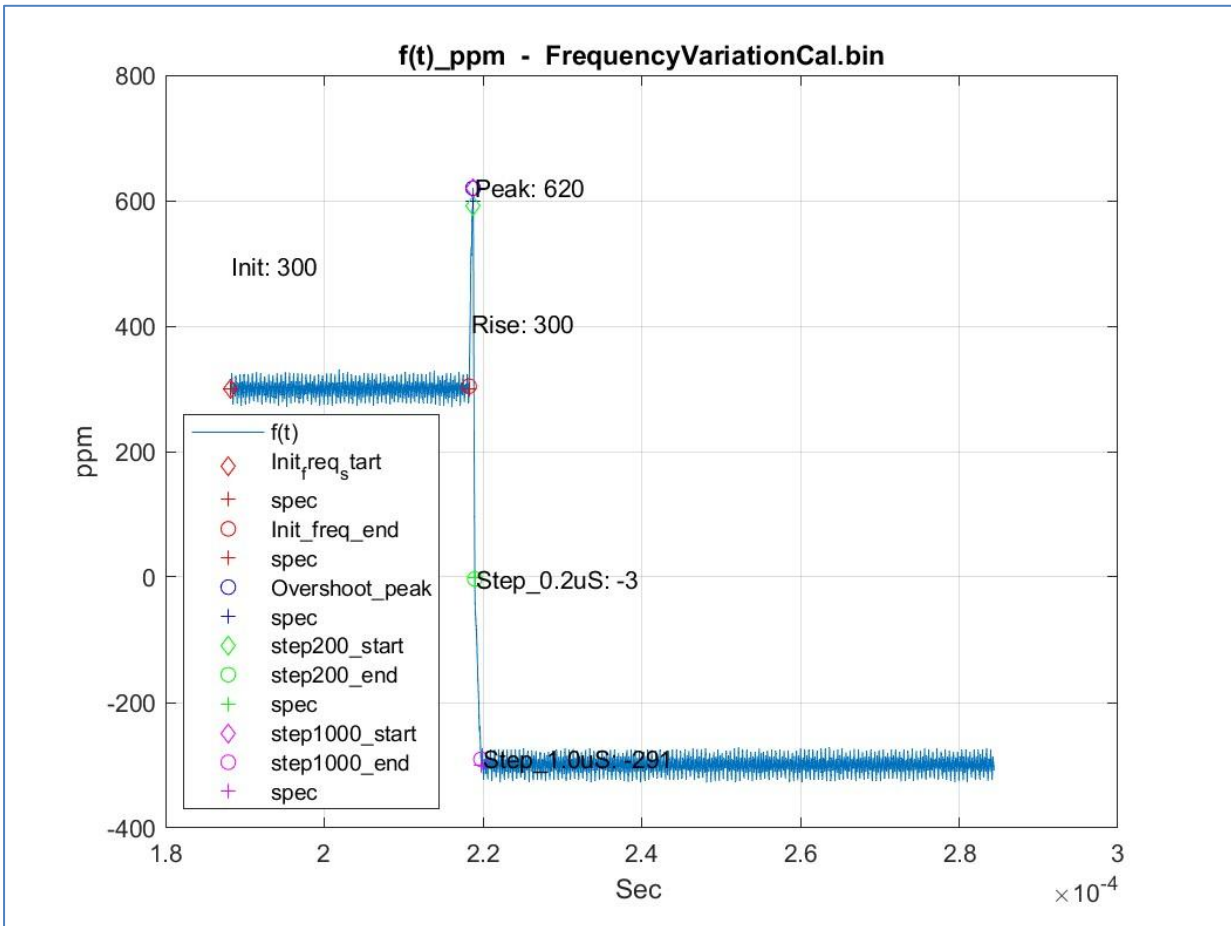


FIGURE 79. FREQUENCY VARIATION DYNAMICS FOR CASE 2

5. Capture the differential output signal with frequency variation dynamics waveform on the scope.
6. Run the SigTest tool according to section 8.4.1 of the SigTest User Manual documentation.
7. Check the SigTest report for frequency variation parameters if all Passed.
8. If Failed, adjust the frequency variation parameters on the BERT setting and repeat steps 5-8 until all the desired results are achieved.

Electrical Compliance Test Specification for GEN4							
Date:	#####						
DIR:	C:\GRL\Rx Test Solution\Applications\USB4_V2_AN_RxTest\AppData\Waveforms\						
File:	FrequencyVariationCal.bin						
RX Frequency Variation Training Measurement:							
INIT_FREQ_VARIATION:	PASS	RX_INIT	300.308	CTS: Min	275	CTS: Max	325
DELTA_FREQ_200nS:	PASS	RX_DEL	594.451	CTS: Min	575	CTS: Max	625
DELTA_FREQ_1000nS:	PASS	RX_DEL	910.401	CTS: Min	875	CTS: Max	925
FREQ_OVERSHOOT:	PASS	RX_FREQ	619.85	CTS: Min	575	CTS: Max	625
STEADY_STATE_FREQ_VAR	PASS	RX_STEA	-299.55	CTS: Min	-325	CTS: Max	-275
Informative:	Symbol R 25.5988 Drift [PPM] -47.88						



9. For the SigTest measurement, use the following template:

- Test Point: tp3
- CTS Test Template: frequency_variation_training
- Command example:

```
. \USB4_SigTest.exe gen4 rx tp3 frequency_variation_training
C:\SigTest_USB4_CTS\Waveforms\ rx_frequency_variation_gen4_tp3.bin none
rx_frequency_variation_calibration_tp3 none
```

9.20 Receiver Frequency Variation Test Case 1

After completing the Case 1 calibration, proceed to perform the receiver frequency variation test Case 1 as follows:

1. Recall the receiver frequency variation calibrated results for Case 1 from Section 9.18.
 2. Activate the receiver under test with maximum number of aggressor lanes configured as transmitters generating PRTS19 with preset#0 to 50 Ω termination. Activate the remaining receivers, incoming signal detection is not required.
 3. Perform the following TER test phase:
 - If the TS2.clksw pattern is not required for this test by the DUT, follow the TER test TYPE I or TYPE II.
 - If the TS2.clksw pattern is required for this test by the DUT, follow the TER test TYPE II only.
- a) For the TER test TYPE I:
- Start the TER test on PRTS7.
 - Run the frequency variation test on the ETT and start link training.
 - Wait for the ETT prompt window to appear to start sending frequency variation dynamics.
 - Click on the “OK” button and send the frequency variation dynamics on the BERT in 1 second.
 - Wait for 2 seconds.
 - Read the TER ratio as reported by the ETT.
 - If the TER ratio is $< 1E-4$ then the test is considered as Passed, or otherwise Failed.
- b) For the TER test TYPE II:
- Start the TER test on PRTS7.
 - Switch to the TS2.clksw pattern right after the TER test starts.
 - Wait for 2 μ seconds.
 - Apply the clock switch event within the next 8 μ seconds.
 - Switch back to the PRTS7 after 10 μ seconds after switching to TS2.clksw.
 - Wait for 2 seconds.
 - Read the TER ratio as reported by the ETT.
 - If the TER ratio is $< 1E-4$ then the test is considered as Passed, or otherwise Failed.
4. Repeat steps 1-3 10 times.
 5. Repeat all the above steps for each Receiver Lane.

Note: Refer to the CTS Appendix F for TYPE I and TYPE II.

9.21 Receiver Frequency Variation Test Case 2

After completing the Case 1 calibration, proceed to perform the receiver frequency variation test Case 2 as follows:

1. Recall the receiver frequency variation calibrated results for Case 2 from Section 9.19.
 2. Activate the receiver under test with maximum number of aggressor lanes configured as transmitters generating PRTS19 with preset#0 to 50 Ω termination. Activate the remaining receivers, incoming signal detection is not required.
 3. Perform the following TER test phase:
 - If the TS2.clksw pattern is not required for this test by the DUT, follow the TER test TYPE I or TYPE II.
 - If the TS2.clksw pattern is required for this test by the DUT, follow the TER test TYPE II only.
- a) For the TER test TYPE I:
- Start the TER test on PRTS7.
 - Run the frequency variation test on the ETT and start link training.
 - Wait until the ETT prompt window to appear to start sending frequency variation dynamics.
 - Click on the “OK” button and send the frequency variation dynamics on the BERT in 1 second.
 - Wait for 2 seconds.
 - Read the TER ratio as reported by the ETT.
 - If the TER ratio is $< 1E-4$ then the test is considered as Passed, or otherwise Failed.
- b) For the TER test TYPE II:
- Start the TER test on PRTS7.
 - Switch to the TS2.clksw pattern right after the TER test starts.
 - Wait for 2 μ seconds.
 - Apply the clock switch event within the next 8 μ seconds.
 - Switch back to PRTS7 after 10 μ seconds after switching to TS2.clksw.
 - Wait for 2 seconds.
 - Read the TER ratio as reported by the ETT.
 - If the TER ratio is $< 1E-4$ then the test is considered as Passed, or otherwise Failed.
4. Repeat steps 1-3 10 times.
 5. Repeat all the above steps for each Receiver Lane.

Note: Refer to the CTS Appendix F for TYPE I and TYPE II.

10 Appendix B: Receiver Stressed Eye Calibration Using SigTest

The SigTest post processing analysis application can be run to ensure signal quality compliance for the USB4 V2 receiver stressed eye calibration.

Below provides a summary of the SigTest requirements. Please refer to the USB4 V2 SigTest User Manual from USB-IF for the full set of instructions to perform SigTest measurements.

Note: It is required that you are a member of USB-IF and have attained the proper permissions from USB-IF in order to have access to the USB4 V2 SigTest User Manual.

10.1 Install and Run SigTest

[Note: The following procedure was extracted from the “USB4 SigTest installation and running:” section in the USB4 V2 SigTest User Manual.]

First, make sure that $\geq 16\text{GB}$ RAM (or recommended 32GB RAM and higher) is available on the Controller PC or Scope where SigTest is to be run.

1. Install Matlab Runtime Compiler MCR R2024a (24.1).
2. Create a new folder, for example “SigTest_USB4_CTS” and place the “USB4_SigTest.exe” file into the folder. Run the “USB4_SigTest.exe”.
3. Open PowerShell window from the folder by pressing SHIFT + Right mouse button and then click on “Open PowerShell window here”.

10.2 Set Up Scope for Saving Waveforms

[Note: The following description was extracted from the “Scope definitions for saving waveforms:” section in the USB4 V2 SigTest User Manual.]

- a) Scope requirements and settings:
 - Sampling Rate: $\geq 80\text{GSa/s}$
 - Evaluated record length: $500\mu\text{s}$ per channel
 - No CDR, no average, no interpolation and no equalization applied
 - Bandwidth: 16GHz (for USB4 Gen2) or 21GHz (for USB4 Gen3)
 - Adjust vertical scale to fit signal into Scope screen
- b) The saved waveforms for all receiver tests should be differential (for example: CH1 - CH3), except of the waveform for the AC Common Mode test that should be common (for example: $(\text{CH1} + \text{CH3})/2$).
- c) The waveforms should use the correct test pattern type and length for the respective test as specified in the CTS to avoid test interruption and termination.

11 Appendix C: Connecting Keysight Oscilloscope to PC

If using a Keysight oscilloscope, refer to the following procedure on how to connect the Scope to be used with a controller PC. The Keysight Scope can be connected to the controller PC through GPIB, USB or LAN.

1. Download the latest version of the Keysight IO Libraries Suite software from the Keysight website and install on the controller PC.
2. When installed successfully, the IO icon () will appear in the taskbar notification area of the controller PC.
3. Select the IO icon to launch the **Keysight Connection Expert**.
4. Click Rescan.

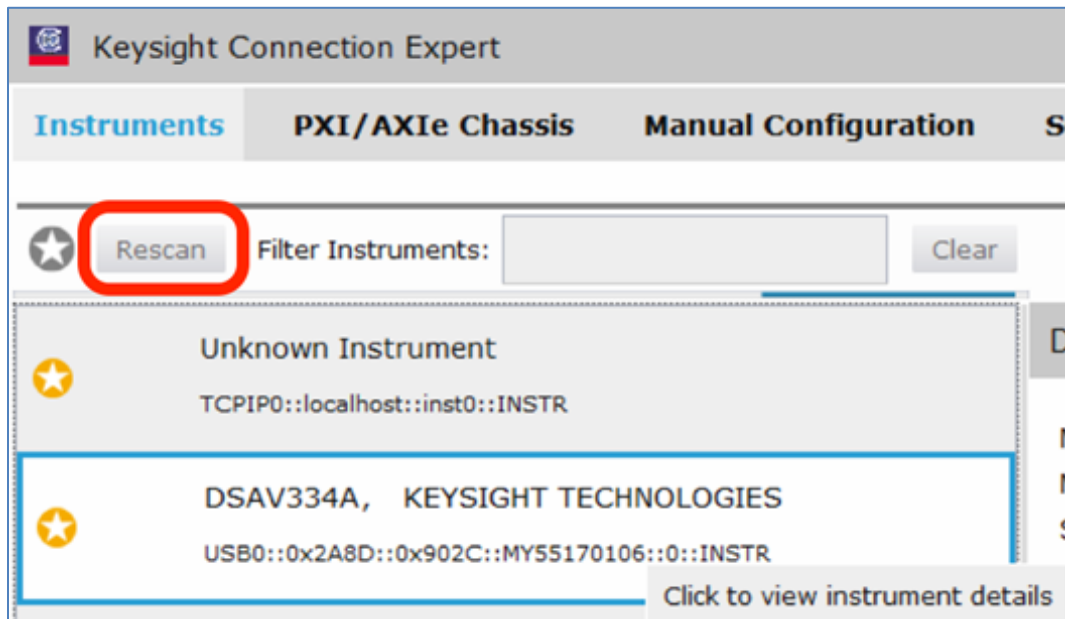


FIGURE 80. KEYSIGHT CONNECTION EXPERT

5. Refresh the system. The Keysight Scope is shown on the left pane and the VISA address is shown on the right pane.

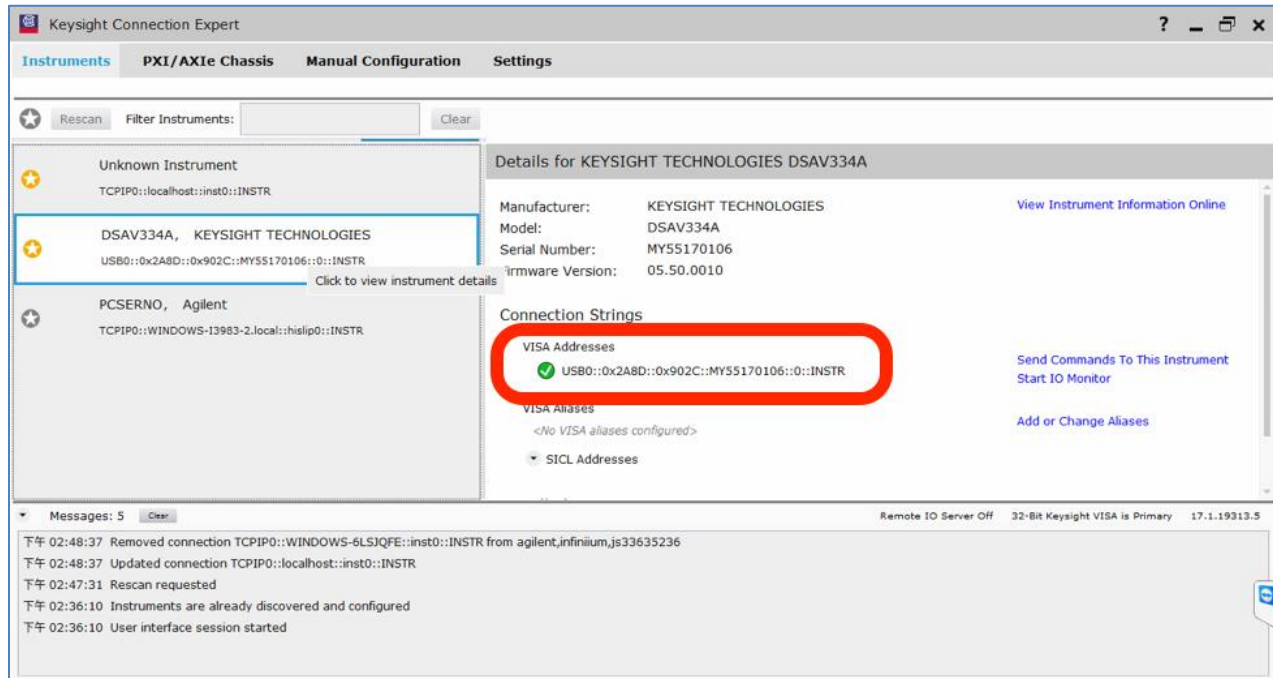


FIGURE 81. OSCILLOSCOPE'S VISA ADDRESS

6. When connecting the Keysight Scope to the PC through GPIB/USB, type in the VISA address into the 'Address' field on the Equipment Setup page of the GRL-USB4-V2-RXA application. If the GRL-USB4-V2-RXA application is installed on the Keysight Scope, type in the Scope IP address, for example "TCPIP0::127.0.0.1::inst0::INSTR". If the GRL-USB4-V2-RXA application is installed on the controller PC to control the Scope via LAN, type in the Scope IP address, for example "TCPIP0::192.168.0.100::inst0::INSTR". Note to **omit** the Port number from the address.

If there is error in connection, type in the Scope IP address as "TCPIP0::192.168.0.100::5025::SOCKET".

12 Appendix D: Connecting Tektronix Oscilloscope to PC

If using a Tektronix DPOJET Series oscilloscope, refer to the following procedure on how to connect the Scope to be used with a controller PC. The Tektronix Scope can be connected to the controller PC through GPIB, USB or LAN.

1. Download the latest version of the Tektronix TekVISA software from the Tektronix website and install on the controller PC.
2. When installed successfully, open the OpenChoice Instrument Manager application.

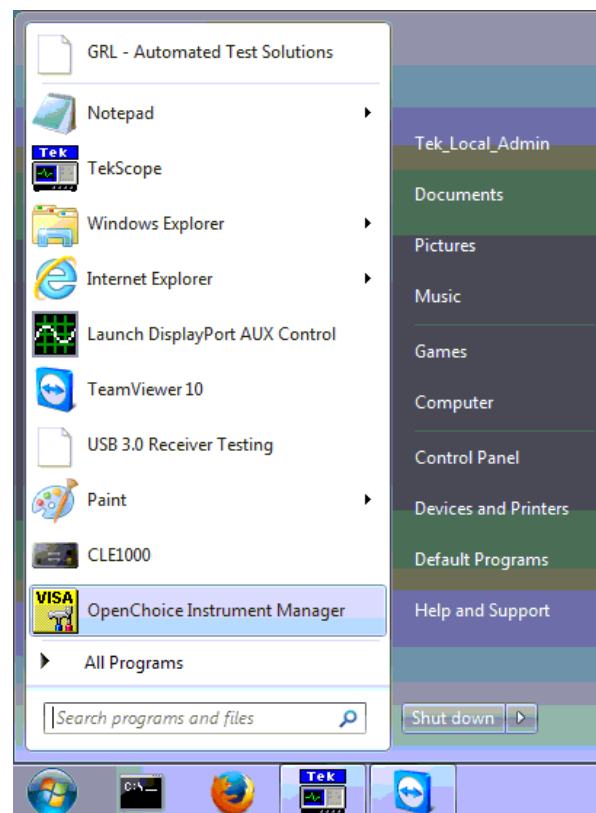


FIGURE 82. OPENCHOICE INSTRUMENT MANAGER IN START MENU

3. The left “Instruments” panel on the OpenChoice Instrument Manager will display all connected instruments. The functional buttons below the “Instruments” panel – “Instrument List Update”, “Search Criteria”, “Instrument Identify” and “Properties” can be used to detect the Scope in case it does not initially appear under “Instruments”.
 - “Instrument List Update”: Select to refresh the instrument list and locate new instruments connected to the controller PC.
 - “Search Criteria”: Select to configure the instrument search function.
 - “Instrument Identify”: Select to use a supported programming language to send a query to identify the selected instrument.
 - “Properties”: Select to display and view the selected instrument properties.

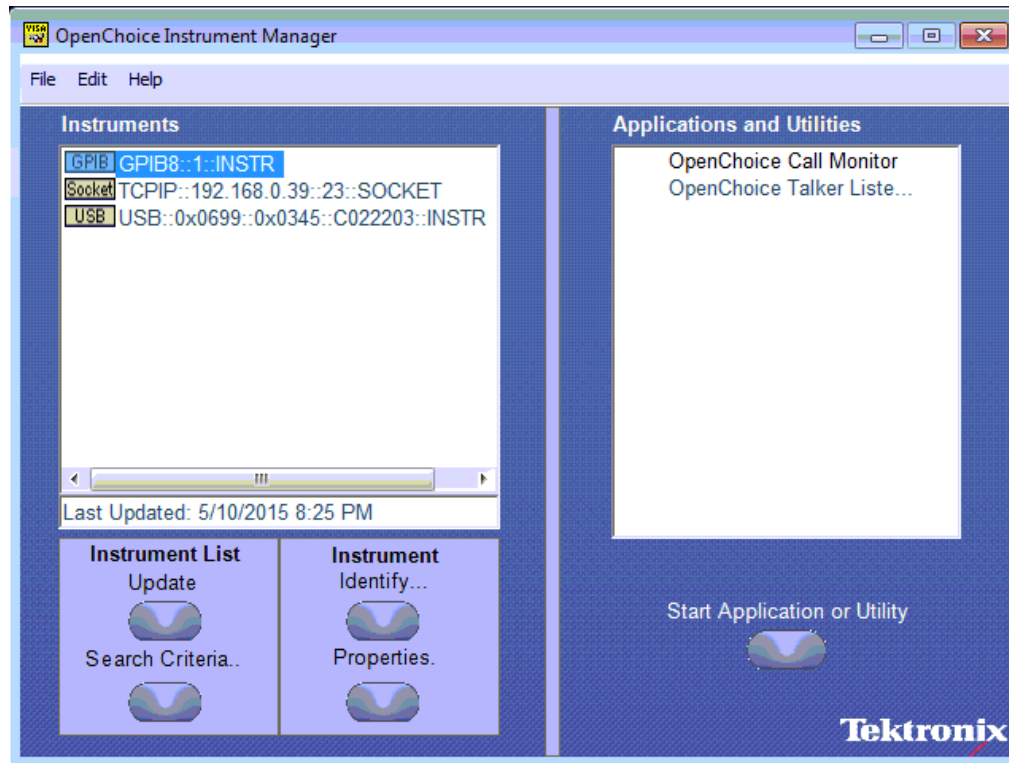


FIGURE 83. OPENCHOICE INSTRUMENT MANAGER MENU

4. If connecting the Tektronix Scope to the controller PC via USB, select the “Search Criteria” function to ensure that USB connection is enabled, and then select the “Instrument List Update” function. When the Scope appears on the “Instruments” panel, select it and then go to the “Instrument Identify” function. This will display the model and serial number of the Scope once detected. Select the “Properties” function to view the Scope address.
5. If connecting the Tektronix Scope to the controller PC via LAN, the Scope IP address must be pre-determined beforehand. Then select the “Search Criteria” function to ensure that LAN connection is enabled and type in the Scope IP address. When the Scope shows up in the list, select it followed by “Search”. The Scope should then appear on the “Instruments” panel. Select it and access the “Instrument Identify” function to view the Scope model and serial number as well as the “Properties” function to view the Scope address.
6. On the Equipment Setup page of the GRL-USB4-V2-RXA application, type in the Scope address into the ‘Address’ field. If the GRL-USB4-V2-RXA application is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example “GPIB8::1::INSTR”. If the GRL-USB4-V2-RXA application is installed on the controller PC to control the Scope, type in the Scope IP address, for example “TCPIP0::192.168.0.100::inst0::INSTR”. Note to **omit** the Port number from the address.

END_OF_DOCUMENT